Fabrication of high temperature carrier-selective passivating contact solar cells for application in monolithic perovskite/c-Si tandem devices

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Fabrication of high temperature carrier-selective passivating contact solar cells for application in monolithic perovskite/c-Si tandem devices

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Abstract

Crystalline silicon homojunction architectures like aluminum back-surface field (BSF) and passivated emitter and rear cell (PERC) dominated the solar cell market for the last decades. Recently, carrier-selective passivating contact (CSPC) designs have shown that they can effectively reduce recombination losses and exhibit efficiencies above 25 % which approaches the Shockley-Queisser limit of single-junction solar cells. To overcome this intrinsic efficiency limit, research and industry have started to investigate multijunction devices which utilize two different absorber layers in order to reduce the spectral mismatch losses. In this project, the focus lies on the fabrication of a high temperature CSPC bottom cell based on polycrystalline silicon oxide (poly-SiO_x) for the application in a monolithic perovskite/crystalline silicon (c-Si) tandem device. Poly-SiO_x features a higher transparency due to the wider band gap which can decrease the free-carrier absorption (FCA) and induce larger band bending in comparison to the classic polycrystalline silicon (poly-Si) contacts.

To fabricate such a c-Si solar cell, the passivation of the contacts was optimised using symmetric lifetime samples. It was found that the optimal processing conditions for the dry thermal oxidation process and the high temperature annealing step are 675 °C for 3 minutes and 900 °C for 15 minutes, respectively. This resulted in an implied open-circuit voltage (iV_{OC}) for the n-doped and p-doped symmetric samples after hydrogenation of 745 mV and 670 mV, respectively. Similarly, the minority charge carrier lifetime at $10^{15}/cm^3$ was above 10 ms for the polished n-type sample and 1.1 ms for the textured p-type sample.

Those optimised processing conditions were adopted for the fabrication of a single-junction n-type front-side polished and p-type rear-side textured CSPC solar cell. This resulted in a device with an efficiency of 16.67 %. By lowering the thermal budget of the recovery annealing conditions after the sputtering of the transparent conductive oxide (TCO) the passivation properties are restored more effectively. It is believed that this improvement stems mainly from the reduction of the defect formation during the annealing step. This resulted in a strongly enhanced single-junction solar cell with a final efficiency of 18.76 %. Other techniques to improve the performance like the modification of the p-layer thickness, the incorporation of an additional annealing step after the a-Si deposition, or the introduction of indium tungsten oxide (IWO) as the TCO did not result in an improvement of the final solar cell efficiency. Optical simulations were performed in GenPro4 to investigate the optical performance of the single-junction solar cell. It was found that the potential is mostly limited by reflection losses and parasitic absorption in the emitter layers.

Furthermore, a monolithic perovskite/c-Si tandem device was fabricated in cooperation with TU Eindhoven. It is important to note that the fabricated device is based on the first single-junction solar cell which does not include the implementation of the improved TCO recovery annealing step. The final tandem solar cell exhibits an efficiency of 23.1 %.

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Nomenclature

ARC	Anti-reflection coating
a-Si	Amorphous silicon
a-SiO_x	Amorphous silicon oxide
BHF	Buffered hydrofluoric acid
BSF	Back surface field
CSPC	Carrier-selective passivating contacts
c-Si	Crystalline silicon
ETL	Electron transport layer
FBC	Front-back contacted
FCA	Free-carrier absorption
FGA	Forming gas annealing
GHG	Greenhouse gas
HF	Hydrofluoric acid
HIT	Heterojunction with intrinsic thin layer
HTL	Hole transport layer
J_{SC}	Short-circuit current density
ITO	Indium tin oxide
iV_{OC}	Implied open-circuit voltage
IWO	Indium tungsten oxide
LCOE	Levelized cost of electricity
LID	Light-induced degradation
LPCVD	Low-pressure chemical vapor deposition
NIR	Near-infrared region
HNO_3	Nitric acid
PECVD	Plasma-enhanced chemical vapor deposition
PERC	Passivated emitter and rear cell
PERL	Passivated emitter and rear, locally-diffused
PERT	Passivated emitter and rear, totally-diffused
POLO	Polycrystalline silicon on oxide
poly-Si	Polycrystalline silicon
poly-SiO_x	Polycrystalline silicon oxide
QSSPC	Quasi-steady-state photoconductance
SHJ	Silicon heterojunction
SiO_x	Silicon oxide
SQ	Shockley-Queisser
TCO	Transparent conductive oxide
TMAH	Tetramethylammonium hydroxide
TOPCon	Tunnel oxide passivating contacts
TRJ	Tunnel recombination junction
UV	Ultraviolet

1

Introduction

The first chapter presents the motivation, the objectives and the outline of this thesis. The motivation addresses the current global climate situation, clarifies the importance of renewable energy research and discusses the impact of the thesis topic. Next, the objectives of the research questions are defined and explained. Lastly, in the outline a short overview of the different chapters is presented.

1.1 Motivation

The international debate concerning climate change is now greater than ever and global warming is seen as one of the most important challenges of the 21st century [24]. In recent years, the subject gained public attention due to an increased effort of the scientific community to highlight the dangers of this development [25]. This caused government treaties and international movements like the Paris Climate Agreement in 2015 and Fridays for Future. However, climate change research is not a product of the last couple of decades. One of the first and most famous individuals who acknowledged climate change was one of the founding fathers of the United States, Thomas Jefferson. He noticed changes in the weather during his lifetime which he related to the increased amount of cleared and cultivated land. By the end of his life he strongly believed in human-induced climate change and proposed to quantify it through measurements. [26, p.24-34].

Nowadays, land use still plays a role in anthropogenic climate change due to changes in albedo and deforestation [27], but the main cause of global warming is greenhouse gas (GHG) emissions from burning fossil fuels. By increasing the number of GHG molecules in the atmosphere, the amount of energy unable to exit our planet rises and as a result, the temperature on earth increases [28, p.133-137]. This rise in temperature is already happening. Anthropogenic activities caused the temperature to increase by 1 °C in comparison to pre-industrial levels and will likely increase more in the decades to come if the emissions of GHG are not lowered immediately [29]. As shown in Figure 1, the average temperature rose by 1 °C since 1850 and the concentration of CO_2 in the atmosphere increased by more than 100 ppm. We are also already experiencing the effects. The rise of the sea level, lower agricultural yield, negative impacts on our drinking water resources and a higher number of extreme weather events are just some of the consequences of climate change. Without effective measures in the next years and decades, the problems will only intensify and large areas of earth might become uninhabitable for humans [30, 31].

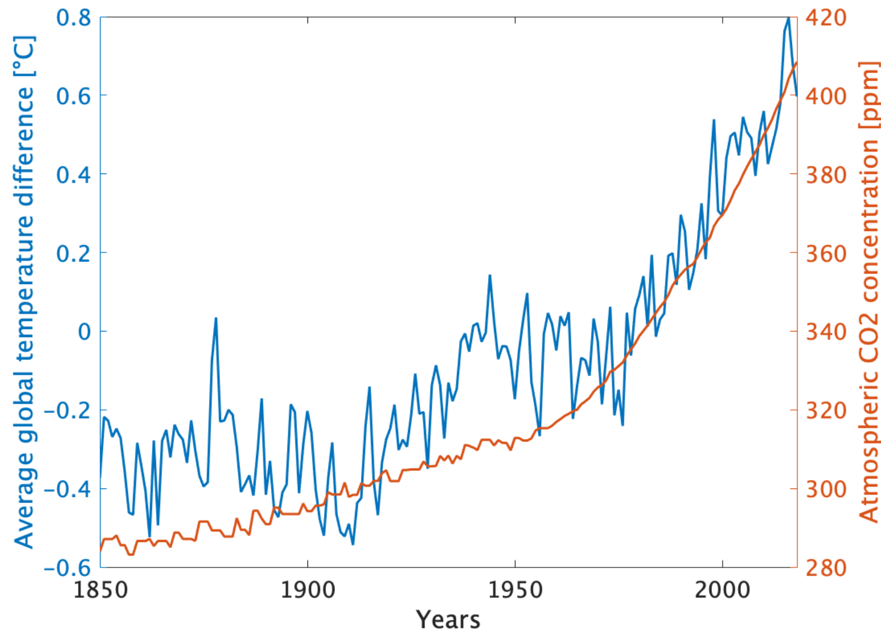


Figure 1: Average global temperature difference in °C relative to the average temperature between 1961-1990 and the increase in CO2 concentration in ppm between 1850 and 2018. Data from ourworldindata.org [1].

Three main strategies to mitigate global warming are discussed in literature [29]. First, geoengineering techniques like radiative forcing could be used to modify our planet's radiative energy budget. However, this technology is still in the very early development stage and can not be expected to make a significant contribution in the near future. Second, negative emission technologies like bioenergy carbon capture and storage, afforestation and direct air carbon capture can contribute to reducing carbon dioxide in the atmosphere. In September 2021, the Zurich based startup *Climeworks*, launched the world's largest direct air capture and storage plant in Iceland which will remove 4000 tons of CO_2 per year [32]. Lastly, the most important mitigation strategy are technologies which reduce the energy-related carbon emissions. Those include renewable energy technologies, nuclear power, fuel switching and efficiency improvements. One of the most promising and mature technology which has a great potential to reduce the energy-related carbon emissions is photovoltaic (PV) solar energy. According to the *bp Statistical Review of World Energy 2021* [33], by the end of 2020, PV solar energy has an installed worldwide capacity of 707.5 GW and the average annual growth rate in the last decade was 38.3% which makes it by far the fastest growing energy technology.

This rapid growth also strongly reduced the costs of solar PV energy systems. An analysis by the National Renewable Energy Laboratory [34] concluded that the price per Watt DC for commercial rooftop PV systems in the US reduced by 69% between 2010 and 2020 with the total hardware costs (modules and BOS components) contributing about 78% of the decline. The cost reduction of PV modules was approximately 85% over the span of the 10 years. A study by the Frauenhofer Institute for Solar Energy Systems [2] in Germany compared the levelized cost of electricity (LCOE) for renewable energy technologies

with conventional power plants. The result, displayed in Figure 2, shows that utility-scale PV power plants are already the cheapest solution for electricity production in Germany with a minimum price of just above 3 €cent per kWh. In comparison, the cheapest fossil fuel alternative is the closed-cycle gas turbine power plant with costs of around 8 €cent per kWh.

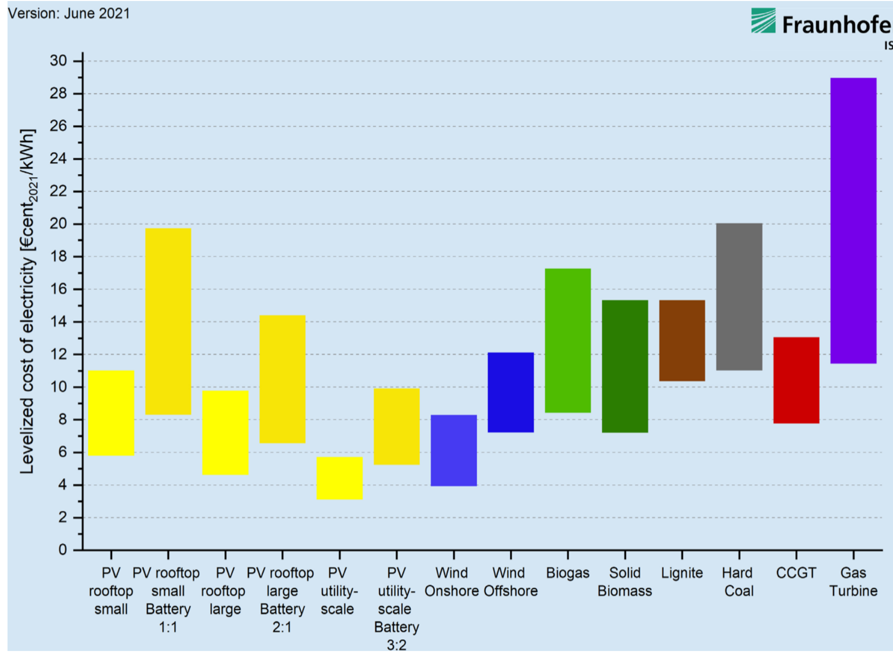


Figure 2: A comparison of the LCOE for different energy technologies in Germany. The ratio for PV battery systems expresses PV power output (kWp) over usable battery usable capacity (kWh) [2].

The price of PV systems is expected to further decrease over the next years. The LCOE of PV ground-mounted systems in Germany is estimated to be about 2.5 €cent per kWh in 2028 and cross the 2 €cent per kWh barrier in 2038 [2]. This challenge, to further decrease the LCOE, can be achieved by improving the efficiency of solar cells [35, 36]. In 2019, silicon-based solar cells made up about 95 % of the market [37]. The current record efficiency for single-junction crystalline silicon (c-Si) solar cells is 26.7 % [38], with the theoretical efficiency limit being 29.4 % [39]. One of the most promising ways to exceed this intrinsic efficiency limit is by using multijunction solar cells. Those devices combine multiple solar cells which utilize different parts of the light spectrum and hence, improve the theoretical efficiency limit [40]. Many different multijunction devices have been researched in the past. One approach is the use of a perovskite top cell and a crystalline silicon bottom cell. An overview of perovskite/c-Si tandem devices which have been investigated in the past is presented in Table 1. Until now, most perovskite/c-Si tandem devices utilize either a classic silicon homojunction solar cell or a silicon heterojunction (SHJ) solar cell based on the HIT contact scheme (heterojunction with intrinsic thin layer). HIT solar cells are based on c-Si with low temperature carrier-selective passivating contacts (CSPC). The 'low temperature' refers to the processing conditions since HIT solar cells are thermally unstable and can only withstand processing temperatures up to approximately 300 °C [41].

Another option, which will be evaluated in this work, is the use of crystalline silicon bottom cells with high temperature CSPC. They are based on a silicon oxide (SiO_x) tunneling

Table 1: Summary of previous research on monolithic perovskite/c-Si multijunction solar cells stating the authors, the institute, the date of publication, the power conversion efficiency (PCE), the type of tunnel recombination junction (TRJ), the type of bottom cell, the cell area, the short-circuit current density (J_{SC}), the open-circuit voltage (V_{OC}) and the fill factor (FF).

Author	Institute	Date of Publication	PCE [%]	TRJ	Bottom Cell	Area [cm^2]	J_{SC} [mA/cm^2]	V_{OC} [V]	FF [%]	Reference
Tockhorn et al.	HZB	2022, Mar	29.8	ITO	HIT	1	19.56	1.92	79.4	[42]
Kohnen et al.	HZB	2021, May	27.9	ITO	HIT	1	17.81	1.94	80.89	[43]
-	OXPV	2021, Jan	29.5	-	-	1.121	20.26	1.88	77.3	[38]
Al-Ashouri et al.	HZB	2020, Dec	29.1	ITO	HIT	1.064	19.26	1.90	79.52	[44]
Schulze et al.	FHISE	2020, May	25.1	ITO	HIT	0.25	17.7	1.77	80.3	[45]
Chen et al.	UNC	2020, Apr	26.1	ITO	HIT	0.42	19.2	1.82	75.3	[46]
Zheng et al.	UNSW	2019, Oct	23.0	none	Homo	4	16.5	1.73	81	[47]
Bett et al.	FHISE	2019, Sep	19.9	ITO	HIT	0.25	14.6	1.83	74.3	[48]
Köhnen et al.	HZB	2019, May	25.0	ITO	HIT	1	17.81	1.78	78.64	[49]
Nogay et al.	EPFL	2019, Mar	25.1	nc-Si	poly-SiC_x	1.42	19.5	1.74	74.7	[50]
Mazzarella et al.	HZB	2019, Feb	25.2	ITO	HIT	1.1	19.0	1.79	74.6	[51]
Hou et al.	TJU	2019, Jan	20.4	ITO	HIT	0.13	15.95	1.83	70.0	[52]
-	OXPV	2018, Dec	28.0	-	-	1.03	19.75	1.80	78.7	[53]
Shen et al.	ANU	2018, Dec	24.1	none	Homo	1	17.8	1.76	78.1	[54]
Hou et al.	NKU	2018, Nov	21.9	ITO	HIT	-	16.89	1.75	74.2	[55]
Chen et al.	UNL	2018, Oct	25.4	ITO	HIT	0.42	17.8	1.80	79.4	[56]
Jost et al.	HZB	2018, Oct	25.5	ITO	HIT	0.81	18.5	1.76	78.5	[57]
Zheng et al.	UNSW	2018, Aug	21.8	none	Homo	1	16.2	1.74	78.0	[58]
Bush et al.	SU	2018, Aug	25.0	ITO	HIT	1	18.4	1.77	77.0	[59]
Sahli et al.	EPFL	2018, Jun	25.2	nc-Si	HIT	1	19.5	1.79	73.1	[60]
Zheng et al.	UNSW	2018, Jun	20.5	none	Homo	4	16.1	1.68	78.0	[61]
Sahli et al.	EPFL	2018, Feb	22.0	nc-Si	HIT	0.25	16.8	1.75	77.5	[62]
Wu et al.	ANU	2017, Oct	22.5	ITO	Homo	1	17.6	1.75	73.8	[63]
Bush et al.	SU	2017, Feb	23.6	ITO	HIT	1	18.1	1.65	79.0	[64]
Werner et al.	EPFL	2016, Sep	16.0	ZTO	Homo	1.43	15.3	1.64	64.8	[65]
Werner et al.	EPFL	2016, Jul	20.5	IZO	HIT	1.43	16.4	1.72	73.1	[66]
Werner et al.	EPFL	2015, Dec	21.2	IZO	HIT	0.17	15.8	1.69	79.9	[67]
Werner et al.	EPFL	2015, Dec	19.2	IZO	HIT	1.22	16.1	1.70	76.7	[67]
Albrecht et al.	HZB	2015, Oct	18.1	ITO	HIT	0.16	14.0	1.76	77.3	[68]
Mailoa et al.	MIT	2015, Feb	13.7	n++	Homo	1	11.5	1.58	75.0	[69]

Abbreviations: Helmholtz-Zentrum Berlin (HZB), Oxford PV (OXPV), Frauenhofer Institute for Solar Energy Systems (FHISE), University of North Carolina (UNC), University of New South Wales (UNSW), Swiss Federal Institute of Technology Lausanne (EPFL), Tianjin University (TJU), Australian National University (ANU), Nankai University (NKU),University of Nebraska-Lincoln (UNL), Stanford University (SU), Massachusetts Institute of Technology (MIT)

layer for chemical passivation and polycrystalline silicon (poly-Si), polycrystalline silicon carbide (poly-SiC) or polycrystalline silicon oxide (poly-SiO_x) contacts for carrier extraction [10]. The advantages of a bottom cell based on high temperature CSPC compared to a SHJ bottom cell are the stability at higher temperatures which allows compatibility with current production lines and enables a good contact formation and bulk-material improvement [10, 50]. To the best of my knowledge, high temperature CSPC have only been integrated in one monolithic perovskite/c-Si tandem solar cell by Nogay et al. [50] and achieved a steady-state efficiency of 25.1%.

1.2 Objective

In this section the research objectives of the project are described. The main objective of this master thesis project is *"the fabrication of a monolithic perovskite/c-Si solar cell with high temperature carrier selective passivating contacts based on poly-SiO_x"*. This research objective is divided into multiple sub-objectives.

1. Process optimization of the polished n-type and textured p-type doped poly-SiO_x contacts in terms of the passivation quality:

    - How do the thermal oxidation conditions and the annealing conditions during

the crystallization process influence the passivation properties like implied open-circuit voltage (iV_{OC}) and minority charge carrier lifetime?

2. Fabrication and improvement of a front-back-contacted (FBC) single-side textured solar cell by investigating different aspects of the device:
   - Is a front-side polished n-type and rear-side textured p-type device based on poly-SiO_x passivating contacts feasible?
   - How does an additional annealing step after the amorphous silicon (a-Si layer) deposition influence the passivation properties?
   - How does the thickness of the doped p-layer change the sputtering damage induced by the indium tin oxide (ITO) deposition?
   - How do the annealing conditions affect the passivation recovery during the annealing process after the sputtering of the transparent conductive oxide (TCO) in terms of iV_{OC} and minority carrier lifetime?
   - How do other TCO designs influence the final device parameters?
3. Integration of the c-Si bottom solar cell based on the developed single-junction device with the perovskite top cell in cooperation with TU Eindhoven:
   - Is a 2-terminal (2T) perovskite/c-Si tandem solar cell with poly-SiO_x passivating contacts feasible?
   - What are the major limitations of such a device?

1.3 Outline

This thesis consists of 9 chapters. In this section the outline of the report is presented and the individual chapters are shortly described.

Chapter 2 reviews the basics of solid state physics with a focus on the application in solar cells. Furthermore, the working principle of photovoltaic devices and fundamental concepts are described. Lastly, the attention is aimed at the main topic of this thesis. High temperature carrier-selective passivating contacts are thoroughly discussed and multijunction devices are introduced.

In Chapter 3, the work flow and the exact conditions during the fabrication process of the devices is described in more detail. Moreover, the characterization techniques are specified and the optical simulation software GenPro4 is shortly presented.

The optimization of the passivating contacts is described in Chapter 4. This is done using symmetric lifetime samples which are fabricated and analyzed in terms of their passivation properties. At the end of the chapter a conclusion about the optimal processing conditions for a single-junction solar cell is given.

The fabrication of the single-side textured FBC solar cell is examined in Chapter 5. The fabrication process is described and the results of the final device are shown.

Chapter 6 focuses on the improvement of the device fabricated in the previous chapter. Different strategies related to the development of the poly-SiO_x contacts and the device properties are tested and analyzed. The results are also presented in this chapter.

The integration of the c-Si bottom cell with the perovskite top cell in cooperation with TU Eindhoven is described in Chapter 7. Furthermore, the results are examined and possible improvements are discussed.

Lastly, in Chapter 8 and 9 a conclusion is drawn and recommendations for further research are presented, respectively. The conclusion offers a summary of the work and points out important learnings. The recommendation chapter is based on the obtained knowledge as well as the experience from the project and provides guidance for future experiments.

2

Fundamentals of solar cells

In this chapter, the underlying physical mechanisms which are needed to understand the conversion of sunlight into electricity are explained. This is based on the books Solar Energy by Smets et al. (2015) [5], Physics of Solar Cells by Peter Wuerfel (2005) [70] and Semiconductor Physics and Devices by Donald A. Neamen (2012) [71]. First in Section 2.1, the underlying theory is introduced and the working principle of solar cells is explained in Section 2.2. Then, slightly advanced concepts like surface passivation and different contact schemes are examined in Section 2.3 and 2.4. Section 2.5 focuses on high temperature carrier-selective passivating contacts which is the main subject of this thesis. Furthermore, in Section 2.6 the multijunction solar cell approach is presented and tunnel recombination junctions (TRJ) are discussed.

2.1 Semiconductor physics

Solar cells are manufactured from materials which are not insulators nor conductors called semiconductors. Ultimately, the behaviour of the charge carriers inside the material is critical to obtain an efficient solar cell. To understand the electrical properties of all solids including semiconductors, quantum mechanics and solid-state physics is utilized. Generally, the electrical properties of solids are described by "energy-band structures". These energy-bands are specific for every material and help to understand the transport characteristics of charge carriers. Considering a single atom, the electrons have discrete energy levels according to atom orbital theory. If many atoms are brought together they form a crystal. However, due to the Pauli exclusion principle two identical electrons can never occupy the same quantum state. Hence, in a crystal each electron occupies a slightly different energy level which results in an enormous amount of discrete energy states. The difference between those states is so minuscule that they practically form a band of energy states. This is illustrated in Figure 3 for a single atom with two energy levels (E'_1 and E'_2) and for a crystal with many discrete energy levels which form an energy band.

Moreover, one can observe in Figure 3 that the energy-band structure of a solid consists of a valence band and a conduction band. Those two are separated by the energy band gap (E_G) which in a perfect crystal is the zone without allowed energy states, hence the electrons can not occupy this zone. Applying this theory to different materials gives information about the electric transport properties. In a conductor the valence and the conduction band overlap and the electrons can move freely within the solid and can transport charge. On the other hand, an insulator and a semiconductor are characterised by the energy band gap which the electrons need to cross to be able to conduct. Depending on the value of the band

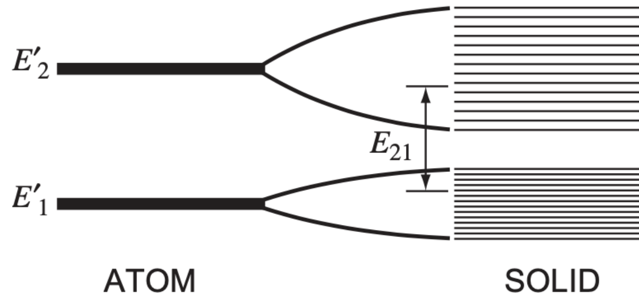


Figure 3: An atom with two discrete energy levels and a solid with many discrete energy levels forming an energy band [3].

gap, the material is called either an insulator or a semiconductor. For semiconductors the illumination or heating of the material is often enough to excite electrons from the valence band into the conduction band. However, for insulators the band gap is usually too big and it would require significant amounts of energy to excite electrons into the conduction band. Therefore, the material is not able to conduct charge. In Figure 4, the simplified band diagrams for insulators, semiconductors and conductors are displayed.

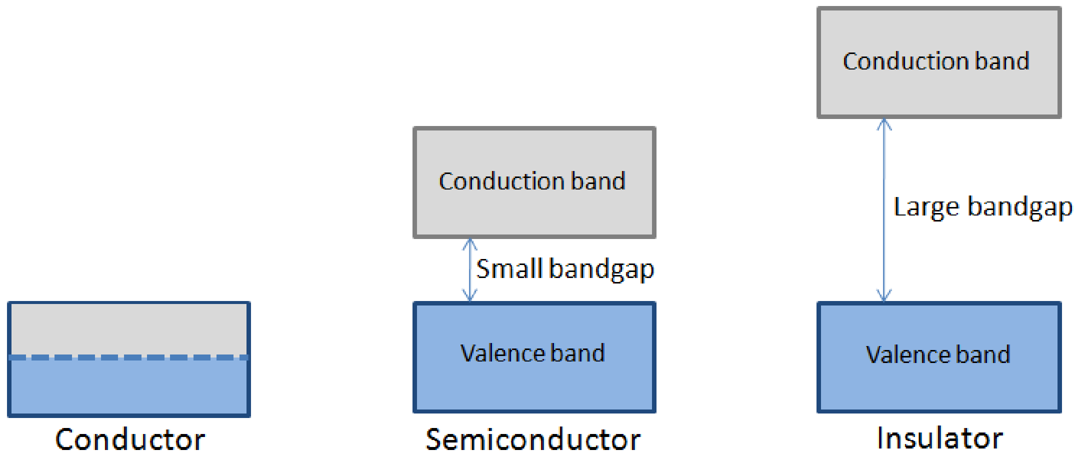


Figure 4: The simplified band structures of a conductor, a semiconductor and an insulator [4].

Once electrons leave the valence band and enter the conduction band they contribute to the electrical conductivity. Furthermore, the leave behind an unoccupied state called *hole* in the valence band which is considered a positively polarized charge carrier due to its associated contribution to the total electrical conductivity. To accurately calculate the concentration of electrons and holes in the material, the density of available energy states and the Fermi-Dirac probability function which computes the probability that an energy level will be occupied by an electron need to be determined. The density of available energy states - also called the density of states (DOS) function - can be derived from the free electron gas model in quantum mechanics. The DOS equation for an electron with mass m in a confined volume is then given by

$$g(E) = \frac{4\pi(2m)^{3/2}}{h^3}\sqrt{E} \tag{1}$$

where h is Planck's constant and E is the energy of the particle. This can be extended to

semiconductors to calculate the density of allowed energy states in the conduction band g_C and the valence band g_V:

$$g_C(E) = \frac{4\pi(2m_e^*)^{3/2}}{h^3}\sqrt{E - E_C} \tag{2}$$

$$g_V(E) = \frac{4\pi(2m_h^*)^{3/2}}{h^3}\sqrt{E - E_V} \tag{3}$$

where m_e^* and m_h^* are the effective mass of electrons and holes, respectively, E_C is the bottom of the conduction band and E_V is the top of the valence band. The effective mass is an analogy to the mass in classical mechanics and not identical for electrons and holes. The DOS function and the Fermi-Dirac distribution function are displayed in Figure 5(a) and Figure 5(b), respectively. The Fermi-Dirac distribution function is derived from statistical mechanics and given by

$$f(E) = \frac{1}{1 + exp(\frac{E-E_F}{k_B T})} \tag{4}$$

where k_B is Boltzmann's constant, T the temperature and E_F the Fermi energy. The Fermi energy is the average energy of electrons in the material and the occupation probability at $E = E_F$ is always 0.5. Next, the electron and hole concentrations as a function of energy can be calculated by multiplying the DOS and the Fermi-Dirac distribution. This can be seen in Figure 5(c).

$$n(E) = g_C(E)f(E) \tag{5}$$

$$p(E) = g_V(E)[1 - f(E)] \tag{6}$$

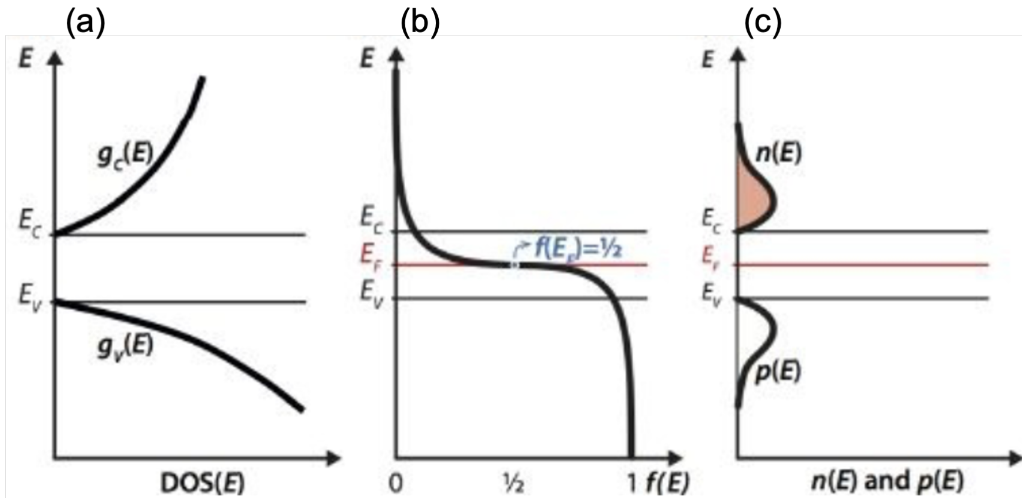


Figure 5: Graph of the density of states (a), the Fermi-Dirac distribution function (b) and the electron and hole concentration (c) depending on the energy level. The density of states and the charge carrier concentrations are zero in the band gap between E_V and E_C [5].

By integrating over the energy, the total number of electrons n and holes p in the con-

duction and the valence band, respectively, can be determined.

$$n = \int_{E_C}^{\infty} n(E)dE = 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{3/2} exp\left[\frac{-(E_C - E_F)}{k_B T}\right] = N_C * exp\left[\frac{-(E_C - E_F)}{k_B T}\right] \quad (7)$$

$$p = \int_{-\infty}^{E_V} p(E)dE = 2\left(\frac{2\pi m_h^* k_B T}{h^2}\right)^{3/2} exp\left[\frac{-(E_F - E_V)}{k_B T}\right] = N_V * exp\left[\frac{-(E_F - E_V)}{k_B T}\right] \quad (8)$$

where N_C and N_V are the effective density of states in the conduction and valence band, respectively. The total number of charge carriers is a fundamental property and enables the determination of other important characteristics of semiconductor devices. The product of n and p is called the intrinsic density n_i and is given by

$$n_i^2 = n * p \quad (9)$$

In an intrinsic semiconductor $n = p$ is always true. Finally, the Fermi level energy E_F can be expressed using Equations 7, 8 and 9.

$$E_F = \frac{1}{2}(E_V + E_C) + \frac{1}{2}k_B T \ln\frac{N_V}{N_C} \quad (10)$$

2.2 The photovoltaic effect - working principle of a solar cell

The working principle of a solar cell is based on a physical phenomenon called photovoltaic effect [5, 71]. The photovoltaic effect is the generation of a voltage at the junction of two different materials when exposed to electromagnetic radiation. In semiconductor physics this junction is known as *pn-junction*. A pn-junction consists of a p-type material and a n-type material which - in a classic crystalline silicon solar cell - are silicon doped with boron atoms and phosphorus atoms, respectively. When connecting the two materials, an electric field forms across the space-charge region at the interface due to the diffusion and recombination of electrons and holes which is shown in Figure 6.

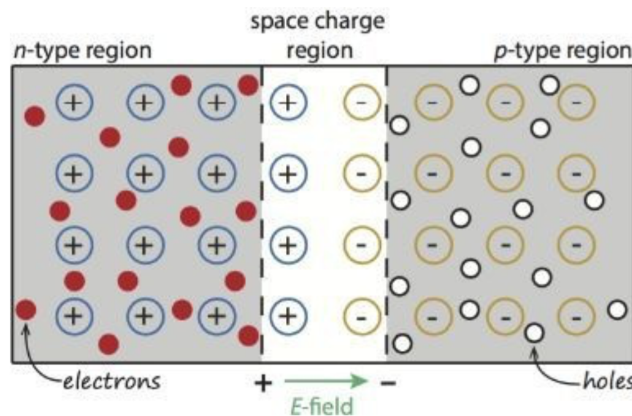


Figure 6: A simple schematic of a pn-junction including the space-charge region and the electric field. [5].

This pn-junction is the building block of a solar cell. To obtain a working solar cell and produce a voltage and a current upon illumination, three important processes must be considered: the generation, separation and collection of charge carriers. These three processes are described in the following section as well as the most important loss mechanisms during each process. The working principle is also schematically presented in Figure 7.

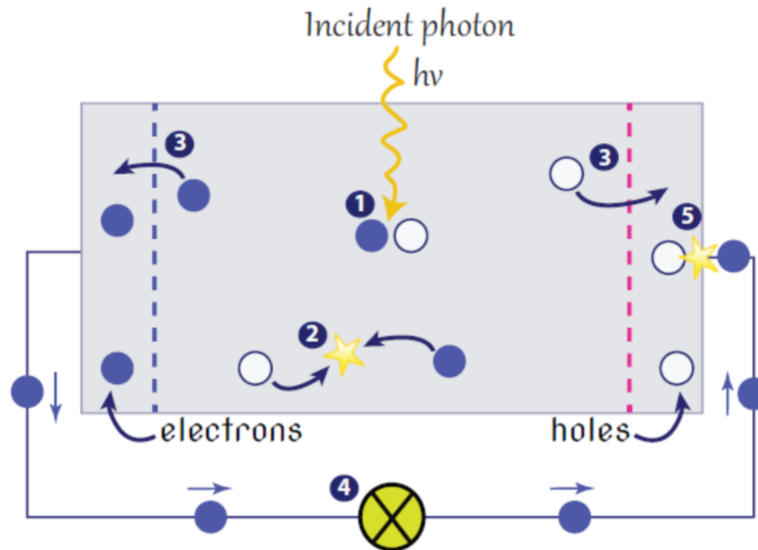


Figure 7: The working principle of a solar cell. First, photons are absorbed and generate electron-hole pairs (1). Recombination of charge carriers (2) should be minimized and separation and collection at the metal contacts (3) has to be promoted. Finally, the electrons move through the external current, do work (4) and recombine with the holes (5). [6].

2.2.1 Generation of charge carriers

Once the pn-junction is exposed to electromagnetic radiation - for example sunlight - the materials absorbs the incoming photons which results in the generation of electron-hole pairs and the splitting of the Fermi level into two quasi-Fermi levels. The difference between the two quasi-Fermi levels is used to calculate the implied open-circuit voltage (iV_{OC}) in solar cell precursors. To ensure an efficient absorption of photons the optical properties of the different layers of the solar cell have to be optimised. This is done by reducing reflection of light at interfaces and minimising the so-called parasitic absorption, which refers to photon absorption in other layers of the solar cell, since those photons do not contribute to the generated voltage. As explained in the Section 2.1, another important parameter is the band gap energy of the material. That is an intrinsic material property which represents the minimal energy necessary to excite an electron from the valence band to the conduction band and therefore create an electron-hole pair. Photons which possess an energy below this threshold will not be absorbed and consequently also do not contribute to the generated electricity. Photons with an energy equal or greater than the band gap energy can be absorbed. However, the energy difference between the band gap energy and the energy of the photon is lost as thermalization energy. Those two loss mechanisms - the non-absorption and thermalization losses - are referred to as spectral mismatch losses and are responsible for about half of the incident solar energy being lost.

2.2.2 Separation of charge carriers

Once the electron-hole pair has been created, the two charge carriers have to be separated to prohibit recombination. The recombination has a strong effect on the solar cell voltage. A high recombination rate reduces the generated voltage and hence the efficiency of the solar cell. Different kinds of recombination mechanisms exist which can be categorised into radiative/non-radiative and into bulk/surface recombination mechanisms. Those different mechanisms are shortly described and illustrated in Figure 8.

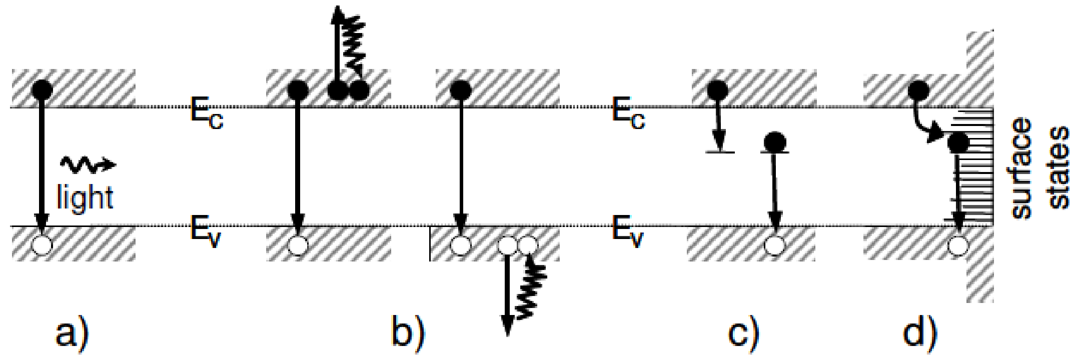


Figure 8: The four recombination mechanisms: a) radiative, b) Auger, c) SRH and d) surface recombination [7].

Radiative recombination

The basic recombination mechanism is the **radiative recombination**. The excited electron falls back to the valence band from its meta-stable state in the conduction band and recombines with a hole. The excess energy is emitted as a photon, hence radiative. It is most common in direct band gap semiconductors.

Non-radiative recombination

On the other hand, non-radiative recombination mechanisms release the energy through lattice vibrations, so-called phonon modes, and the energy is converted to heat. Here we can distinguish three different mechanisms. First, **Auger recombination** is a three-particle process. The excited electron falls back to the valence band and does not emit a photon but transfers its energy to another electron (hole) which is excited higher (lower) into the conduction (valence) band. Finally, this third particle returns to its low-energy state and the energy is transferred to phonon modes. This mechanisms has a greater importance at high doping levels since more particles are present and the likelihood of a three-particles process increases. Second, **Shockley-Read-Hall (SRH) recombination** is a trap-assisted mechanism. Hereby, a defect in the lattice - like an impurity atom - promotes the recombination by acting as a trap between the valence and the conduction band. This mechanism is dominant in the bulk of indirect band gap semiconductors at most conditions. Radiative, Auger and SRH recombination mechanisms are also called bulk recombination mechanisms since they mainly take part within the bulk of the material. The last non-radiative recombination mechanism is **surface recombination**. It is similar to the SRH recombination since it is also facilitated

by trap states between the valence and the conduction band. However, the trap density is substantially higher at surfaces (and interfaces) which results in many so-called dangling bonds. Dangling bonds are interface defects and aid recombination of electrons and holes. Surface recombination can be the dominant recombination mechanism in crystalline silicon solar cells and significantly reduce the efficiency of the cell. In Figure 9, it can be observed that SRH recombination is the dominating effect regarding the minority carrier lifetime for silicon solar cells. Only at high injection level does Auger recombination play an important role. The two main methods to reduce the surface recombination are chemical passivation and field-effect passivation. The two techniques are discussed in more detail in Section 2.3.

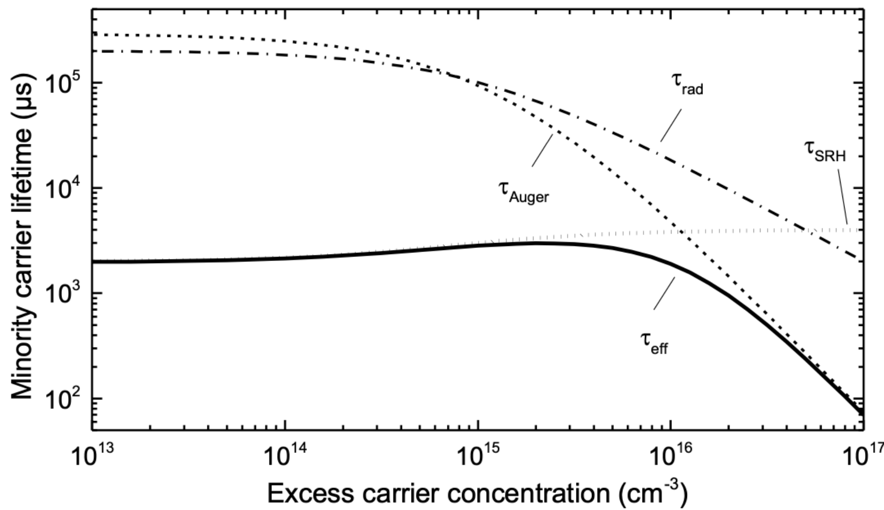


Figure 9: The influence of the different recombination mechanisms on the minority charge carrier lifetime [8].

2.2.3 Collection of charge carriers

After the generation and the separation, the last step is to collect the charge carriers and enable the electrons to flow through the external circuit where they can do work and recombine with the holes on the other side. This step involves the actual conversion from chemical to electrical energy. The extraction of charge carriers is accomplished by a metal layer which is highly conductive and facilitates an efficient carrier collection. In the case of high temperature carrier selective passivating contacts, the doped polycrystalline silicon (poly-Si) contacts are usually very thin to reduce parasitic absorption they also exhibit high sheet resistance which increases the majority carrier recombination. In order to reduce the transport losses, a transparent conductive oxide (TCO) is often used as an additional layer between the doped layer and the metal. The TCO should exhibit multiple qualities like high transparency, low sheet resistance, low contact resistance with the bordering layers, appropriate refractive index matching and the processing should influence the quality of the solar cell as little as possible [72]. Losses can also occur due to a low shunt resistance which results in leakage currents.

2.3 Surface passivation

As already shortly discussed in Section 2.2.2, surface recombination strongly influences the performance of the solar cell. Hence, it is necessary to reduce the surface recombination velocity - a measure of the recombination rate - as much as possible to fabricate an efficient solar cell [73]. The importance of surface recombination also increases due to the development of thinner wafers [74]. There are two main techniques to achieve this: chemical passivation and field-effect passivation [75].

2.3.1 Chemical passivation

Chemical passivation is performed to reduce the surface defects which act as trap-states between the valence and conduction band and promote recombination (Figure 10). The dangling bonds at the surface are saturated by depositing a passivation layer like silicon oxide (SiO_x) or intrinsic amorphous silicon (a-Si) on the silicon absorber layer. Moreover, hydrogenation can be used to further decrease the surface recombination velocity by passivating the dangling bonds with hydrogen atoms. A more detailed description of the SiO_x passivating layer which is utilised in high temperature CSPCs is given in Section 2.5.1.

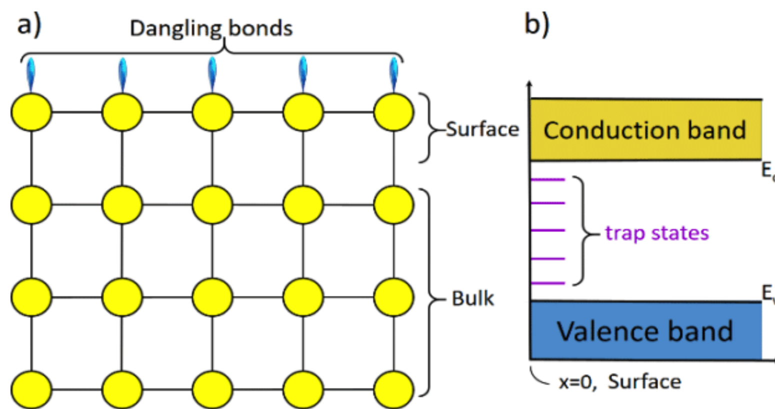


Figure 10: A representation of the dangling bonds at the surface (a) and the trap states in the band gap which promote recombination (b) [6].

2.3.2 Field effect passivation

The second method to decrease the surface recombination velocity is called field-effect passivation. This technique takes advantage of an electric field formed either by a charged layer like SiN_x or a highly-doped region which acts like another pn-junction (back surface field) [73]. Both methods form an electric field, reduce the minority carrier concentration at the surface and promote the collection of the majority carriers (Figure 11). However, this also reduces the diffusion length and therefore, the life time of the minority carriers in the emitter layer which has to be taken into account.

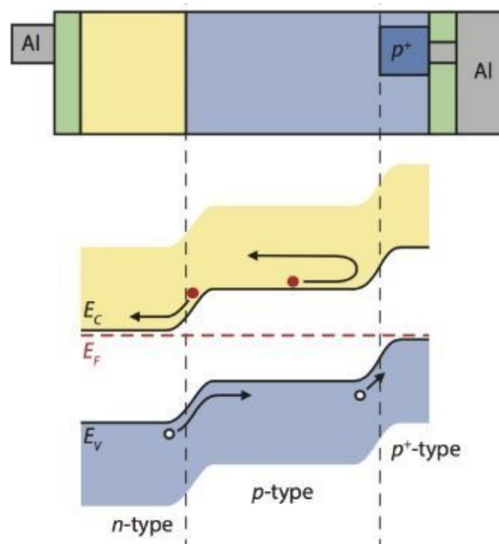


Figure 11: A p-type solar cell with a highly doped p+ region at the back contact (back-surface field) which selectively collects the holes and repels the electrons. Its band diagram shows the effect of the p+ region [5].

2.4 Contact schemes

The contact between the crystalline silicon and the metal electrodes is of uttermost importance. To fabricate efficient solar cells, a high passivation level at the interface needs to be achieved to minimize recombination and at the same time, the charge carriers have to be efficiently extracted. This is one of the main challenges to reach the theoretical efficiency limit of single-junction crystalline silicon solar cells.

2.4.1 Current contact schemes

The classical methods to accomplish these goals are by reducing the contact area between the absorber material and the metallic contacts and by utilizing pn-junctions at the interfaces [9, 10]. One of the most common contact schemes is the aluminium back surface field (Al-BSF) as shown in Figure 12a. This design includes a heavily doped layer - the back surface field - between the absorber and the back contact which acts as pn-junction and reduces the minority carrier concentration near the interface and therefore the surface recombination velocity. However, introducing heavily doped regions also increases the intrinsic charge carrier recombination and limits the efficiency [76]. Another group of contact schemes are the PERC, PERL and PERT contacts. Those abbreviations stand for passivated emitter and rear cell, passivated emitter and rear locally-diffused and passivated emitter and rear totally-diffused, respectively [9]. They all have the passivation of the rear contact in common by minimizing the contact between the absorber and the back contact to local regions. Furthermore, the PERL design includes heavily doped regions right above the contact which act as a localized pn-junction (Figure 12b). In contrast, the PERT design does not include a localized back surface fields but has a heavily doped layer which covers the entire area. Those two designs - the Al-BSF and the PERX group - are currently the industry standard and applied in most crystalline silicon solar cells on the market [10, 77].

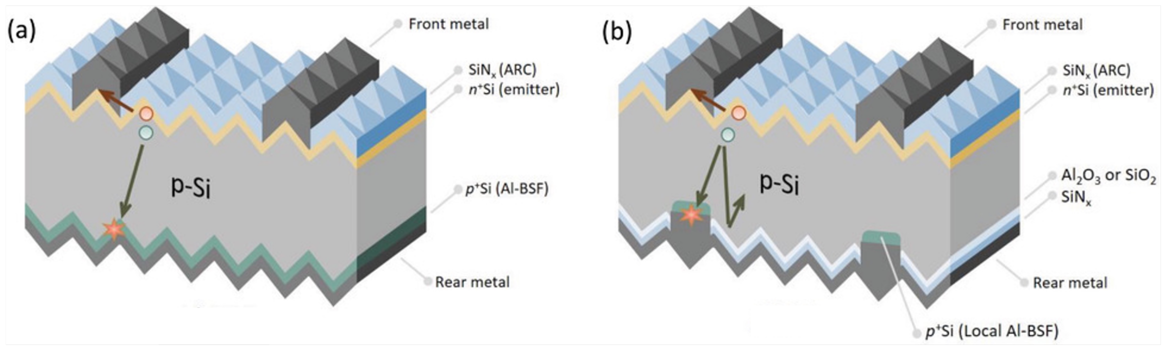


Figure 12: Schematics of design of the Al-BSF (a) and the PERL (b) solar cells [9]

2.4.2 Carrier selective passivating contacts

To further improve the efficiency of solar cells, new contact schemes are researched. A promising approach are carrier-selective passivating contacts (CSPC) [10, 41, 75, 76, 77, 78]. This method does not exhibit direct contact between the silicon absorber and the contact but involves a passivating layer which minimizes surface defects. Hence, the contacts are spatially separated from the absorber. A well-designed CSPC should fulfill multiple criteria like a high passivation quality, a low contact resistivity and a good carrier selectivity. This refers to preventing the unwanted carrier from being collected and at the same time extracting the desired carrier. It is measured as the ratio of resistance of the majority and the minority carriers at the contact [75]. Moreover, the passivation quality can be determined by the recombination current density J_0 [79]. A better passivation results in a lower amount of defects and accordingly in a lower recombination current density. Also, optical properties like reflection and parasitic absorption have to be taken into account to determine the overall performance of a CSPC.

The HIT (heterojunction with intrinsic thin layer) contact scheme is one of the most investigated cells with CSPCs [80]. It consists of a thin intrinsic a-Si passivation layer. Subsequently, a doped a-Si layer is applied to collect the charge carriers as shown in Figure 13 (a). However, there are some drawbacks to this design like the low thermal stability which does not comply with many industrial high temperature processes, the light-induced Staebler-Wronski degradation which leads to efficiency losses or parasitic absorption due to the comparable band gap of a-Si and crystalline silicon (c-Si) [81].

Another approach is the use of high temperature CSPCs like tunneling oxide passivating contacts (TOPCon) and polycrystalline silicon on oxide (POLO) contact designs [41, 75]. A schematic of the POLO architecture is presented in Figure 13 (b). It is based on an ultra-thin SiO_2 passivation layer capped by a poly-Si or polycrystalline silicon oxide (poly-SiO_x) carrier separation layer. The main purpose of the silicon oxide layer is the chemical passivation of the c-Si/poly-Si interface by lowering the defect density and reducing charge carrier recombination. In this thesis the TOPCon/POLO architecture is utilised with poly-SiO_x contacts. Thus, this design will be discussed in more detail in the next section.

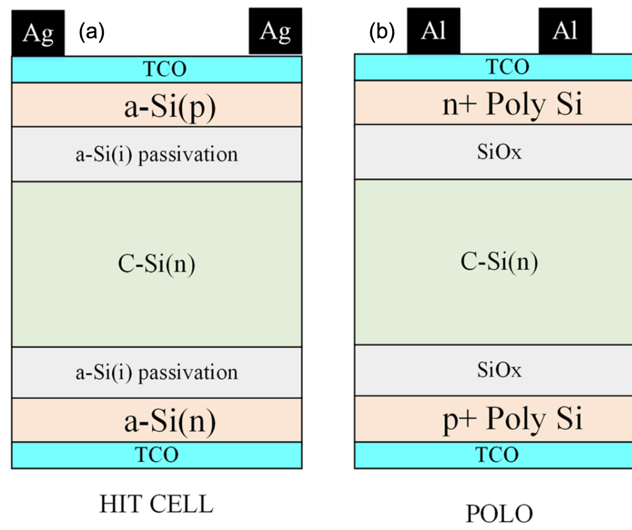


Figure 13: Architecture of the HIT (a) and the POLO (b) solar cells. The thickness of the different layers is not to scale [10].

2.5 POLO - High temperature carrier selective passivating contacts

As already mentioned, the exact structure of the POLO architecture is shown in Figure 13 (b). However, be aware that the layer thickness is not to scale in the illustration. The n-type c-Si absorber is in the range of hundreds of µm while the SiO_x passivation layer is usually only about 1-2 nm. The contacts and the TCO layer are typically in the ten to hundred nanometer range. In this section the different layers and their interaction will be examined.

2.5.1 SiO_x passivation layer

The SiO_x passivating layer has multiple purposes. The main function is the surface passivation of the interface. In comparison to the classic contact schemes, the passivating contacts strongly reduce the recombination current density and hence increases the minority carrier lifetime. This enables the fabrication of devices with very high open-circuit voltages [10, 78]. However, silicon oxide is an insulating material and the implementation of such a layer reduces the electrical conductivity. Therefore, the question arises how the transport of the charge carriers through the silicon oxide layer can be ensured. According to literature, two different concepts coexist which explain the transport of charge carriers through the passivating layer [82, 83]. First, quantum tunneling through the silicon oxide is possible if the layer is thin enough [84]. The tunneling probability P is proportional to the thickness of the oxide as shown in equation 11, where d_{ox} is the thickness of the silicon oxide film, m is the mass of the tunneling particle, Φ is the energy barrier height of the film and h the Planck constant.

$$P(d_{ox}) \propto \exp(-d_{ox} * \sqrt{\frac{8 * \pi^2 * m * \phi}{h^2}}) \qquad (11)$$

Hence, the thickness has to be approximately 1-2 nm to ensure efficient conductivity. Moreover, the energy barrier is higher for holes than it is for electrons at the n-type contact

which also enhances the selectivity of the layer. This can also be observed in Figure 14 where the energy band diagram of the n-type contact of a TOPCon solar cell is depicted.

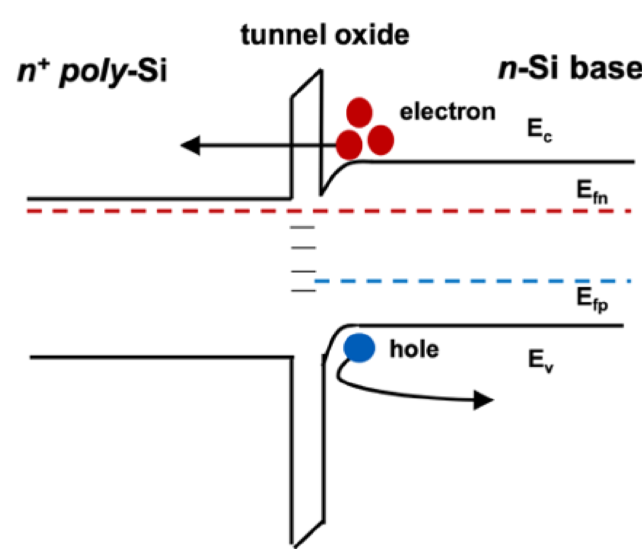


Figure 14: Energy band diagram of a n-doped poly-Si/c-Si interface of a TOPCon solar cell. The band offsets for the holes and electrons are 3.1 and 4.8 eV, respectively [10].

The second method of charge carrier transport is through small pinholes in the tunneling layer [83]. During the production process, the solar cell is annealed at high temperatures (800-1000 °C). This can lead to the partial breakup of the thin SiO_x layer and the formation of minuscule pinholes. At those pinholes there is direct contact between the c-Si absorber and the poly-SiO_x layer without the insulating effect of the tunneling layer. Hence, charge can be transported relatively easily across the barrier. However, too many pinholes will negatively affect the efficiency of the solar cell due to the increase of defects and since the tunneling layer also acts as a barrier for the diffusion of dopants from the doped poly-SiO_x to the c-Si absorber. This dopant diffusion will lower the field effect passivation of the interface [85]. Hence, the thermal stability of the thin film has to be sufficient to achieve an optimal trade-off [86, 87].

Other important properties of the tunneling layer are directly related to the topics which were just introduced like charge transport and interface passivation. The uniformity is especially important with such a thin layer since small deviations can already have a considerable effect. The density and chemical composition also play a big role since they will strongly effect the thermal stability of the layer. Lastly, the optical properties of the tunneling layer will effect the solar cell performance. Higher absorption will lower the efficiency of the device. However, since the thickness of the layer is very thin compared to the c-Si absorber and SiO_x is a very transparent material at the relevant wavelength range, this only plays a minor role and can be neglected.

Different deposition methods can be used to apply the ultra-thin SiO_x layer. Dry thermal oxidation, wet-chemical oxidation, ozone oxidation and plasma-enhanced chemical vapor deposition (PECVD) are common methods for the layer deposition. The various deposition methods result in slightly different properties which also influences the solar cell. Dry thermal oxidation distinguishes two types of oxidation, one at higher temperatures (900-

1100 °C) and the other one at medium temperatures (500-700 °C) with higher oxygen gas pressure [88]. Thermal oxidation of silicon and the Si/SiO_2 interface have been extensively studied [89, 90]. The growth rate mainly depends on the diffusion of oxygen into the silicon layer and is proportional to the square root of the time. This process is described by the Deal-Grove model [89] which has been slightly modified for ultra-thin SiO_x films [91, 92]. The original Deal-Grove model only takes the diffusion limited regime into account which is based on the observation that the atomic oxygen has to diffuse through the already deposited film before it can react with the silicon substrate. The modified model by Massoud et al. also considers the linear growth regime right at the start of the reaction which is the relevant thickness range for the application in TOPCon solar cells. Those two different regimes can be observed in Figure 15.

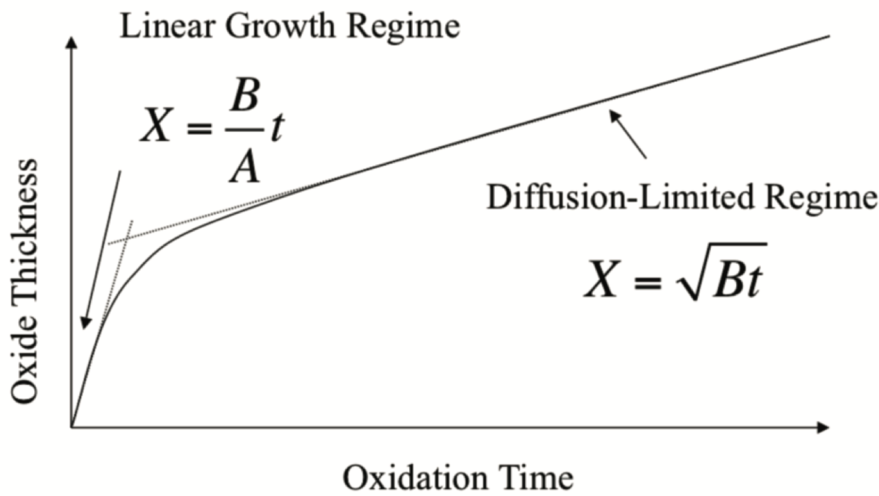


Figure 15: The two regimes for the oxide growth. For an ultra-thin SiO_x thickness the linear growth regime is valid, for thicker layers the oxide growth is limited by the diffusion of oxygen through the SiO_x layer [11].

A second approach to oxidize the surface of a silicon wafer is by using wet-chemical oxidation [84]. This is done by submerging the substrate into an acid media, sometimes at elevated temperatures. Various different solutions can be used, examples are nitric acid (HNO_3), hydrochloric acid (HCl), sulfuric acid (H_2SO_4), mixtures of acids or solutions with hydrogen peroxide (i.e. piranha). Nitric acid oxidation of silicon (NAOS) is one of the most common wet-chemical paths and already well-established in the microelectronics industry [88]. The HNO_3 solution follows the reaction shown in equation 12. Atomic oxidation is formed and reacts with the silicon surface to form SiO_x. Different concentrations and temperatures lead to varying growth rates of the layer and can influence the properties. The growth mechanisms is similar to the one in dry thermal oxidation.

$$2HNO_3 \longrightarrow 2NO + H_2O + 3O \tag{12}$$

Another method to grow thin SiO_x films is by using ozone (O_3) [93]. This process is more environmentally friendly than the usage of acid media in the wet-chemical approach. It utilizes ozone gas which is very reactive and can easily oxidize a silicon surface. There are two different methods: First, photo-oxidation (UV/O_3) is achieved by the excitation of

ozone gas using photons according to equation 13 [94].

$$O_3 + hv \longrightarrow O_2 + O \tag{13}$$

The atomic oxygen can then oxidise the silicon wafer. This can be done at relatively low temperatures (below 300 °C) in a dry environment. Compared to the photo-oxidation of O_2 it requires low-energy photons which protects the substrate from high-energy particles which accordingly leads to a lower defect formation. Second, wet de-ionized ozone oxidation (DIO_3) is also an option for the film growth [93, 95]. For this approach, ozone is dissolved in ultra-pure DI-water and the silicon wafer is submerged in the solution. The ozone then oxidizes the surface and forms the SiO_x layer. The growth rate depends on the ozone concentration but like the thermal oxidation and the wet-chemical oxidation, the thickness is self-limiting due to its dependence on the diffusion of oxygen into the substrate [96].

Another approach for the deposition of the tunneling oxide is plasma-enhanced chemical vapor deposition (PECVD). It is used in the fabrication of many films like optical coatings, dielectrics as well as in the semiconductor industry. Like the name suggests the chemical reaction is initiated by a plasma. This has the advantage that the deposition can take place at lower temperatures around 200-350 °C. Moreover, it can be efficiently integrated into the production process since the doped contacts - which are deposited after the SiO_x - are often also deposited using PECVD. The plasma is usually created via electrical energy [97].

The most important properties of the SiO_x are the stoichiometry and density which influences the thermal stability of the layer and the interface defects density which is important for the recombination and minority charge carrier lifetime. The stoichiometry of the thin SiO_x film is usually analysed by X-ray photoelectron spectroscopy (XPS). In XPS, the surface of a sample is irradiated with X-ray beams and the kinetic energy and number of ejected electrons is measured. From this information, the elemental composition and the oxidation state can be calculated. For SiO_x, the different oxidation states are Si^0 which are bulk silicon bonds, suboxide bonds (Si^{1+}, Si^{2+}, Si^{3+}) which are non-stoichiometric silicon oxide bonds and finally Si^{4+} bonds which describe stoichiometric silicon oxide bonds and are desirable for a dense and thermally stable SiO_x thin film. Mandal et al. [12] compared thermal oxidation, wet-chemical oxidation and the PECVD approach while Moldovan et al. [96] compared the two ozone oxidation methods with the wet-chemical approach. In the first comparison, it is shown that thermal oxidation method leads to the best stoichiometry with a Si^{4+} contribution to the total amount of bonds of 73.3% and 87.9% for p-type and n-type doped contacts respectively while for the wet-chemical oxidation and the PECVD oxidation only result in 40-70% Si^{4+} bonds [12]. Comparing the wet-chemical approach with the UV/O_3 and the DiO_3 method, it is observed that the wet-chemical approach results in a poorer stoichiometry while the two ozone oxidation methods lead to a similar sub-oxide ratio [96]. In conclusion, thermal oxidation results in the silicon oxide with the highest stoichiometry which might result in a higher thermal stability.

The interface defect density is another important parameter. It can be determined us-

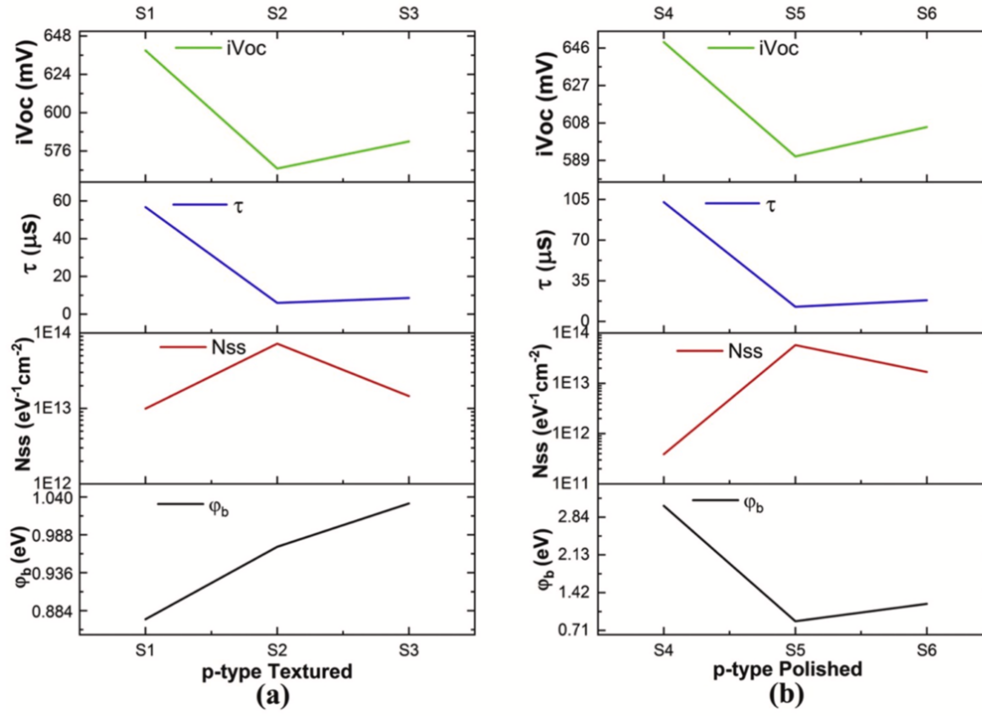


Figure 16: Change of open-circuit voltage, lifetime, trap state density and energy barrier height of p-type textured and polished samples with different SiO_x layers (S1 and S4 deposited via thermal oxidation, S2 and S5 is deposited via wet-chemical oxidation, S3 and S6 deposited via PECVD) [12].

ing Capacitance-Voltage (CV) measurements. A metal-semiconductor junction - with the thin SiO_x layer in-between acting like a capacitor - is created to form a depletion region at the interface which is empty of mobile charge carriers and only contains ionized atoms and electrically active defects. By varying the voltage and measuring the capacitance, certain properties of the depletion region like doping profile and defect density can be extracted. The defect density was lowest for all samples (p and n-type, polished and textured) for the thermal oxidation method compared to the wet-chemical and the PECVD approach [12]. Only, for the textured p-type sample the PECVD method achieved a similar result as shown in Figure 16. The lowest interface state density was measured for the n-type polished sample with $2*10^{11}$ states/(eV*cm^2). This is directly related to the lifetime of the minority charge carriers and the iV_{OC}. However, the relationship between those quantities is not linear due to its dependence on the capture cross-section of the exact defect. Also, in a study by Angermann et al. [95], the defect density of a sample prepared by thermal oxidation is lower than for samples prepared with wet-ozone oxidation. From iV_{OC} measurements it can be seen that the interface quality is especially important for textured samples. For polished wafers, the iV_{OC} does not vary strongly for ozone or wet-chemical oxidation while for a textured interface the wet-chemical approach exhibits a significantly lower iV_{OC} [96].

2.5.2 Doped poly-Si/poly-SiO_x contact

The charge carrier selectivity can mainly be attributed to the doped contacts. Those induce the necessary band bending and electric fields which leads to the selective extraction of the desired charge carriers [77, 81]. This contact scheme also exhibits high temperature stability

and hence, is compatible with the current industry processing standard [50, 81]. Its processing route is similar to the PERC production standard and can be upgraded relatively cheaply which makes it economically competitive [98]. The drawback of this design are the parasitic absorption and the free-carrier absorption (FCA) [99, 100]. Due to the similar band gap of c-Si and poly-Si, relatively high absorption loses are expected [41]. Also, to achieve a good carrier selectivity the poly-Si layers are usually heavily doped which results in FCA [101, 102]. Those loses can be reduced with poly-SiO_x emitters. Alloying the poly-Si layer with oxygen changes the optical and electrical properties of the material which can potentially lead to lower absorption losses due to their larger band gap. This can also improve the band bending and the carrier selectivity [102, 103].

2.5.3 Transparent conductive oxide

The incorporation of a TCO between the poly-SiO_x contacts and the metal electrodes has multiple purposes. There are optical and electrical arguments as well as process specific requirements like the selection of an appropriate deposition method [72]. The most commonly used TCOs are degenerative doped metal oxides like indium tin oxide (ITO). They exhibit a high carrier mobility, good optical transparency, relatively simple deposition methods and mechanical flexibility. The doping concentration and the oxidation states of the dopants plays a vital role in the performance of those metal oxides since both electrical and optical properties depend on it [72]. In this thesis ITO and indium tungsten oxide (IWO) are utilised. At the front side the TCO works as an anti-reflection coating (ARC) to improve light in-coupling. ARCs are based on the principle of destructive interference. The electromagnetic waves reflected at the air/TCO and TCO/poly-SiO_x interfaces are reflected in antiphase. Hence, the two waves cancel each other out and the result is zero net-reflected energy. The optimal thickness d of the TCO layer can easily be calculated using Equation 14 where λ is the desired wavelength (i.e. 600 nm for the maxima of the AM1.5 spectrum) and n the refractive index of the TCO (i.e about 2 for indium tin oxide). This results in an optimal layer thickness for an indium tin oxide coating of about 75 nm.

$$d = \frac{\lambda}{4 * n} \tag{14}$$

At the rear side the TCO also has an optical function. The TCO behaves as a back reflector to minimize absorption losses in the metal rear contact. In literature layer thicknesses of about 150 nm are standard [104]. Parasitic free carrier absorption (FCA) losses in both TCO layers - front and rear - can not be avoided. Of course, this could be decreased by reducing the layer thickness. However, this would also undermine their functions as a ARC and back reflector. Furthermore, TCOs also perform important electrical purposes. The poly-SiO_x layers have a relatively low lateral conductivity. This would lead to high losses during the transport to the metal fingers at the front side of the solar cell. Thus, the TCO has to exhibit a low sheet resistance to allow lateral carrier transport. There is a trade-off between high carrier mobility and scattering centers since more doping increases the carrier density but

simultaneously also increases the chance of scattering events [105]. Furthermore, higher carrier densities also result in a higher FCA. Hence, there is a second trade-off between optical and electrical properties of TCOs [106].

Another property which can significantly alter the device performance is the contact resistivity at the interfaces. The introduction of a TCO interlayer reduces the effect of Fermi level pinning which can otherwise increase the electrical resistance at the semiconductor/metal interface [78, 107]. Metal-induced gap states (MIGS) and interface dipoles which are not considered in the Schottky-Mott theory introduce a counterproductive band bending which results in a considerable Schottky barrier [108]. The incorporation of a TCO reduces this effect of Fermi level pinning and improves the contact resistivity.

2.6 Multi-junction solar cells

The maximum theoretical efficiency of single-junction c-Si solar cells is estimated to be about 29.4% [39]. This maximum is called the intrinsic Shockley-Queisser (SQ) limit. The main cause of this inherent efficiency limit are the spectral mismatch losses. The spectral mismatch losses result from two different phenomena: non-absorption losses and thermalization losses. Both of those loss mechanisms are related to the mismatch between the energy band gap of the solar cell absorber material and the energy of the incoming light. If the energy of the incoming photon exceeds the energy band gap, the electron is excited deep into the conduction band after which it relaxes back to the edge of the conduction band while the energy difference is lost as heat. This loss mechanism is termed thermalization loss because the excess energy is converted into heat. On the other hand, if the energy of the incoming photon is lower than the energy band gap, the photon can not be absorbed. Hence, it is named non-absorption loss. Both mechanisms are displayed in Figure 17.

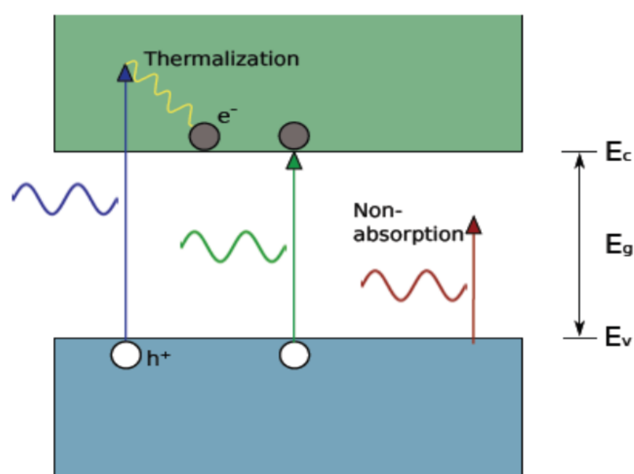


Figure 17: A schematic of the photons with different energies entering the solar cell. In blue, a photon with an energy greater than the band gap is absorbed and energy is lost due to thermalization (yellow). The photon in red does not carry enough energy to create an electron-hole pair and is not absorbed. The photon in green has exactly the same energy as the band gap and hence can be absorbed without any losses. [13].

The most promising concept to significantly lower the spectral mismatch losses and overcome the SQ limit are multijunction devices [109]. Multijunction devices combine two or

more solar cells with different band gaps. Therefore, the subcells can utilize different parts of the light spectrum more efficiently and reduce the spectral mismatch losses. The simplest design is the so-called tandem solar cell which consists of a top cell and a bottom cell. The top cell has a larger band gap and absorbs the high energy photons. The photons with a lower energy are not absorbed by the top cell and reach the bottom cell where they generate an electron-hole pair. There are different design methods for tandem solar cells [14, 110]. The two-terminal (2T) tandem device connects both subcells in series by stacking them monolithically as shown in Figure 18(b). This requires a interconnection layer and current matching conditions between the two subcells to achieve maximum performance. Due to the necessity of current matching, changes in light intensity will also lead to significant variations in the performance of the device [14]. Another option to combine different subcells are four-terminal (4T) tandem devices. Here, the two subcells are not electrically connected, but only optically as shown in Figure 18(a). This is advantageous from a processing point of view since the cells can be manufactured separately but it requires more materials and increases the costs. Recently, there has also been research into three-terminal (3T) tandem devices [111]. 3T tandem devices combine some of the advantages of the 2T and the 4T tandem devices but also add another level of complexity to the manufacturing process.

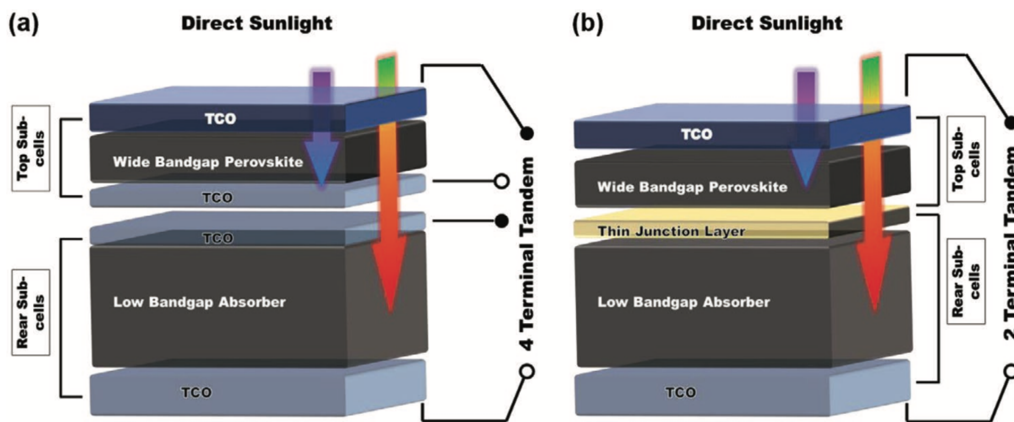


Figure 18: Design architecture of a 4T (a) and a 2T (b) tandem device [14].

In this work, the focus lies on monolithic 2T tandem devices with a perovskite solar cell as the top cell and a c-Si bottom cell based on poly-SiO_x. Since the two subcells are connected in series, Kirchhoff's law applies and the voltages of the two subcells add up while the current is limited by the subcell with the lower current. Hence, current matching of the two cells is required to optimize the overall performance of the tandem device. Furthermore, the interconnection layer - also called tunnel recombination junction (TRJ) - plays an important role in the operation of the tandem device.

2.6.1 Tunnel recombination junction

The TRJ is an essential part of a monolithic multijunction solar cell. In the case of a tandem solar cell, two individual cells with same polarity are stacked on top of each other in se-

ries. Thus, at the top and the bottom of the device the majority carriers have to be collected while at the interface of the two subcells, the charge carriers need to recombine to guarantee an efficient solar cell [62]. Therefore, the main task of the interface layer is to ensure efficient recombination of the majority carriers. If efficient recombination of charge carriers is not achieved, the built-in voltage is reduced and the efficiency of the device is negatively affected. To achieve this it requires a low lateral conductivity and a sufficient vertical conductivity. Furthermore, the contact between the layers has to be of an ohmic nature with a non-rectifying behaviour to avoid barriers for the charge carriers to enter the layer [112]. Other important criteria for a TRJ are a high optical transparency and low reflectance - especially in the higher wavelength range - to avoid parasitic absorption. Since the bottom cell is below the TRJ it would strongly decrease the efficiency of the device if the interconnection layer absorbs significant parts of the incoming light in the near-infrared range (NIR). Also, a good processing compatibility with the two subcells is advantageous [14].

The most common intermediate layer in 2T solar cells are TCOs like ITO. As presented in Table 1, the majority of perovskite/c-Si tandem cells utilize ITO as a TRJ. ITO is often also used as the electrode in c-Si solar cells and therefore, there is sufficient experience and good compatibility with the whole process. Generally, this is an effective approach. However, it also suffers from numerous drawbacks. First, parasitic absorption at higher wavelengths presents an issue [113]. Second, the poor refractive index matching between the bottom cell and the ITO results in high reflectance at the interface [114]. The band diagrams of the interface of the top and the bottom cell without an ITO and with an ITO as the TRJ are shown in Figure 19(a) and (b), respectively. A more detailed overview of the tunneling region is given in Figure 19(c).

Another option which is implemented regularly are TRJs based on p/n junctions made from hydrogenated nano-crystalline silicon (nc-Si:H). Even though they exhibit a higher absorption than ITO in the short wavelength range, they can reduce the parasitic absorption in the relevant NIR [62, 115]. Furthermore, due to the similarity in refractive index with c-Si the reflectance is strongly reduced. Lastly, nc-Si:H also exhibits a low lateral conductivity while being conductive enough to facilitate the vertical transport of charge carriers across the TRJ [116].

A third option is to not include an additional layer but to utilize the bottom layer of the perovskite as a quasi recombination junction. Materials like TiO_2 and SnO_2 have been implemented to act as a electron transport layer and a recombination layer simultaneously [47, 54].

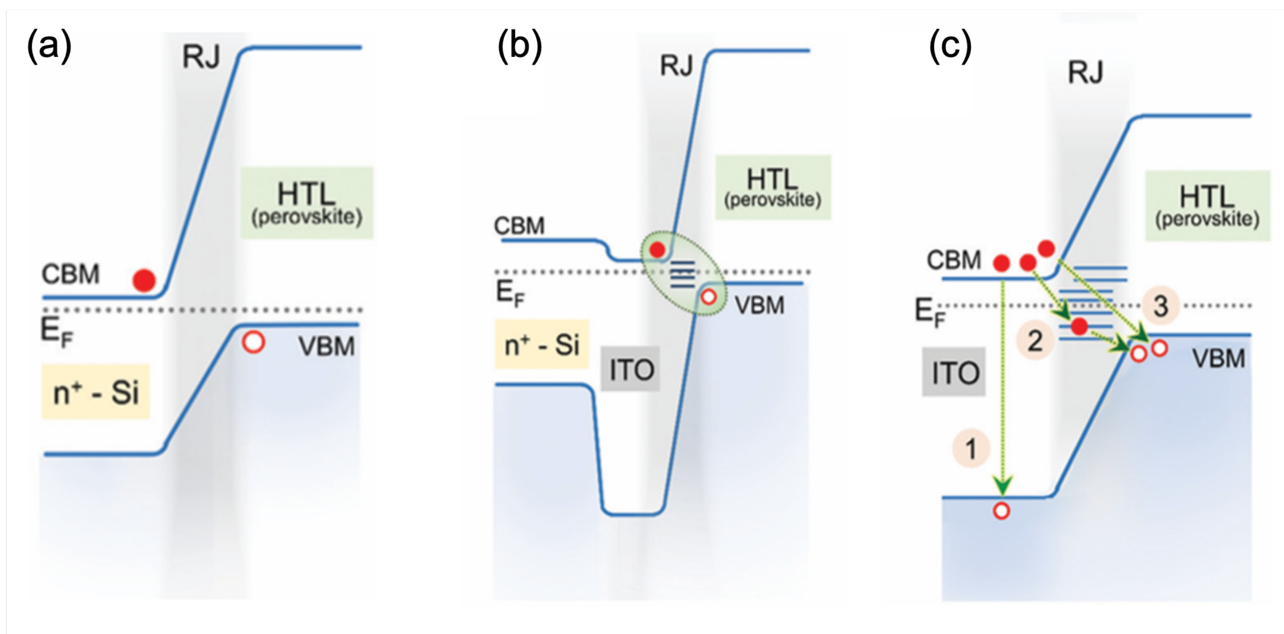


Figure 19: The band diagrams of the interface between the perovskite top cell and the silicon bottom cell without an intermediate layer (a) and with an ITO as the TRJ (b). In (c), the tunneling region is zoomed in and one can observe different recombination mechanisms; local tunneling (1), trap-assisted tunneling (2) or direct tunneling (3). [15].

3

Experimentation

In this chapter the different fabrication and characterization methods are introduced. First, in Section 3.1 the individual fabrication steps of the high-temperature carrier-selective passivating contact solar cell are discussed. Those steps were carried out in the cleanroom facilities of the Else Kooi Laboratory and the Kavli Nanolab at TU Delft. Second, the technologies for the analysis and characterization are explained in more detail in Section 3.2. Those measurements were performed at the Electrical Sustainable Power Laboratory at TU Delft. Lastly, a short introduction to the optical simulation software GenPro4 developed at the PVMD group at TU Delft is given in Section 3.3.

3.1 Fabrication

The fabrication of the solar cell includes numerous process steps. A detailed overview of every step is given below. As a substrate, n-type float zone $< 100 >$ oriented silicon wafers with a diameter of 100 mm, a thickness of 280 µm (+/- 20 µm) and a resistivity of 1-5 Ωcm are used. N-type wafers have multiple advantages over p-type which is the current industry standard. First, p-type wafers suffer from light-induced degradation (LID) due to the formation of metastable boron-oxygen complexes during illumination [117]. Furthermore, n-type wafers exhibit a higher charge carrier lifetime and are more tolerant to chemical and crystallographic defects [118].

3.1.1 Texturing of silicon wafer

Texturing of wafers is a standard process to increase the absorption properties of solar cells [5]. It refers to the creation of pyramid-like structures on the wafer surface. This leads to a lower reflection and enhanced absorption which results in an increased short-circuit current density (J_{SC}). However, it can also increase the complexity of the fabrication process due to the structural changes of the interface. Multiple different methods like mechanical engraving, plasma etching and chemical etching exist to texture silicon wafers. In this work wet-chemical etching is adopted for the texturing procedure [119]. To obtain a single-side textured wafer, the first step is the deposition of a silicon nitride (SiN_x) layer to protect one side of the wafer from the texturing process. Subsequently, the wafer is submerged into an aqueous Tetramethylammonium Hydroxide (TMAH) solution for 15 minutes at 85 °C. The solution consists of 4L of water, 1L of TMAH and 120ml of AlkaTex8. This results in a selective etching process of the $< 100 >$ silicon atoms and the formation of pyramids and faces with a $< 111 >$ orientation. The pyramids are approximately 0.5-2 µm in size

[120]. After that, the wafer is dipped into a solution of hydrofluoric acid (HF) and nitric acid (HNO_3) for two minutes to smoothen the tips of the pyramids [121]. Finally, the wafer is submerged into buffered hydrofluoric acid (BHF) to remove the SiN_x layer.

3.1.2 Standard cleaning

Prior to the start of the depositions, the sample undergoes a standard cleaning procedure to remove any organic and inorganic contamination. First, the wafer is immersed into a 99% HNO_3 solution for 10 minutes and then rinsed with deionised (DI) water for 5 minutes. Subsequently, the wafer is immersed into a 69.5% HNO_3 for 10 minutes at 110 °C and again rinsed for 5 minutes with DI water. To remove the native oxide layer on the wafer surface before any deposition, the wafer undergoes a Marangoni cleaning and drying procedure. For the Marangoni process the sample is submerged in 0.55% HF for 5 minutes and then rinsed in DI water for another 5 minutes together with the addition of isopropyl alcohol. Following the standard cleaning and Marangoni process the wafer is ready for the deposition of the silicon oxide (SiO_x) layer.

3.1.3 Dry thermal oxidation

The ultra-thin SiO_x tunneling layer plays an important role in the working mechanism of the high-temperature CSPC. A detailed overview of various deposition methods is given in Section 2.5.1. In this thesis the deposition of the oxide layer is done by dry thermal oxidation [88]. For the deposition of the SiO_x layer the wafers are placed vertically in a quartz boat in a Tempress furnace. First the atmosphere is flushed with nitrogen while the temperature is increased from 600 °C to 675 °C at a rate of 10 °C per minute. Once the final temperature is reached, oxygen is introduced to the system to initiate the oxidation reaction of the silicon. After three minutes the oxygen flow is stopped, the furnace is flushed with nitrogen again to prevent any further film growth and the temperature is ramped down. Directly after this oxidation step the wafers should be placed in the low-pressure chemical vapor deposition (LPCVD) system to hinder the growth of a native oxide layer.

3.1.4 Deposition of a-Si by LPCVD

To protect the ultra-thin silicon oxide layer, an amorphous silicon (a-Si) layer is deposited directly after the oxidation process via LPCVD. Chemical vapor deposition is the deposition of a solid thin film from the gas phase via a chemical reaction. The advantage of performing the deposition at lower pressure is the higher uniformity and lower defect density of the layer. A 10 nm thick layer is grown in a tube furnace at 580 °C with a SiH_4 gas flow rate of 45 sccm at 150 mTorr. A schematic of a LPCVD furnace is shown in Figure 20. The gas enters the deposition tube and is thermally activated to initiate the deposition reaction. On the other side of the tube the excess gas is removed again.

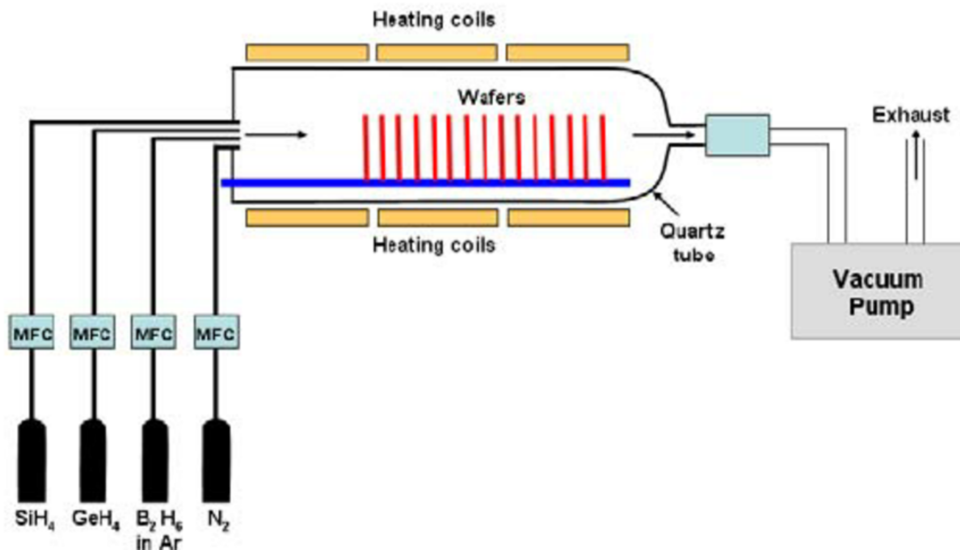


Figure 20: A schematic of a LPCVD furnace [16].

3.1.5 Deposition of doped amorphous SiO_x by RF-PECVD

Prior to the deposition of the doped amorphous silicon oxide (a-SiO_x) layer, the native oxide layer has to be removed by Marangoni drying. This is done to avoid interface defects. The defects are similar to the blisters which can develop if hydrogen is rapidly released during the annealing process [122]. After that, the deposition of the doped a-SiO_x can take place. Plasma-enhanced chemical vapor deposition (PECVD) is performed at low pressure and like the name suggests, the chemical reaction is initiated by a plasma. This has the advantage that the deposition can take place at lower temperatures around 200-350 °C. The plasma is created via electrical energy [97]. The gas is directed between two electrodes and a voltage is applied which ionizes the gas. The simplest method is the DC discharge PECVD where a direct current is applied between the plates. However, this results in problems with insulating films since at a certain thickness the plasma can not be maintained due to the insulating effect of the grown layer. Therefore, radio frequency or microwave PECVD setups are commonly utilised which circumvent this problem. A typical radio frequency PECVD setup is shown in Figure 21. The gas is directed towards the reaction chamber where it is ionized. The highly reactive gas reacts on the substrate surface and forms the solid film. The film growth and film properties depend on many factors like the temperature, pressure, gas composition, reactor geometry, applied voltage, homogeneity of the discharge, distribution of species in the plasma and frequency [123]. For the deposition of the thin film layers in this project, the PECVD system AMOR by Elettrorava is used. Just after removing the native oxide layer, the wafer is placed in the reaction chamber at about 300 °C and a gas mixture of silane (SiH_4), carbon dioxide (CO_2), hydrogen (H_2), phosphine (PH_3) and diborane (B_2H_6) is introduced into the reaction chamber. The gas is ionized by applying a RF voltage of 13.56 MHz and the deposition takes place.

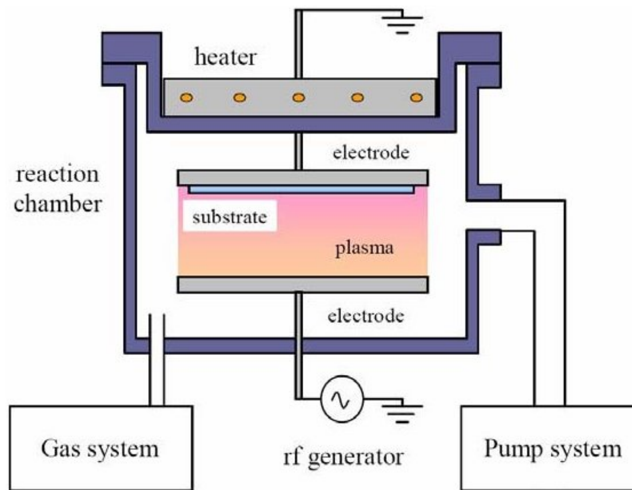


Figure 21: Schematic of a radio frequency PECVD setup [17]

3.1.6 High-temperature annealing

Following the deposition of the doped amorphous silicon oxide layers, the sample is annealed at high temperature to crystallise the amorphous layers previously deposited. Furthermore, dopants and oxygen will diffuse into the intrinsic a-Si LPCVD layer. The annealing is usually performed between 800 °C and 1000 °C in nitrogen atmosphere. It strongly influences the passivation quality of the ultra-thin SiO_x layer as well as the field effect passivation of the device. Higher annealing temperatures leads to the formation of pinholes in the SiO_x layer and slightly decreases its thickness [124]. The pinholes can enhance the charge transport through the layer but also lower the passivation quality [86, 82]. However, high annealing temperatures also increase the dopant diffusion from the contacts into the crystalline silicon (c-Si) absorber material which lowers the field effect passivation.

3.1.7 Hydrogenation

Hydrogenation is performed to further passivate interface defects and lower the recombination losses. Different hydrogenation processes are widely adopted in almost every silicon solar cell [125]. Hydrogenated dielectric layers like AlO_x or SiN_x are used as a hydrogen source and during the thermal annealing process, hydrogen atoms are ejected into the bulk of the material to passivate interface defects like dangling bonds. In this project, SiN_x is deposited via PECVD using silane gas and ammonia at 400 °C followed by forming-gas annealing (FGA) at 400 °C for 30 minutes.

3.1.8 Deposition of TCO by RF magnetron sputtering

In homojunction solar cells the transport of the charge carriers to the metal happens in the doped contacts. However, in carrier-selective passivating contacts the amorphous and polycrystalline silicon layers are not conductive enough [126, 106]. Hence, TCOs are necessary in TOPCon solar cells due to the poor lateral conductivity of the polycrystalline silicon oxide (poly-SiO_x) layers. There are multiple material requirements to the TCO like low sheet resis-

tance, high transparency, low absorption and reflectance and a low Schottky barrier. This is described in more detail in Section 2.5.3. The most common TCO is indium tin oxide (ITO) which is usually made up of 90% indium oxide (In_3O_3) and 10% tin oxide (SnO_2). ITO is most commonly deposited via a magnetron sputtering process. Sputtering is a physical vapor deposition process during which the sputtering gas (usually argon) bombards a target and physically ejects atoms from the target. A plasma is used to energize the argon atoms due to collisions with electrons. In magnetron sputtering, magnets are used to confine the electrons close to the target surface. A typical magnetron sputtering chamber is shown in Figure 22. This leads to a higher deposition rate since the energized argon atoms are also closer to the target surface and therefore more likely to hit and eject atoms from the target. The ejected atoms will then form a solid thin film on the substrate. Due to the high energy of the particles which deposit on the substrate sputtering damage can occur. Sputtering damage introduces defects to the substrate surface and can reduce the passivation in solar cells. This can be partially recovered by a post TCO deposition annealing.

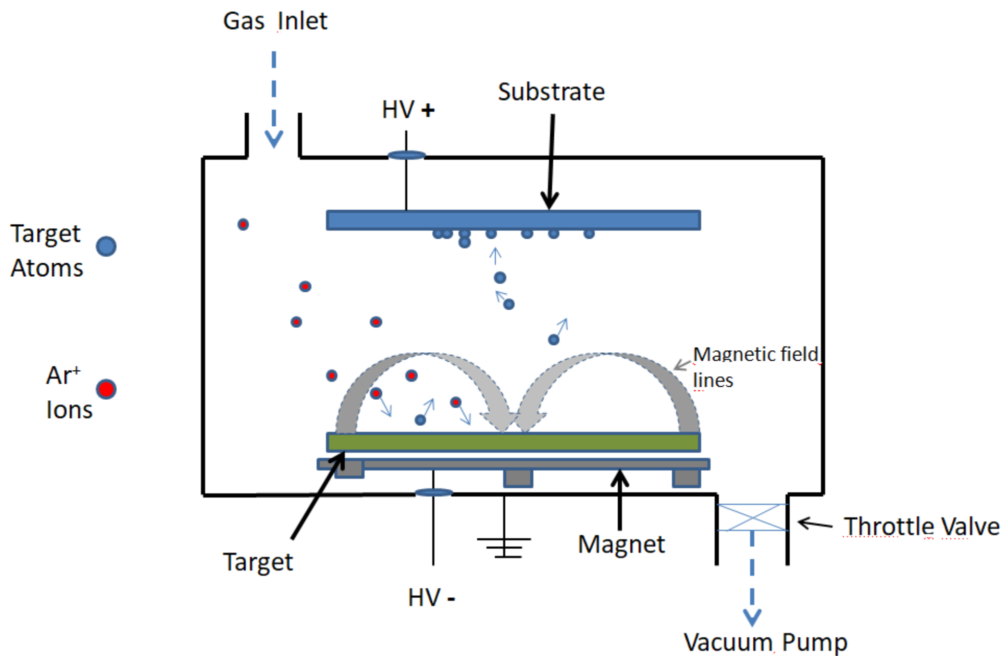


Figure 22: Schematic of a radio frequency magnetron sputtering setup [18].

3.1.9 TCO recovery annealing

It is well-known that sputtering deposition methods induce defects in the surface layers of the sample due to the bombardment with highly energized particles [127]. This phenomenon increases the defect density and negatively influences the passivation quality of the device. It has been shown that the sputtering process itself is responsible for the damages and not the sputtered material [128]. The degradation of the implied open-circuit voltage (iV_{OC}) seems to originate from the creation of dangling bonds from Si-Si or Si-H bonds which are both susceptible to rupture upon bombardment with Ar atoms. However, it has been observed that the damage can be (partially) recovered by annealing at temperatures

between 200-400 °C [129, 130, 131]. The TCO recovery annealing conditions utilized in this work are discussed in more detail in Section 6.1.

3.1.10 Deposition of metal contacts

Lastly, the metal contacts have to be deposited. The purpose of the metal is the efficient collection of charge carriers due to its high conductivity. However, metal also has a very low transmission of light in the relevant wavelength range. Hence, at the front side the metal coverage has to be minimised to ensure that the light can enter the solar cell device. For single junction solar cells this is done by screen printing because of the need for a mask at the front side while for the tandem device full-area thermal evaporation is adopted [19]. Screen printing utilizes a screen with a stencil where the silver paste is pushed through by the squeegee. A schematic is shown in Figure 23. During the process the screen has direct contact with the sample which can lead to surface damages. Furthermore, the silver paste consists of small silver particles embedded into a binder. Hence, the samples have to be annealed after the process to evaporate the binder and to ensure contact formation between the ITO/Ag interface but also between the individual silver particles. This is done at 170 °C for 30 minutes. Finally, another annealing step at 250 °C for 5 minutes on a hot-plate is applied to further improve the contact formation.

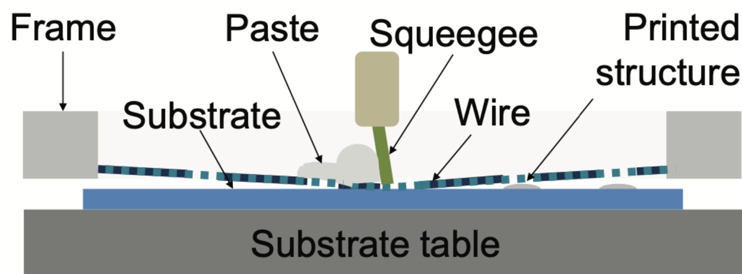


Figure 23: Schematic of the screen printing setup [19].

For the c-Si bottom cell for tandem application full back-area thermal evaporation is used. Thermal evaporation is a physical vapor deposition technique that usually takes place at very low pressure to reduce the processing temperature [132]. Small silver particles are heated in a crucible and evaporated onto the substrate for a final film thickness of 500 nm.

3.2 Characterization

In this section, the different methods used to analyse and characterize the different material layers and the solar cell are introduced and discussed.

3.2.1 Photoconductance Lifetime Measurement

Lifetime measurements are important to characterize the passivation quality of the solar cell precursor during different steps of the fabrication process. The most important parameters which are determined are the effective lifetime of the minority carriers (τ_{eff}), the iV_{OC} and

the saturation current density (J_0). For this project, the Sinton WCT-120 is used to measure the iV_{OC} and lifetime of the samples during every step from the annealing to the metallization. A schematic of the measurement setup is shown in Figure 24.

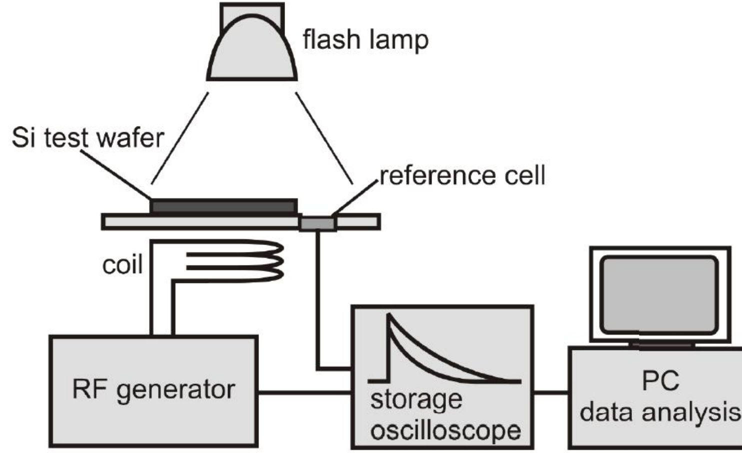


Figure 24: Schematic of a photoconductance lifetime measurement setup [20]

The principle is based on the measurement of the photoconductance of a sample when illuminated with a light flash [133, 134]. As shown in Figure 24, the wafer is placed on the stage and is then illuminated by a lamp for very short time periods. During the illumination, the minority carrier concentration and conductance increases which is recorded by the measurement setup. The continuity equation links the generation G and recombination R of the carriers with the change in minority carrier concentration $\frac{\delta \Delta p}{\delta t}$ in a n-type semiconductor where the current density J is zero since no currents are flowing in steady-state:

$$\frac{\delta \Delta p}{\delta t} = G - R + \frac{1}{q} \nabla J \tag{15}$$

Now, we can apply the definition of the effective charge carrier lifetime:

$$\tau_{eff} = \frac{\Delta p}{R} \tag{16}$$

By combining equation 15 and 16, we arrive at equation 17 which connects the effective charge carrier lifetime with the generation and the minority carrier concentration. A higher illumination also increases the conductance since more charge carriers are injected.

$$\tau_{eff} = \frac{\Delta p}{G(t) - \frac{\delta \Delta p}{\delta t}} \tag{17}$$

The lifetime measurement can be conducted in two different modes. First, the transient photoconductance (TPC) measurement is based on an extremely short light pulse. After the sample is illuminated for just a moment, the generation is assumed to be zero and the decay of the minority charge carrier concentration is measured by the setup. In this case, equation 17 simplifies since *G(t)* can be neglected. This method is usually recommended for samples with a lifetime of 200 µs and more. On the other hand, quasi-steady-state photoconductance (QSSPC) is based on a very slow variation of the illumination which means one can neglect

the $\frac{\delta \Delta p}{\delta t}$ term in equation 17 since the generation is significantly higher. This mode is recommended for samples with a very low lifetime below 200 µs. The iV_{OC} can be calculated according to equation 18 where N_D is the donor concentration and n_i the intrinsic charge carrier concentration.

$$iV_{OC} = \frac{k_B T}{q} ln \left[\frac{\Delta p (N_D + \Delta p)}{n_i^2} \right] \quad (18)$$

3.2.2 Spectroscopic Ellipsometry

Spectroscopic ellipsometry (SE) is an optical characterization technique [135]. A flat sample is irradiated with polarized light and the change in the polarization upon reflection or transmission is measured to determine different properties like thickness, surface roughness, refractive index and dielectric constant. In Figure 25, the setup is shown. It consists of a light source, a polarizer, a compensator (which improves accuracy of the measurement), another polarizer (called an analyzer) and a detector. The unpolarized light is first linearly polarized by the polarizer and then reflected by the sample. This induces a change in the amplitude ratio and the phase difference of the light which is measured by the detector after it passes the analyzer. Theoretically, SE can achieve extremely high accuracy up to single atomic layers due to the high sensitivity in measuring the phase difference. However, this is complicated to achieve since the optical models used in the analysis can hardly simulate real imperfections in such thin layers [135]. Furthermore, the technique is non-destructive and there is no direct contact with the sample. For this project, the M-2000 ellipsometer by J.A. Woollam is used to measure the thickness of various layers like the SiO_x passivating layer and the ITO.

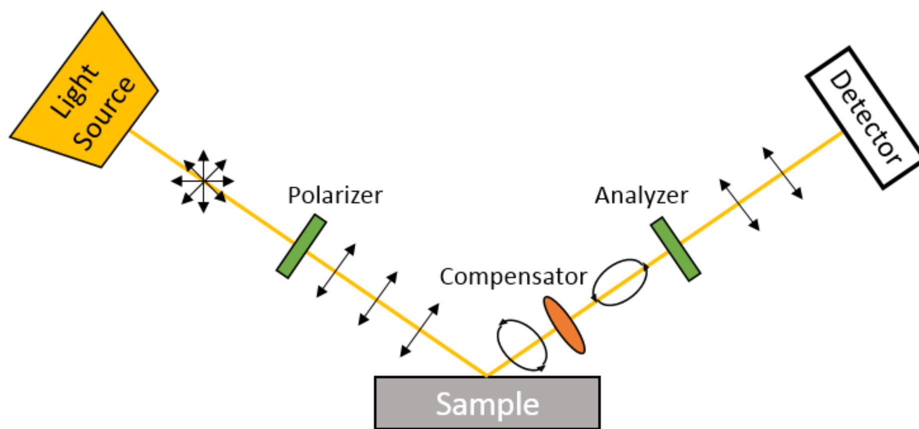


Figure 25: Schematic of the working principle of a spectroscopic ellipsometry measurement setup [21].

3.2.3 Illuminated J-V measurement

J-V measurements are used to characterize the final performance of solar cells [5]. The most important parameters of a solar cell are the open-circuit voltage (V_{OC}), the short-circuit current density (J_{SC}), the fill factor (FF) and the efficiency (η). For this project, a solar simulator

from Wacom is utilised for the measurements. This is to ensure that standard test conditions (STC) apply. Hence, the illumination is always $1000W/m^2$ and the AM1.5 spectrum is simulated using a Xenon/Halogen lamp. Furthermore, the temperature of the device is kept constant at 25 °C.

The J_{SC} is the maximum current that the device can deliver at short-circuit conditions. It depends on the photon flux since more light with higher energy results in an increased generation of charge carriers. Furthermore, it is also strongly dependent on the optical properties of the solar cell device like the reflection and transmission of the layers.

The V_{OC} is the maximum voltage that the device can deliver when no current flows. It mainly depends on the photo-generated current J_{ph} and the saturation current density J_0 which is a measure of the recombination in the solar cell (Equation 19). Since the generated current varies mostly with the illumination, the V_{OC} is strongly dependent on the recombination.

$$V_{OC} = \frac{k_B T}{q} ln\left(\frac{J_{ph}}{J_0} + 1\right) \tag{19}$$

The fill factor is the ratio of the maximum power that the device can actually deliver and the theoretical power output at the V_{OC} and the J_{SC} conditions. This can be observed in equation 20 where the subscript mpp signifies the current/voltage at the maximum power point. The fill factor is a measure of the junction quality and can be reduced due to resistive losses. The series and shunt resistance play an important role in solar cells and influence the J-V curve strongly. Due to modern processing techniques, the shunt resistance usually does not affect the performance of the fabricated devices significantly while the series resistance poses a concrete challenge and lowers the slope of the J-V curve and reduces the fill factor.

$$FF = \frac{J_{mpp} * V_{mpp}}{J_{SC} * V_{OC}} \tag{20}$$

Lastly, the final efficiency of the solar cell is the ratio of the maximum power output P_{mpp} of the solar cell and the incident power I_{in}. As shown in equation 21, it can also be rewritten to be dependent on the J_{SC}, the V_{OC} and the fill factor.

$$\eta = \frac{P_{mpp}}{I_{in}} = \frac{J_{mpp} * V_{mpp}}{I_{in}} = \frac{J_{SC} * V_{OC} * FF}{I_{in}} \tag{21}$$

3.2.4 EQE measurement

The external quantum efficiency (EQE) describes the number of photons that are collected by the external circuit compared to the number of photons incident on the solar cell [5]. Therefore, it is the ratio of the current of the device and the photon flow. The EQE can be measured by determining the photocurrent I_{ph} of the device and dividing it by the spectral photon flux $\Psi_{ph,\lambda}$ with q being the elementary charge as shown in equation 22. $\Psi_{ph,\lambda}$ is determined by using a reference diode with a known EQE curve.

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\Psi_{ph,\lambda}} \tag{22}$$

The EQE measurement can also be utilised to determine the J_{SC} of the device according to the equation below with $\phi_{ph,\lambda}^{AM1.5}$ being the spectral photon flux of the AM1.5 spectrum.

$$J_{SC} = -q \int_{\lambda_1}^{\lambda_2} EQE(\lambda)\phi_{ph,\lambda}^{AM1.5} d\lambda \tag{23}$$

In this project a self-built EQE measurement setup is used. It consists of a wavelength selective light source, a light detector and a current meter. Filters and monochromators are utilised to generate small wavelength ranges between 300 nm and 1200 nm to measure the EQE at different wavelengths.

3.2.5 SunsVoc measurement

The SunsVoc measurement is used to determine a pseudo J-V curve [136, 137]. A flash light with a slow decay is used to produce a voltage vs. illumination curve. The J_{SC} value from the Wacom or EQE measurement is used as an input parameter. Using the SunsVoc measurement, a pseudo open-circuit Voltage pV_{OC} and a pseudo fill factor (pFF) are determined which neglect the series resistance in the solar cell and demonstrate the upper limit of the two values. This can be handy to analyse the series resistance R_s which can be calculated according to equation 24.

$$R_{s,SunsVoc} = (pFF - FF)\frac{V_{OC}J_{SC}}{J_{mpp}^2} \tag{24}$$

3.2.6 UV/VIS/NIR spectroscopy

For the measurement of reflection, transmittance and absorptance a LAMBDA 1050+ UV-Vis-NIR spectrophotometer from PerkinElmer is adopted. Ultraviolet-Visible-Near-Infrared (UV/Vis/NIR) spectroscopy can be used to analyze the optical characteristics of various materials. For this thesis it is especially interesting to characterise the reflection of the finished solar cell to investigate the internal quantum efficiency. This can help to evaluate the possible potential of the device. To measure the different optical properties the sample is illuminated with wavelengths between 300 and 1200 nm. In the case of the reflection measurement the sample is mounted at the back side of a so-called integrating sphere which is coated with highly reflective material on the inside. The sample is then illuminated and the reflection for every wavelength is measured by a photodetector. An overview of the optical setup of such a system with the integrating sphere and the sample positions is shown in Figure 26.

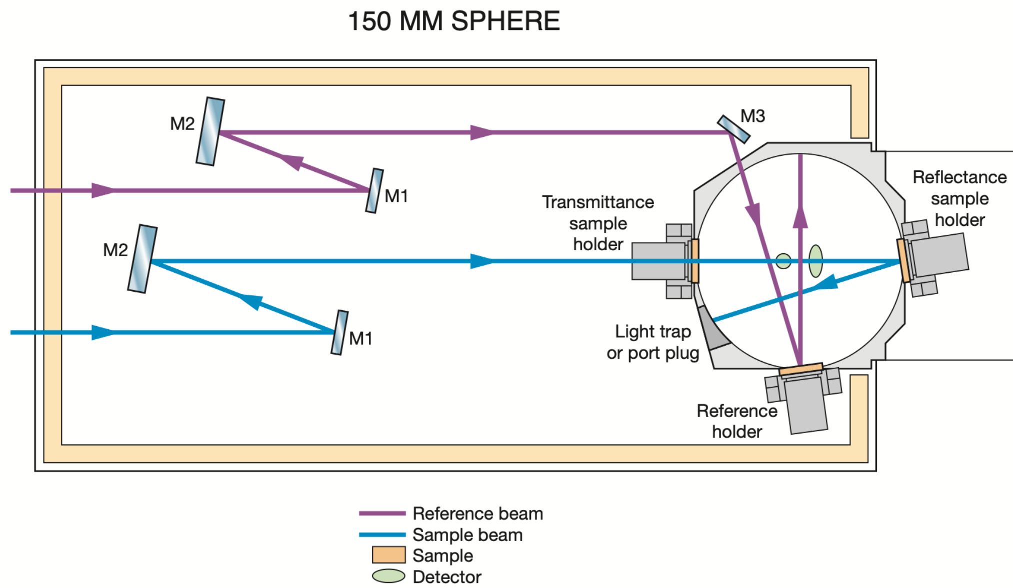


Figure 26: Top view of the optical setup of the UV/Vis/NIR spectrophotometer [22].

3.3 Optical Simulations - GenPro4

GenPro4 is a simulation software developed by researchers at TU Delft which models the optical properties of solar cells of any type. It utilizes wave and ray optics to simulate how various materials and interfaces behave and interact with light. It purely focuses on the optical properties of solar cells and completely disregards the electrical properties. GenPro4 is especially useful to determine the absorptance in the different layers and for current matching multijunction devices. Below the software is briefly described. A more detailed explanation can be found in the paper by Santbergen et al. (2017) [23].

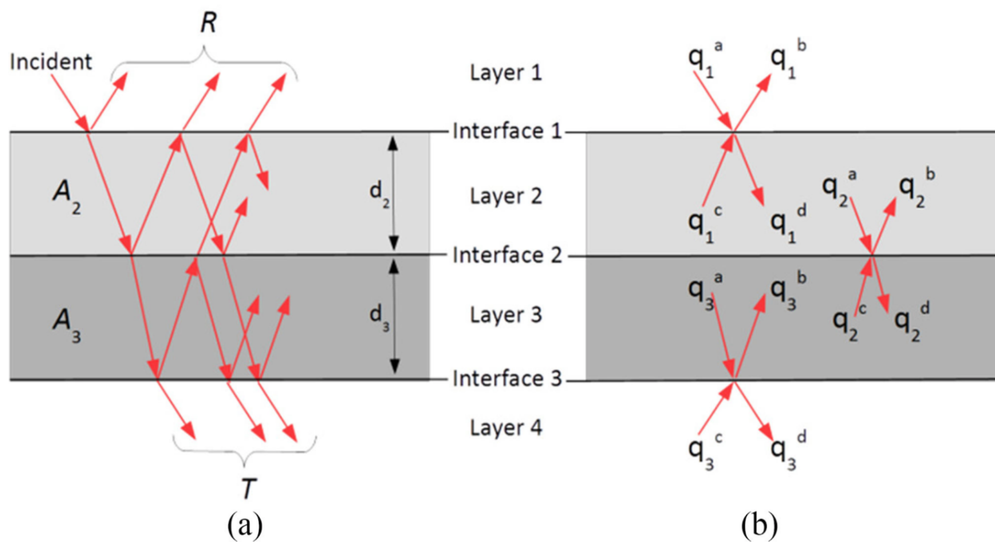


Figure 27: The path of light in a solar cell (a) and a schematic representation of the basic working principle of the net-radiation method (b) [23].

The software is programmed in Matlab and needs the thickness of the layers as well as the complex refractive index at every wavelength as input parameters. This information is

used to calculate the reflectance, absorptance and transmittance in every material. GenPro4 considers the scattering of electromagnetic waves at interfaces and the trapping of light within the different layers. It reduces the solar cell to a 1-D multilayer structure which strongly reduces the computational power and time.

It can model flat interfaces based on basic optical formulas like the Fresnel equations, Snell's law and the Lambert-Beer law. This is done by using ray optics and simply calculating the reflectance (R), absorptance (A) and transmittance (T) as displayed in Figure 27a where d represent the thickness of the layers. Since, the path of an electromagnetic wave can be quite complex the so-called net-radiation method is utilised which is shown in Figure 27b where q represents the light intensity flux and the subscripts and superscripts corresponds to the interface number and the propagation direction, respectively. This method essentially adds or subtracts the light intensity for every wavelength according to the interaction with the interfaces and materials. However, to reduce reflection most solar cells utilize textured interfaces. That can also be simulated using GenPro4 by introducing wave effects like diffraction interference with a scalar scattering model [138, 139]. This is only necessary when considering textured features that are smaller than the wavelength. For flat interfaces one discrete propagation direction is assumed. When considering textured interfaces, the electromagnetic waves are represented by an angular intensity distribution over the available propagation direction.

4

Passivation optimization of poly-SiO_x contacts

In this chapter the focus lies on the passivation optimization of the polycrystalline silicon oxide (poly-SiO_x) passivating contacts. The two different types of lifetime samples (polished n-type and textured p-type) are shown in Figure 28. First in Section 4.1, the fabrication steps of n and p-type symmetric passivation samples are described. In Sections 4.2 and 4.3 the influence of the annealing conditions on both symmetric samples are presented and discussed. Finally, the effect of the hydrogenation on the implied open-circuit voltage (iV_{OC}) and the charge carrier minority lifetime is evaluated and the optimal silicon oxide (SiO_x) passivating layer thickness and annealing conditions are determined in Section 4.4. Finally, a brief conclusion is given in Section 4.5. Furthermore, polished p-type symmetric samples were also fabricated for the fabrication of a double-side polished (DSP) solar cell. The results are presented in Appendix A.2. The starting point of this work is based on previous work done in the PVMD group at TU Delft [140, 141].

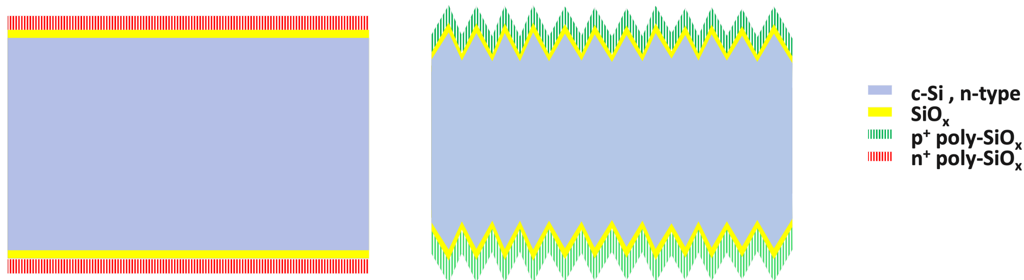


Figure 28: Design of the symmetric samples used for the passivation optimization. A n-type crystalline silicon (c-Si) wafer is capped with a SiO_x film and p-doped (p+)/n-doped (n+) poly-SiO_x layers. Only the p-type symmetric sample is textured.

4.1 Fabrication process of symmetric samples

To determine the optimal fabrication process, an passivation optimisation of the symmetric samples needs to be performed. The final device has a polished n-type front contact and a textured p-type rear contact. Hence, symmetric samples for each of those contacts were prepared and analysed. Below, the fabrication process of the textured p-type symmetric sample is described. The fabrication process for the polished n-type symmetric sample is the same except for phosphorous as the dopant and without the texturing step. The whole procedure is also illustrated in Figure 29. As the starting point, n-type float zone $< 100 >$ oriented silicon wafers with a diameter of 100 mm, a thickness of 280 μ*m* (+/- 20 μ*m*) and a resistivity of 1-5 Ω cm are utilised.

- To obtain double-side textured wafers, the wafers are submerged into an aqueous Tetramethylammonium Hydroxide (TMAH) solution for 15 minutes at 85 °C. The solution consists of 4L of water, 1L of TMAH and 120ml of AlkaTex8. After the texturing step, the wafer is dipped into a solution of hydrofluoric acid (HF) and nitric acid (HNO_3) for two minutes to smoothen the tips of the pyramids. This whole procedure is only done for the p-type symmetric samples.

- To prepare the wafers for the depositions, they undergo a standard cleaning procedure to remove organic and inorganic contaminations. First, the wafers are immersed into a 99% HNO_3 solution for 10 minutes and then rinsed with deionised (DI) water for 5 minutes. Subsequently, the wafers are immersed into a 69.5% HNO_3 solution for 10 minutes at 110 °C and again rinsed for 5 minutes with DI water. This is followed by a Marangoni drying to remove the native oxide layer.

- Next, the ultra-thin SiO_x tunneling layer is deposited via dry thermal oxidation. This is done in a horizontal Tempress furnace at 675 °C. The optimal conditions of the oxidation is investigated in this chapter in Sections 4.2 - 4.4. A longer oxidation reaction corresponds to a thicker SiO_x layer.

- Immediately after the thermal oxidation, a 10 nm intrinsic amorphous silicon layer is deposited in a low-pressure physical vapor deposition (LPCVD) furnace with a silane flow rate of 45 standard cubic centimeter per minute (sccm).

- Subsequently, the boron-doped amorphous silicon oxide (a-SiO_x) is deposited via plasma-enhanced chemical vapor deposition (PECVD) on both sides of the wafer. Before that, the wafers undergo a Marangoni drying to remove the native oxide layer to obtain a good contact between the intrinsic amorphous silicon (a-Si) and the doped a-SiO_x layers.

- The wafers are then annealed at high temperature to crystallize the amorphous layers and activate the dopants for the diffusion from the doped to the intrinsic layer. Now, the passivation quality of the symmetric sample is determined using the Sinton WCT-120 photoconductance lifetime measurement setup. This includes the iV_{OC} and the lifetime of the minority charge carriers (τ).

- Lastly, the hydrogenation process is performed. A hydrogenated silicon nitride (SiN_x) layer is deposited. Subsequently, this layer acts as a hydrogen source during the forming gas annealing at 400 °C for 30 minutes to passivate the defects and improve the passivation quality. Again, the iV_{OC} and τ are measured using the lifetime measurement setup.

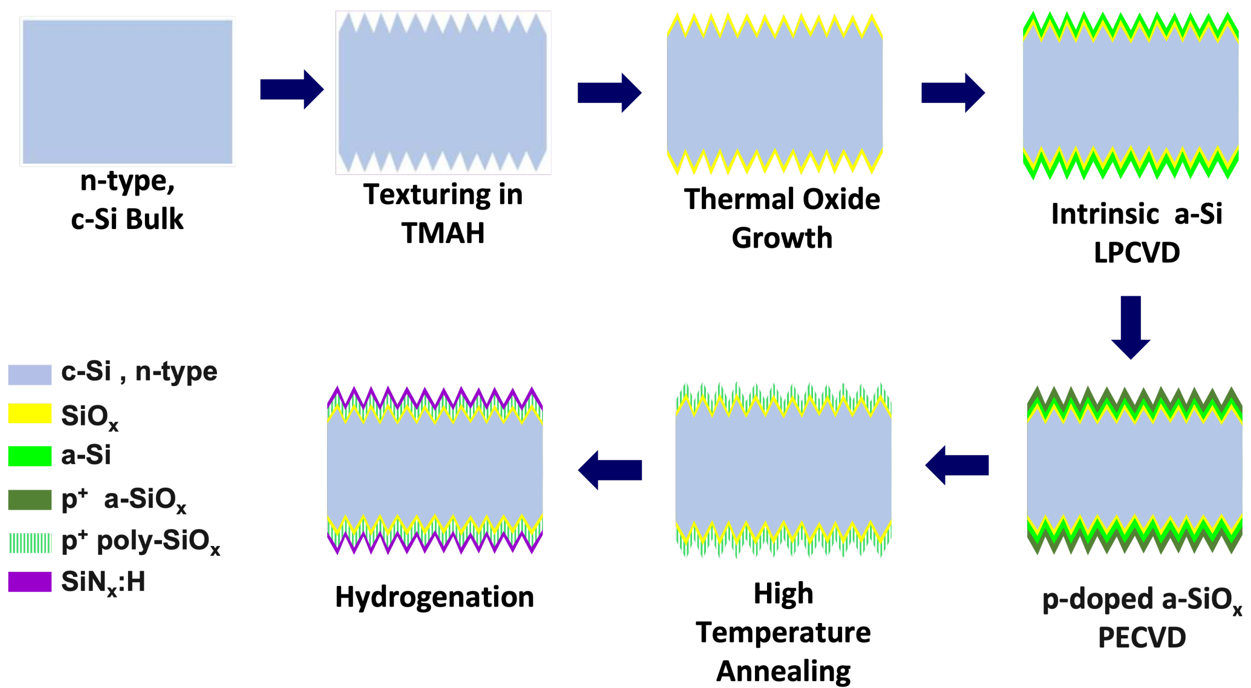


Figure 29: Fabrication process of a p-type textured symmetric sample used to optimize the processing conditions.

4.2 Optimization of the polished n-doped poly-SiO_x contact

In Figure 30, the results of the passivation tests of the polished n-doped poly-SiO_x symmetric sample before hydrogenation are displayed. On the vertical axis the iV_{OC} is given, while on the horizontal axis the three different annealing conditions are presented. Temperatures between 850 and 950 °C were chosen according to literature and previous experience within the PVMD group [12, 88, 96, 140]. The color of the markers indicates the duration of the dry thermal oxidation process. A longer thermal oxidation corresponds to a thicker SiO_x layer. It can be observed that the maximum iV_{OC} of 727 mV was measured for thermal oxidation conditions of 675 °C 3 minutes when annealed at 900 °C for 15 minutes. A slightly lower iV_{OC} of 725 mV was measured for the sample with a thermal oxidation duration of 4 minutes denoted in yellow in Figure 30 for the same annealing conditions. Generally, the values for the annealing temperature of 900 °C are best for all the different silicon oxide thicknesses. At a lower thermal budget, insufficient dopant diffusion might limit the passivation. A rapid decrease at a higher annealing temperature can be observed. The reason for this might be the thermal instability of the passivating layer at higher temperature and consequentially the enhanced diffusion of dopants into the crystalline silicon (c-Si) bulk which lowers the field effect passivation [88]. However, the relatively high iV_{OC} of the 2 minute thermal oxidation sample denoted in blue in Figure 30 at 950 °C is counter-intuitive since the thin silicon oxide passivating layer should disintegrate first at higher temperature and hence display a lower passivation than the samples with a relatively thicker passivating layer. Therefore, other effects like the formation of pinholes at higher temperatures might be responsible for this behaviour [87, 142]. In conclusion, the annealing conditions at 900 °C are superior, especially compared to annealing at a higher thermal budget for polished n-doped symmetric samples.

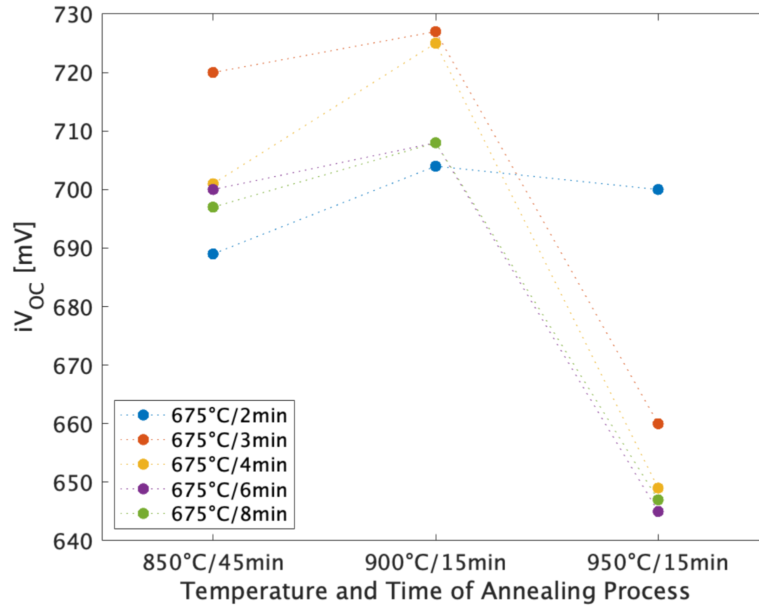


Figure 30: Comparison of the iV$_{OC}$ of the polished n-type symmetric samples with different SiO$_x$ thicknesses and different annealing conditions (dashed lines display the trend but do not depict measurements).

4.3 Optimization of the textured p-doped poly-SiO$_x$ contact

Similar to section 4.2, the results of the textured p-doped symmetric samples are presented in Figure 31. Again, the color denotes the duration of the dry thermal oxidation which results in a different thickness of the SiO$_x$ film. A clear trend with a higher passivation quality at lower annealing temperature for almost all samples can be observed. This reduction in passivation stems from the higher dopant diffusion into the silicon bulk at higher thermal budgets which lowers the field effect passivation [88]. The only outlier is the sample with the thinnest silicon oxide passivating layer denoted in blue in Figure 31 which displays the highest implied open-circuit voltage of 644 mV at an annealing temperature of 950 °C. Again, the reason might be related to the insufficient diffusion of dopants [87, 142]. The same passivation is observed for a thermal budget of 675 °C 2 minutes and 675 °C 8 minutes at an annealing temperature of 850 °C. However, the differences between the individual samples is only a few mV which is low compared to the results presented in Section 4.2. The passivation is generally much lower compared to the polished n-type symmetric samples. There are three main reasons for this. First, textured surfaces usually display a lower passivation quality since the thin films are often less uniform which results in a higher defect density at interfaces [12]. Second, for the p-doped symmetric samples boron is used as a dopant. Boron has a lower atomic radius then phosphorus and thus has a higher bulk diffusivity as well as enhanced diffusion along grain boundaries [143]. This will lead to an enhanced diffusion into the silicon bulk compared to the n-doped samples. Lastly, boron-oxygen complexes have been reported to reduce the minority carrier lifetime in silicon solar cells [144]. This phenomenon is especially pronounced with the poly-SiO$_x$ passivating contacts. The large amount of oxygen atoms might lead to the formation of detrimental boron-oxygen complexes which strongly reduces the minority carrier lifetime. Since the diffusion of boron will

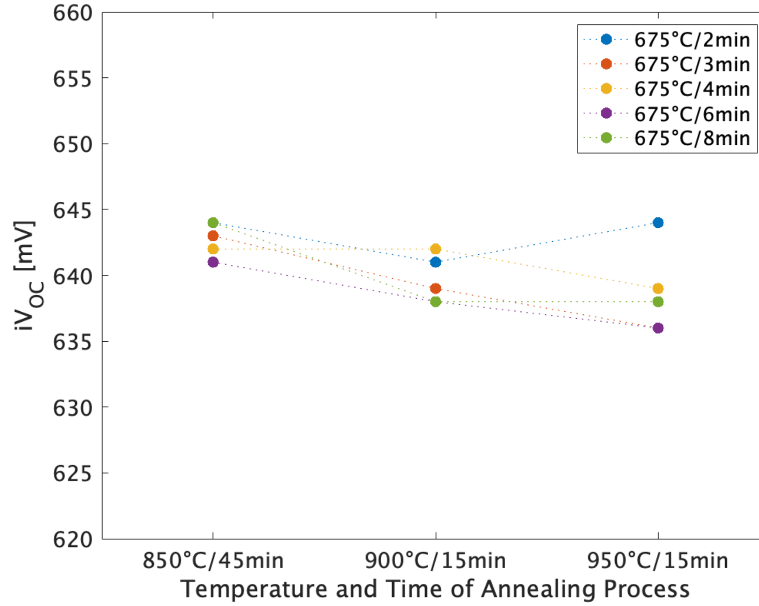


Figure 31: Comparison of the iV_{OC} of the textured p-type symmetric samples with different SiO_x thicknesses and different annealing conditions (dashed lines display the trend but do not depict measurements).

increase with higher temperature, a decrease in passivation quality is expected. Hence, the annealing conditions are optimal at 850 °C for textured p-doped symmetric samples. Even though this was found to be optimal, the choice of thermal budget also depends on the n-doped symmetric samples as described in Section 4.2 since the same processing conditions are finally applied to both contacts in a single-junction device.

4.4 Hydrogenation

In this section, the passivation quality of the symmetric samples with different thermal budgets during the dry thermal oxidation as described in Section 3.1.3 will be compared. This includes the iV_{OC} after annealing at 900 °C for 15 minutes and after hydrogenation. Furthermore, the minority charge carrier lifetime as a function of the minority charge carrier density after the hydrogenation process measured with the photoconductance lifetime measurement setup is analyzed. The annealing conditions of 900 °C and 15 minutes were chosen due to the results in the previous two sections. This is also discussed in more detail in Section 4.5. The iV_{OC} for the samples which were annealed at 850 °C and 950 °C are presented in Appendix A.1 in Figures 68 to 71. Hydrogenation is a process to chemically passivate the interface by introducing hydrogen atoms which can effectively reduce the defect density. This improves the passivation quality and decreases the recombination rate. In this project, the deposition of a hydrogenated SiN_x layer is followed by an annealing in forming gas at 400 °C for 30 minutes. The principles of chemical passivation and hydrogenation are described in more detail in Section 2.3.1 and 3.1.7, respectively.

First, in Figure 32 the iV_{OC} of the polished n-doped symmetric samples after annealing (depicted in blue) and after hydrogenation (depicted in orange) are presented. It can be observed that the sample with the 3 minute thermal oxidation exhibits the highest iV_{OC} of 745

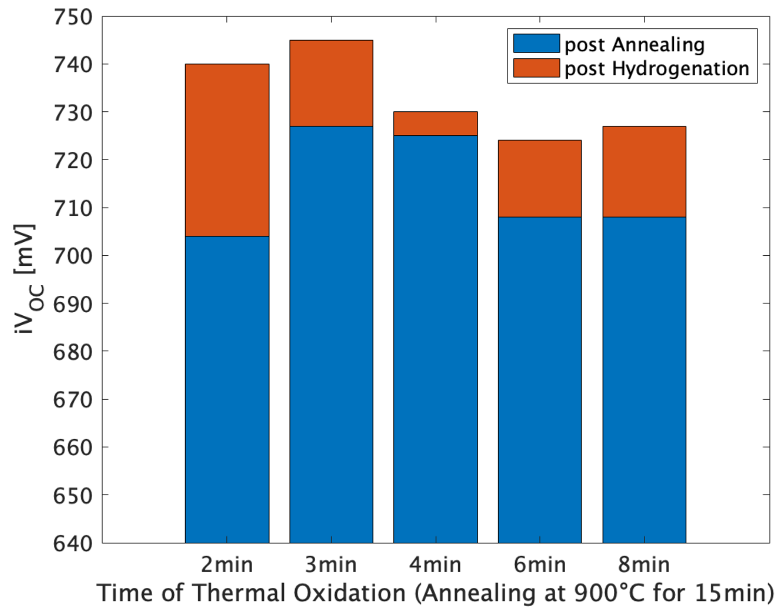


Figure 32: Comparison of the iV$_{OC}$ of the polished n-type symmetric samples with different SiO$_x$ thicknesses after annealing (blue) and after hydrogenation (orange).

mV after the hydrogenation process. Also interesting to mention is that the sample with a thermal oxidation duration of 2 minutes displays the highest passivation gain from 704 to 740 mV upon hydrogenation. This is plausible since the 675 °C 2 minutes SiO$_x$ layer is assumed to have the lowest thermal stability and hence a higher defect density after annealing. Therefore, the hydrogenation potential is higher.

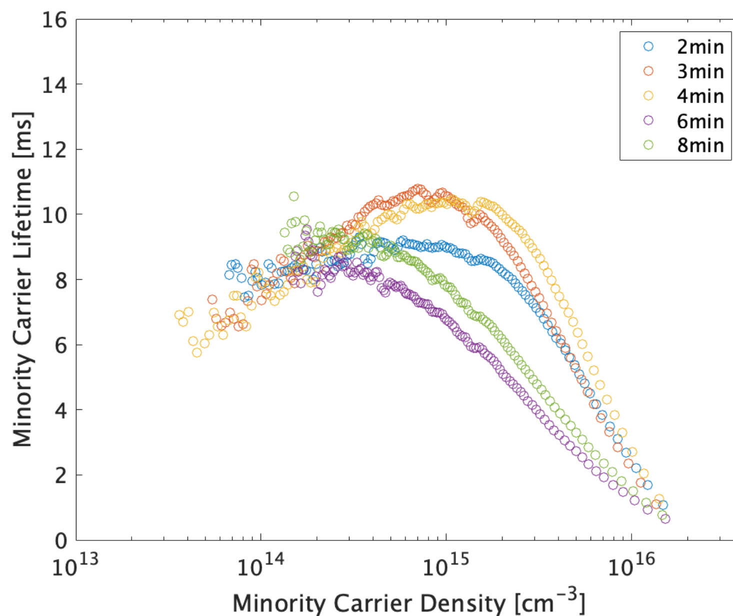


Figure 33: Comparison of the minority carrier lifetime as a function of the minority carrier density of polished n-type symmetric samples with different SiO$_x$ thicknesses after hydrogenation.

In Figure 33, the minority charge carrier lifetime is plotted against the minority charge carrier density. One can observe the typical shape of a lifetime curve. As explained in Section 2.2.2, in silicon solar cells Shockley-Read-Hall recombination is dominant at lower injection level while Auger recombination dominates at higher injection levels [8]. The consequence is a maxima at an injection level of 10^{14} - 10^{15} charge carriers per cm^3. The maximum lifetime is above 10 ms at about 10^{15} carriers per cm^3 for the 3 minute and 4 minute thermal oxidation samples. The other three samples exhibit a lower lifetime according to the photoconductance measurement. This can be explained by a higher defect density due to a lower thermal stability for the 2 minute SiO_x layer which promotes recombination [86, 87]. On the other hand, thicker SiO_x layers like the samples with 6 minutes and 8 minutes thermal oxidation acts as a barrier for the charge carriers because they exhibit a lower tunneling probability which decreases the carrier extraction [84].

In Figure 34, the iV_{OC} of the textured p-type sample with different dry thermal oxidation conditions are displayed. The sample with a thermal oxidation duration of 2 minutes exhibits the highest iV_{OC} after hydrogenation of 676 mV. However, the two samples with slightly thicker layers (3 and 4 minutes thermal oxidation) also display passivation values above 670 mV. The samples corresponding to a thermal budget of 6 minutes and 8 minutes during the dry thermal oxidation process display a lower passivation of just above 660 mV. This originates from the lower carrier extraction due to the decrease in tunneling probability [84].

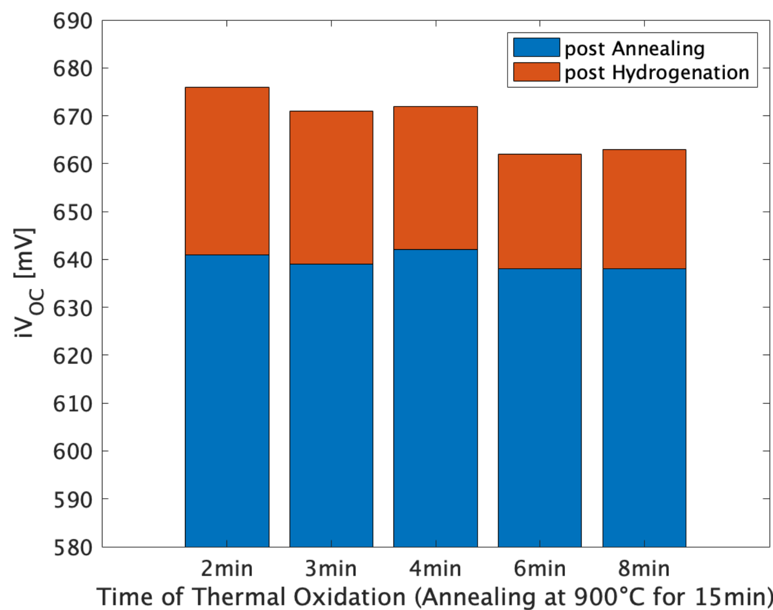


Figure 34: Comparison of the iV_{OC} of the textured p-type symmetric samples with different SiO_x thicknesses after annealing (blue) and after hydrogenation (orange).

The minority charge carrier lifetime curves are shown in Figure 35. It can be observed that the second sample, with the 3 minute thermal oxidation time, displays the highest lifetime over the entire measurement range with a lifetime above 1 ms at 10^{15} carriers per cm^3. The two samples with the thicker silicon oxide layers exhibit the lowest lifetime which, as

just mentioned above, is related to an enhanced recombination due to the lower tunneling probability [84].

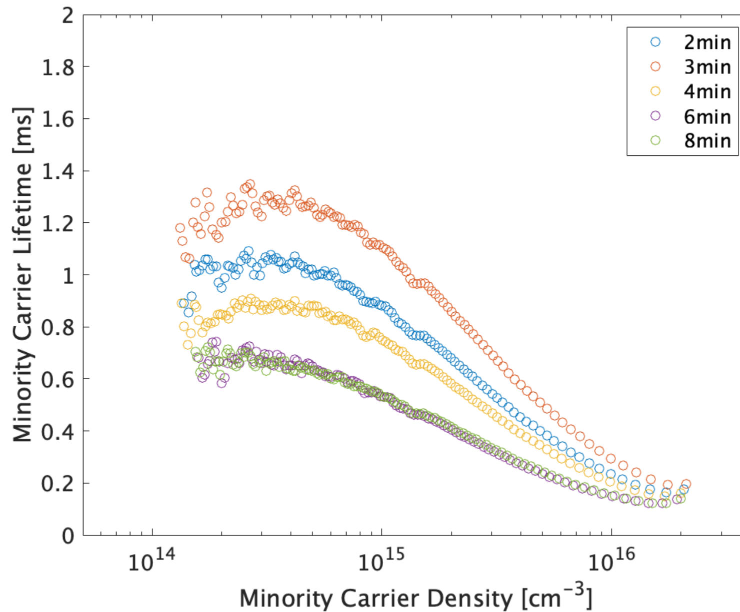


Figure 35: Comparison of the minority carrier lifetime as a function of the minority carrier density of textured p-type symmetric samples with different SiO_X thicknesses after hydrogenation.

4.5 Summary

As expected, the passivation quality of the polished n-type symmetric sample is higher than the textured p-type symmetric sample before and after hydrogenation. The three main reasons for this were already mentioned in Section 4.3. Shortly summarized, polished surfaces usually display a higher passivation due to the higher uniformity of the layers and a lower defect density at the interfaces which results in a longer minority carrier lifetime. Furthermore, p-type symmetric samples suffer from the higher diffusion of boron compared to phosphorous and the formation of boron-oxygen complexes [85].

By examining the results of Sections 4.2 and 4.3, one can observe different trends for the different symmetric samples. Hence, a trade-off for the fabrication of a solar cell has to be found. The differences in passivation depending on the exact annealing conditions for the polished n-type symmetric samples are relatively large. The passivation quality strongly decreases when the samples are annealed at 950 °C which most likely stems from the enhanced diffusion of phosphorous into the c-Si at higher temperatures. This effect lowers the field effect passivation and increases Auger recombination [85]. For the textured p-doped symmetric samples the optimal annealing conditions are 850 °C for 45 minutes. Thus, for a solar cell with a polished n-type contact and a textured p-type contact, a compromise has to be found. It was decided to move forward with the annealing conditions of 900 °C and 15 minutes since the differences in passivation for the textured p-doped symmetric samples at different annealing conditions are only about 5 mV which is relatively small.

For determining the optimal thickness of the silicon oxide passivating layer, Section 4.4

has to be taken into account as well. Dopant diffusion has to be sufficient to reach the interface but excessive dopant diffusion will reduce the field effect passivation. For the polished n-type symmetric sample, the highest iV_{OC} and minority carrier lifetime was observed for the 3 minute thermal oxidation sample. The textured p-type symmetric sample followed a similar trend for the lifetime curves even though the iV_{OC} was slightly higher for the sample with a thermal oxidation duration of 2 minutes.

In conclusion, for the fabrication of a polished n-type front/textured p-type rear solar cell the processing conditions for the thermal oxidation and the high temperature annealing were chosen to be 675 °C/3 minutes and 900 °C/15 minutes, respectively.

5

Single-side textured front-back contacted solar cell

In this chapter the fabrication of a single-side textured (SST), front-back contacted (FBC) polycrystalline silicon oxide (poly-SiO_x) solar cell is discussed. The structure is depicted in Figure 36. In Section 5.1, the processing procedure for the fabrication of the solar cell is described. The performance of the solar cell is examined and analyzed in Section 5.2. Furthermore, a double-side polished (DSP) and a double-side textured (DST) FBC solar cell were fabricated. The results are presented and compared with the SST single-junction solar cell in Appendix A.3.

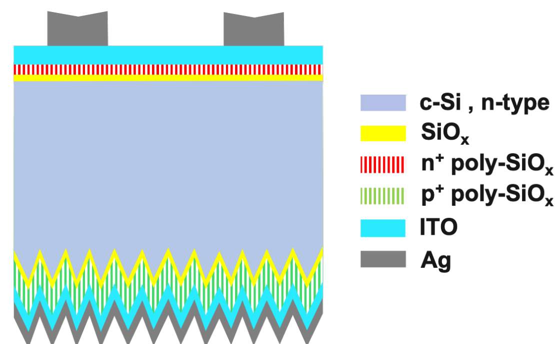


Figure 36: Schematic structure of single-side textured FBC solar cell.

5.1 Fabrication process of the single-junction solar cell

As the starting point, n-type float zone $< 100 >$ oriented silicon wafers with a diameter of 100 mm, a thickness of 280 μm (+/- 20 μm) and a resistivity of 1-5 Ω cm are utilised.

- To obtain single-side textured wafers, a 500 nm thick silicon nitride (SiN_x) layer is first deposited on one side to protect it against the texturing process. The wafers are then submerged into an aqueous Tetramethylammonium Hydroxide (TMAH) solution for 15 minutes at 85 °C. The solution consists of 4L of water, 1L of TMAH and 120ml of AlkaTex8. After the texturing step, the wafer is dipped into a solution of hydrofluoric acid (HF) and nitric acid (HNO_3) for two minutes to smoothen the tips of the pyramids. Finally, the single-side textured wafers are dipped into BHF to remove the protective SiN_x layer.

- To prepare the wafers for the depositions, they undergo a standard cleaning procedure to remove organic and inorganic contaminations. First, the wafers are immersed into a 99% HNO_3 solution for 10 minutes and then rinsed with deionised (DI) water for 5 minutes. Subsequently, the wafers are immersed into a 69.5% HNO_3 solution for 10

minutes at 110 °C and again rinsed for 5 minutes with DI water. This is followed by a Marangoni drying to remove the native oxide layer.

- Next, the ultra-thin silicon oxide (SiO_x) tunneling layer is deposited via dry thermal oxidation. The processing conditions for the dry thermal oxidation are 675 °C and 3 minutes. This is discussed in more detail in Section 4.5.

- To protect the SiO_x passivation layer, a 10 nm intrinsic amorphous silicon layer is deposited immediately afterwards in a low-pressure chemical vapor deposition (LPCVD) furnace with a silane flow rate of 45 sccm.

- The samples then again undergo a Marangoni drying to remove the native oxide layer to obtain a good contact between the intrinsic amorphous silicon (a-Si) and the doped amorphous silicon oxide (a-SiO_x) layers. A 20 nm n-doped a-SiO_x layer is then deposited on the polished side of while the 20 nm p-doped a-SiO_x layer is deposited on the textured side of the sample. The processing conditions are shown in Table 2.

Table 2: Final thickness and gas flow during the PECVD deposition of the doped a-SiO_x layers in sccm

Contact type	Thickness	SiH_4	CO_2	B_2H_6	PH_3	H_2
polished n-type	20 nm	4	6.4	-	4.8	35
textured p-type	20 nm	8	2	5	-	100

- Subsequently, the wafers are annealed at 900 °C for 15 minutes as discussed in Chapter 4 to crystallize the amorphous layers and activate the dopants for the diffusion from the doped to the intrinsic layer.

- To further improve the passivation quality of the sample a hydrogenation step is incorporated. This is done to passivate defects like dangling bonds at the interfaces. A 120 nm hydrogenated SiN_x layer is deposited via PECVD on both sides of the sample which is followed by forming gas annealing (FGA) for 30 min at 400 °C. During the annealing step the silicon nitride layer acts as a hydrogen source and the hydrogen diffuses into the previously deposited layers to passivate defects at the interface of the crystalline silicon and the SiO_x passivating layer. After the hydrogenation the SiN_x layer is etched away by a HF/BHF dip.

- Next, the transparent conductive oxide (TCO) is deposited via RF-Magnetron sputtering. A 75 nm and 150 nm thick layer is deposited on the front and rear side, respectively.

- To recover the passivation degradation due to the indium tin oxide (ITO) deposition, a TCO recovery annealing step at 400 °C in hydrogen environment for 1 hour is incorporated. This is discussed in more detail in section 6.1.

- The silver (Ag) metal contacts are applied via screen printing utilizing a mask with an area of 4 cm^2. After that, the wafers are annealed at 170 °C in ambient air for 30 minutes.
- Finally, a post metallization annealing is applied at 250 °C for 5 minutes to improve the contact formation. The front and rear side of the solar cell are shown in Figure 38.

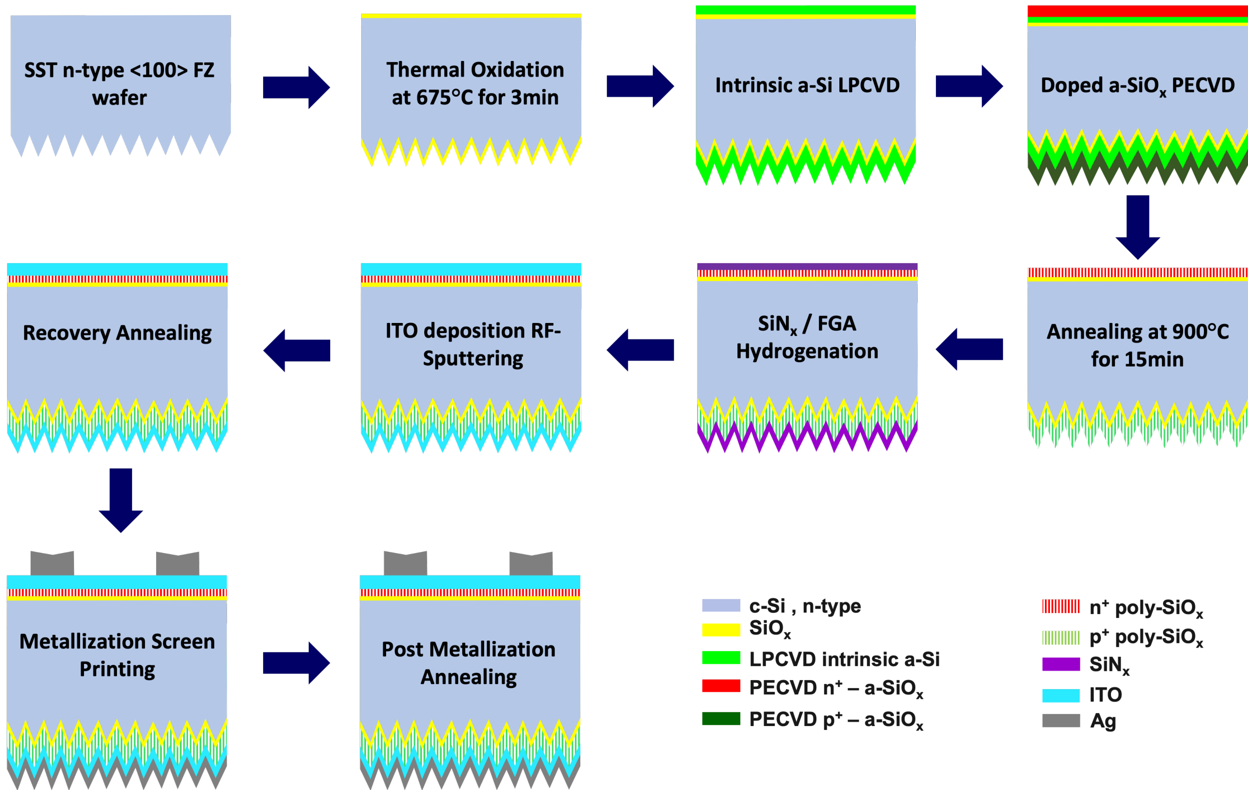


Figure 37: Fabrication process of a FBC single-junction solar cell.

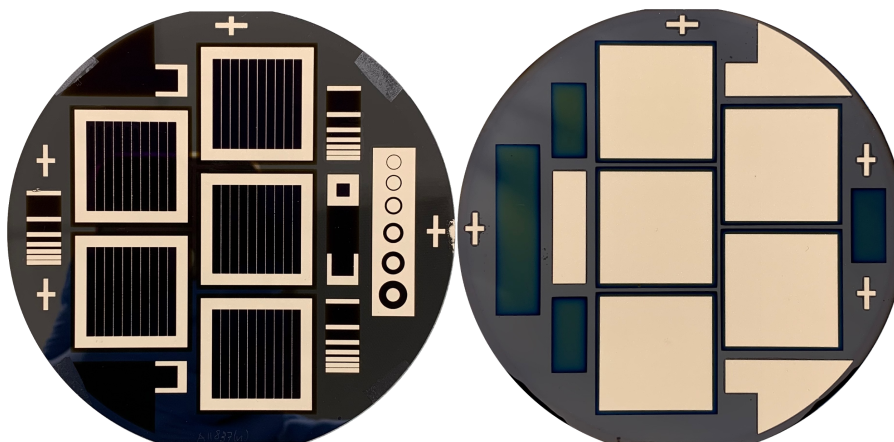


Figure 38: The front (left) and rear (right) side of the single-junction FBC solar cell.

5.2 Results

In this section the results of the single-side textured FBC solar cells will be discussed. The final structure is depicted in Figure 36. The solar cell consists of a SST n-type wafer which is passivated on both sides by a SiO_x layer. It utilizes ITO as a TCO on both sides and the silver electrodes are applied via screen printing. The change in passivation after every processing step is depicted in Figure 39. After the annealing process and the hydrogenation step, the sample displays an iV_{OC} of 664 mV and 690 mV, respectively.

In Chapter 4, the iV_{OC} of the polished n-type and textured p-type symmetric lifetime sample was measured to be 745 mV and 670 mV, respectively. Thus, it can be deduced that if the contribution to the iV_{OC} of the n-doped and p-doped contacts was equal, the iV_{OC} of the SST solar cell should be above 700 mV. However, the iV_{OC} of the fabricated solar cell is only about 690 mV after hydrogenation. From this we can infer that the textured p-type contact plays a disproportionately high role in the iV_{OC} of the solar cell. The ITO deposition strongly degrades the passivation from 690 mV to 664 mV again. This is expected due to the damages from the high-energy particles colliding with the sample during the sputtering process [127, 128]. Lastly, the TCO recovery annealing step as described in Section 3.1.9 only increases the implied open-circuit voltage by 7 mV to a value of 671 mV. Previously, the TCO recovery annealing has proven more effective for n-type textured/p-type polished samples and researchers were able to restore the level of iV_{OC} before the ITO deposition [140]. The TCO recovery annealing also recovered the sputtering damage for double-side polished solar cells fabricated in this project. The results are shown in Appendix A.3. Hence, it is believed that the p-type textured poly-SiO_x contact is the reason for the ineffectiveness of the TCO recovery annealing at 400 °C for the n-type polished/p-type textured solar cell discussed in this chapter.

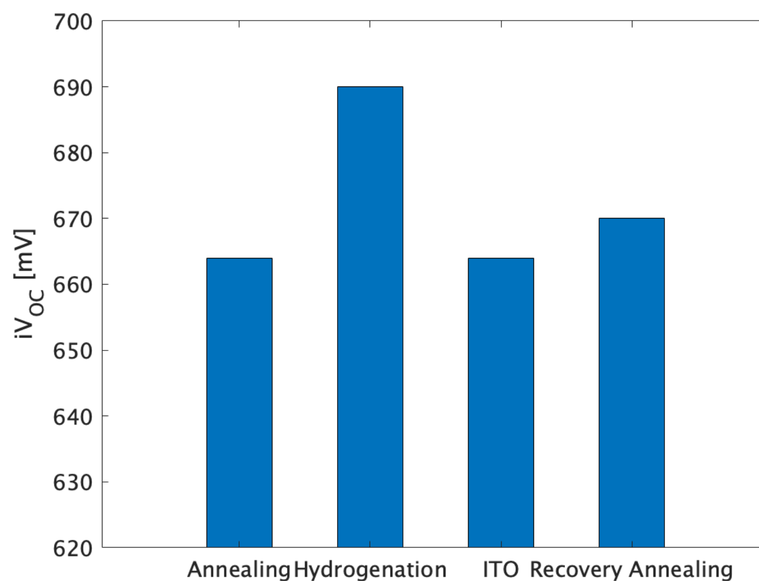


Figure 39: Measured iV_{OC} of the solar cell after every processing step.

The effect of the TCO recovery annealing can also be observed in Figure 40. Here, the minority charge carrier lifetime is depicted vs. the injection level. As expected, the minority charge carrier lifetime increases upon hydrogenation due to the chemical passivation of the interface defects and decrease because of the sputtering damage from the high-energy particles. However, the lifetime further decreases after the TCO recovery annealing process which is not expected. As just mentioned, the textured p-type poly-SiO_x contact could be the cause. This could originate from a lower thermal stability of the textured surface which leads to an enhanced diffusion of boron [12, 85, 143, 144]. A possible solution to this problem is to choose a lower recovery annealing temperature and/or time to reduce dopant diffusion and lower the defect formation in the solar cell. This will be further discussed in Section 6.1.

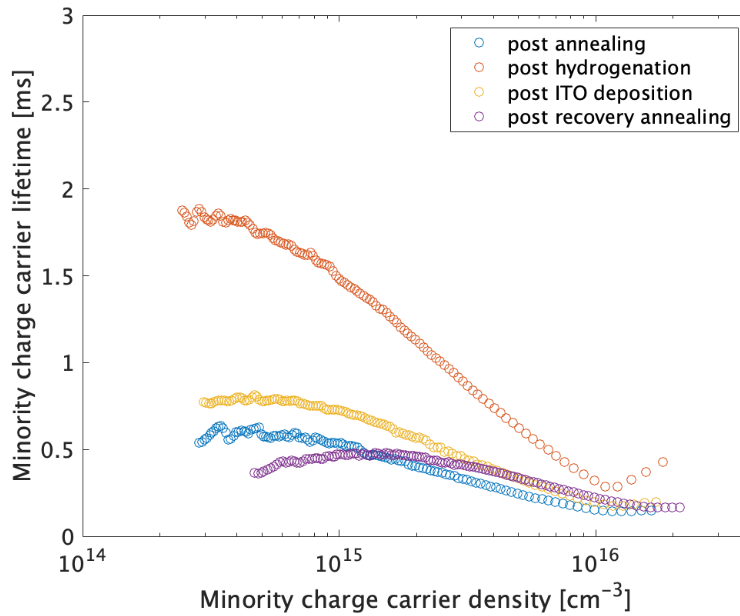


Figure 40: Minority charge carrier lifetime vs. minority charge carrier density of the solar cell after every processing step.

The results from the JV-curve measurements after screen printing and after the post metallization annealing are shown in Figure 41. The post metallization annealing refers to an annealing step at 250 °C for 5 minutes as described in Section 3.1.10 after the metallization. The final solar cell exhibits an efficiency of 16.67 % with an open-circuit voltage (V_{OC}) of 649 mV, a short-circuit current density (J_{SC}) of 34.28 mA/cm^2 and a fill factor (FF) of 74.93 %. One can observe that the screen printing leads to a decrease in open-circuit voltage of about 20 mV compared to the iV_{OC} after the TCO recovery annealing. This is due to the formation of defects at the ITO/Ag interface and the diffusion of silver atoms into the ITO bulk upon annealing the metal electrode [19]. Furthermore, it has been shown that a post metallization annealing can improve the short-circuit current density and the fill factor of solar cells by reducing the contact resistivity at the interface and the lateral resistivity of the electrodes [145]. This improvement takes place due to the enhanced evaporation of binder in the silver paste and increased sintering and densification at higher temperatures and hence improved contact formation. The effect is also visible for the solar cells fabricated in this project. The fill factor and J_{SC} increase by 2.87% and 1.21 mA/cm^2, respectively.

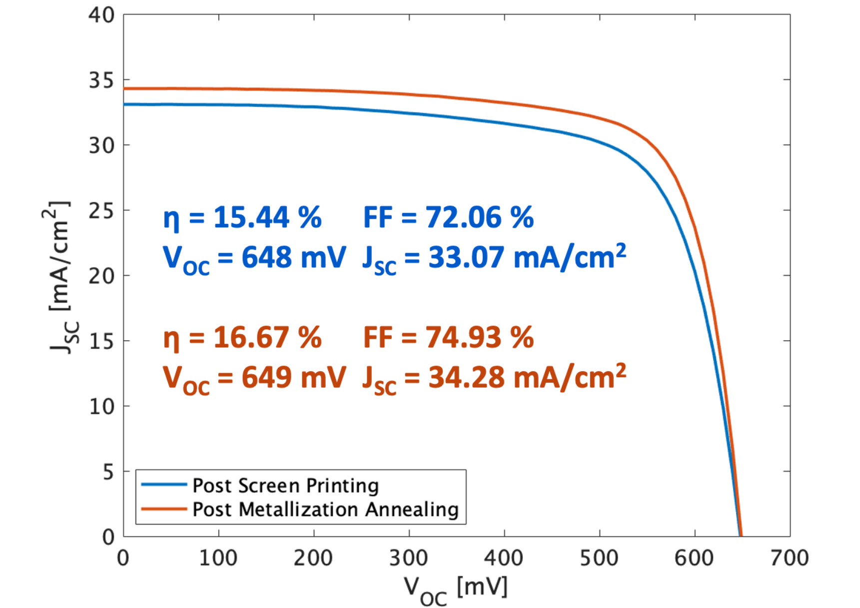


Figure 41: Comparison of the J-V curves of the single-junction FBC solar cell after screen printing (blue) and after the post metallization annealing (orange).

In Table 3 the results from the Wacom J-V and SunsVoc measurement are given. One can notice that there is especially a big difference between the measured fill factor and the pseudo fill factor. The reason for this can be a high series resistance (R_S) due to various factors like a too thick silicon oxide SiO_x passivating layer which would hinder the tunneling mechanism or the contact with the TCO layer. The series resistance can be calculated according to Equation 24 presented in Section 3.2.5 and is also given in Table 3. A series resistance of 0.76 Ω cm^2 is relatively high which also explains the large difference between the FF and the pFF [86]. Contact resistivity measurements can be performed to potentially find the reason for the high R_S.

Table 3: Comparison of J-V curve and SunsVoc measurement including pseudo fill factor (pFF), pseudo V_{OC} (pV_{OC}), pseudo efficiency ($p\eta$) and the calculated series resistance (R_S)

Method	Area [cm^2]	J_{SC} [mA/cm^2]	V_{OC}/pV_{OC} [mV]	FF/pFF [%]	$\eta/p\eta$[%]	R_S [Ωcm^2]
Wacom J-V	4	34.28	649	74.9	16.7	-
SunsVoc	4	-	665	80.7	18.4	0.76

In Figure 42, the external quantum efficiency (EQE) and the reflection of the fabricated solar cell are plotted. One can observe high reflection losses at the higher wavelength range (600-1000 nm) which limits the absorption and hence the current density of the solar cell. Parasitic absorption losses in the emitter layers and the TCO reduce the solar cell performance especially at wavelengths below 600 nm and above 1000 nm. The optical losses are discussed in more detail in Section 6.5.

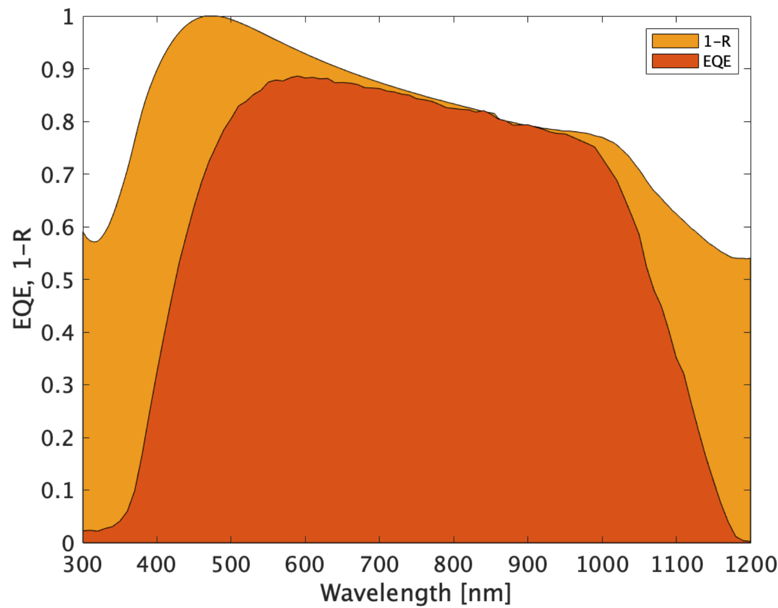


Figure 42: The results of the EQE and reflection measurement of the FBC single-junction solar cell.

5.3 Summary

A single-junction FBC poly-SiO_x solar cell has been fabricated. A maximum iV_{OC} of 690 mV has been achieved after the hydrogenation process. The iVoc was reduced by 26 mV due to the sputtering damage during the ITO deposition. A recovery annealing step at 400 °C after the TCO deposition restored 7 mV and was even detrimental for the minority charge carrier lifetime. A final device efficiency of 16.67 % was achieved with a fill factor of 74.93 %, a V_{OC} of 649 mV and a J_{SC} of 34.28 mA/cm^2. From the reflection measurement it can be observed that the reflection losses limit the solar cell performance between 600 - 1000 nm while parasitic absorption affects the performance at lower and higher wavelengths.

6

Further analysis of the front-back contacted solar cell

This chapter focuses on further enhancing the performance of the solar cell fabricated in the previous chapter. First, the TCO recovery annealing is discussed in Section 6.1. Next, in Section 6.2 the influence of the p-doped polycrystalline silicon oxide (poly-SiO$_x$) thickness is examined. In Sections 6.3 and 6.4 an additional annealing step after the deposition of the amorphous silicon (a-Si) layer and different transparent conductive oxide (TCO) schemes are investigated, respectively. Finally, optical simulations are carried out to analyze the optical performance of the solar cell in Section 6.5.

6.1 TCO recovery annealing

As already mentioned in Section 3.1.9, the TCO recovery annealing after the indium tin oxide (ITO) deposition aims to minimize the effective sputtering damage. The impact of high-energy particles during the sputtering process generates defects in the crystal structure which can be cured by thermal annealing which (partially) restores the passivation quality of the device [128]. This post TCO recovery annealing does not only influence the passivation quality but also the contact resistivity and sheet resistance of the TCO layer. Studies on the annealing effect after the TCO sputtering deposition for polycrystalline silicon (poly-Si) TOPCon solar cells have been done which use relatively high annealing temperatures between 350-500°C [129, 130]. However, Figure 39 and Figure 40 in Chapter 5 show that the applied annealing method in this project at 400°C for 60 min in hydrogen only recovers a few mV of passivation and even has a negative effect on the minority charge carrier lifetime. Previous work done at the PVMD group at TU Delft showed that a TCO recovery annealing at 400 °C for 60 minutes can almost fully restore the passivation degradation suffered during the ITO deposition process for a textured n-type/polished p-type FBC solar cell [140].

Table 4: Different processing conditions for the TCO recovery annealing experiment for the six samples and the reference sample (Sample 7)

Sample	Temperature [°C]	Time [min]	Ambient Atmosphere
1	150	5	Air
2	150	15	Air
3	200	5	Air
4	200	15	Air
5	250	5	Air
6	250	15	Air
7	400	60	H_2

However, this is not observed for a polished n-type/textured p-type FBC solar cell in this project. The main difference between the two solar cells is the surface morphology of the n-type and p-type contacts. Textured surfaces can exhibit lower uniformity and higher defect densities [12]. The introduction of the textured p-type poly-SiO_x layer could limit the effect of the TCO recovery annealing. It is theorized that the implementation of the textured p-type poly-SiO_x layer introduces more diffusion pathways for the dopants in the p-layer. This would lead to enhanced dopant diffusion into the bulk and the formation of boron-oxygen complexes which act as recombination centers for the charge carriers [20, 143, 144]. The diffusion and defect formation could be decreased by a lower thermal annealing budget, i.e. a reduction in temperature and time during the annealing process. Hence, a series of annealing experiments were carried out on single-side textured solar cells after the ITO deposition. A detailed overview of the exact processing conditions during the experiments can be found in Table 4. All samples are FBC solar cells which are processed until the TCO deposition. The fabrication process is described in Chapter 5. Samples 1-6 are annealed between 150 and 250 °C for 5 or 15 minutes in air while sample 7 acts as a reference sample and is annealed at 400 °C for 60 minutes in hydrogen. The results of the annealing experiment are depicted in Figure 43. The vertical axis displays the percentage of iV_{OC} that was recovered during the TCO recovery annealing compared to the total sputtering damage. On the horizontal axis the 6 different samples are shown in terms of their annealing temperature and as mentioned before, sample 7 acts as a reference sample with the current annealing method. The color of the bars represents the annealing duration.

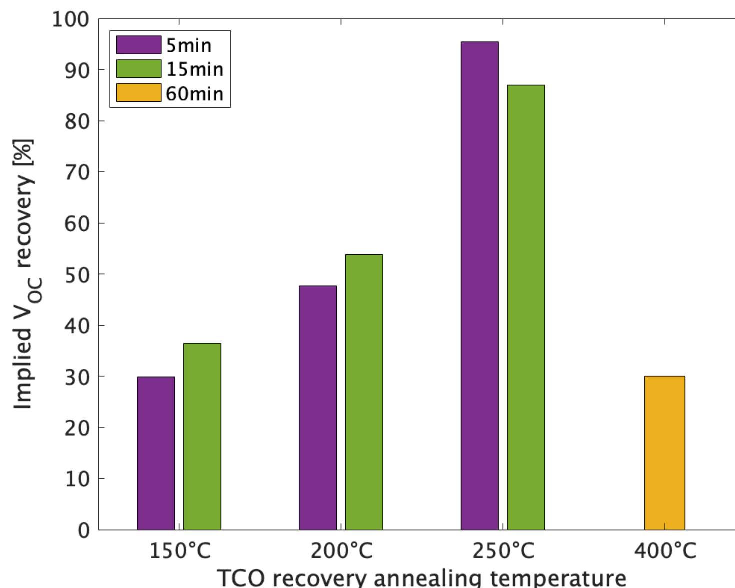


Figure 43: Passivation recovery in percent of the total sputtering damage for the different annealing conditions compared to the standard annealing process depicted in yellow.

According to the experimental series the maximum iV_{OC} recovery of 95% was achieved at an annealing temperature of 250 °C and 5 minutes. At lower temperatures the annealing might not have a big enough curing effect on the defects induced by the sputtering. If the annealing temperature is too high, the defect formation and dopant diffusion might increase

which promotes recombination and lowers the field effect passivation [86, 87].

Implementing the recovery annealing at 250 °C and 5 minutes into the single-side textured FBC solar cell fabrication process and comparing it with the previous annealing conditions at 400 °C and 60 minutes, we can observe an improvement in iV_{OC} after the annealing step in Figure 44. Even though the solar cell which is annealed at 250 °C, depicted in orange, exhibits a slightly lower iV_{OC} throughout the entire fabrication process it clearly outperforms the solar cell annealed at 400 °C, which is depicted in blue, after the TCO recovery annealing.

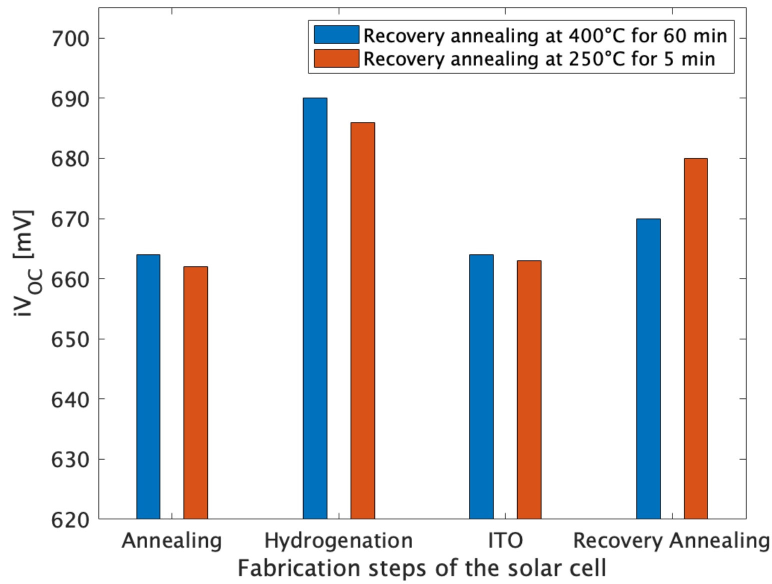


Figure 44: Comparison of the change in iV_{OC} after every processing step for two almost identically fabricated FBC solar cells. The only difference are the processing conditions during the TCO recovery annealing. The color of the bars denotes the temperature and time during the TCO recovery annealing process.

Moreover, the minority charge carrier lifetime also increases with the new TCO recovery annealing conditions of 250 °C for 5 minutes. The minority charge carrier lifetime for every fabrication step is shown in Figure 45. The blue curve depicts the lifetime after the high temperature annealing. As expected, the lifetime strongly increases upon the hydrogenation of the sample which can be observed in the orange curve. Subsequently, the ITO is deposited and the lifetime reduces again which is depicted in yellow. The two different TCO recovery annealing conditions can be compared which are depicted in purple with two different symbols. During the recovery annealing at 400 °C, the minority charge carrier lifetime barely improves at a higher injection level and even deteriorates at a minority charge carrier density below 10^{15} per cm^3, while an increase in lifetime over the entire wavelength range can be observed after the improved TCO recovery annealing at 250 °C.

In Figure 46, the J-V curves of the solar cells with the different TCO recovery annealing conditions are shown. The J-V curve depicted in blue corresponds to the solar cell with a TCO recovery annealing at 400 °C for 60 minutes. The device exhibits an efficiency of 16.67 %, a fill factor of 74.93 %, a V_{OC} of 649 mV and a J_{SC} of 34.28 mA/cm^2. The orange J-V curve corresponds to the solar cell with a TCO recovery annealing at 250 °C for 5 minutes. This

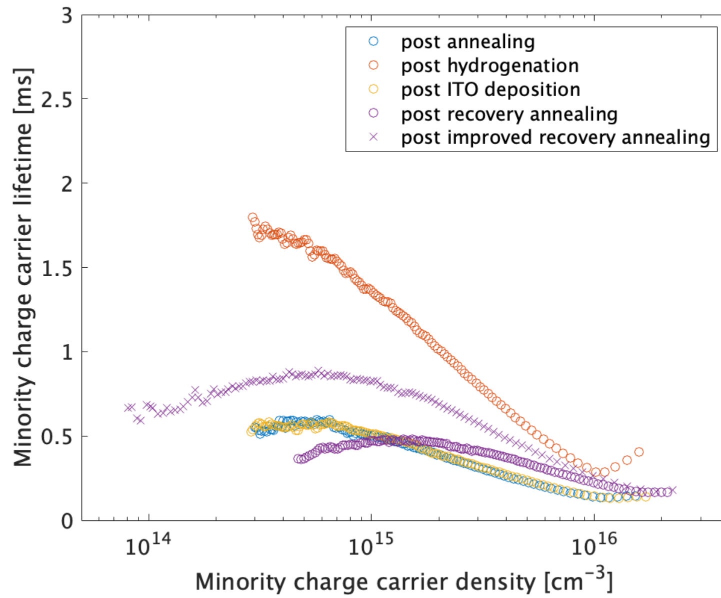


Figure 45: Minority charge carrier lifetime vs. minority charge carrier density after every processing step. The TCO recovery annealing at 400 °C is compared with the improved TCO recovery annealing at 250 °C.

device exhibits an efficiency of 18.76 %, a fill factor of 78.90 %, a V_{OC} of 664 mV and a J_{SC} of 35.81 mA/cm^2. The open-circuit voltage improves by 15 mV in the final device which further reassures the theory that the lower annealing temperature might decrease the defect density and enhances the passivation quality. This effect seems to indirectly also influence the carrier extraction and the interface resistance which can be seen in the simultaneous improvement of the short-circuit current density (J_{SC}) and the fill factor by 1.53 mA/cm^2 and 3.89%, respectively. Overall the efficiency increases from 16.67 % to 18.76 % with the new annealing conditions. Hence, from here on the new annealing scheme at 250 °C and 5 minutes will be implemented in all solar cells.

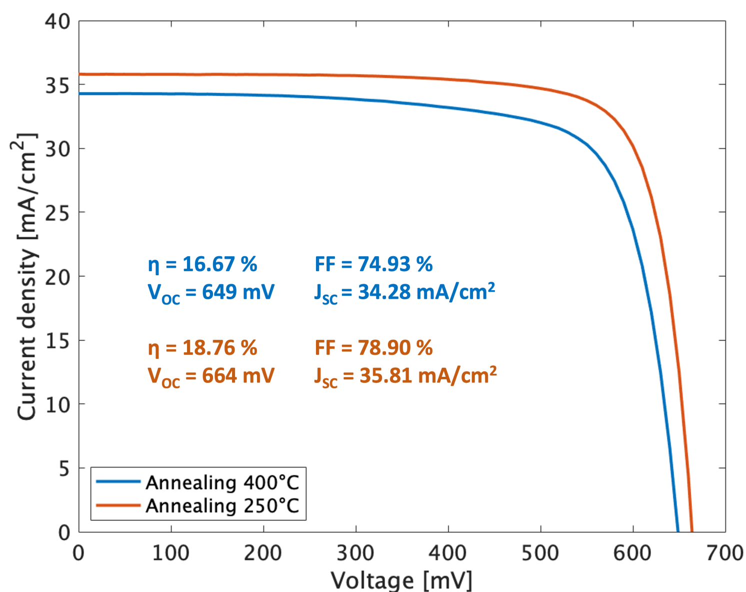


Figure 46: J-V curves of the initial solar cell with the TCO recovery annealing at 400 °C (blue) as fabricated in Chapter 5 and the solar cell with the improved TCO recovery annealing at 250 °C (orange).

In Figure 47, the external quantum efficiency (EQE) curve of the solar cell with a TCO recovery annealing at 400 °C is shown in blue while the EQE of the solar cell with the improved TCO recovery annealing at 250 °C is shown in orange. It can be observed that there is a clear increase in EQE with the improved annealing conditions over the wavelength range from 500 - 1200 nm. This could be due to an enhanced carrier extraction and reduced interface reflection due to the lower defect density and formation of other phases like oxygen-boron complexes. A similar trend can be observed in the reflection measurement as displayed in Figure 48. The sample with the improved annealing scheme at 250 °C exhibits reduced reflection losses in the wavelength range between 500 to 1150 nm. Hence, the enhanced J_{SC} might be a combination of improved carrier extraction due to reduced recombination and a reduction in reflection losses. The improvement in fill factor might stem from the reduced defect density at the interfaces [146].

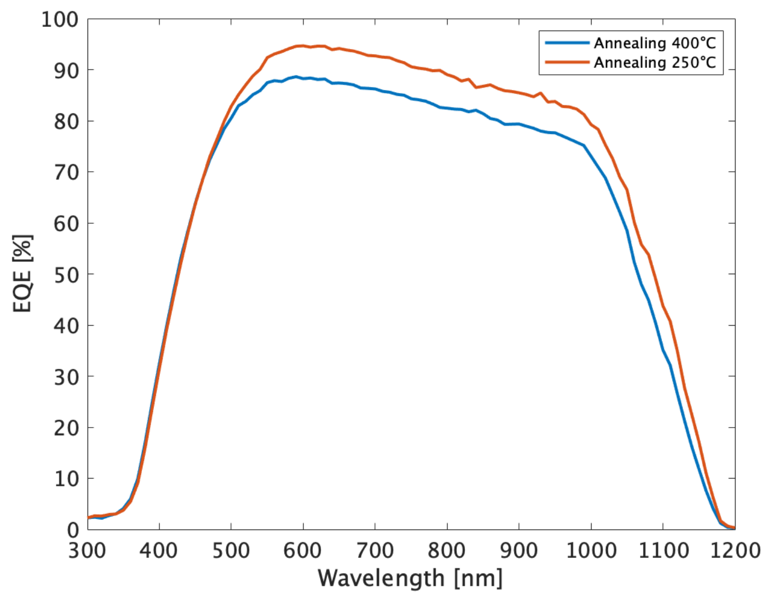


Figure 47: Comparison of the EQE curves of the initial solar cell with the TCO recovery annealing at 400 °C (blue) as fabricated in Chapter 5 and the solar cell with the improved TCO recovery annealing at 250 °C (orange). The sample with the improved TCO recovery annealing exhibits an improved EQE between 450 and 1150 nm.

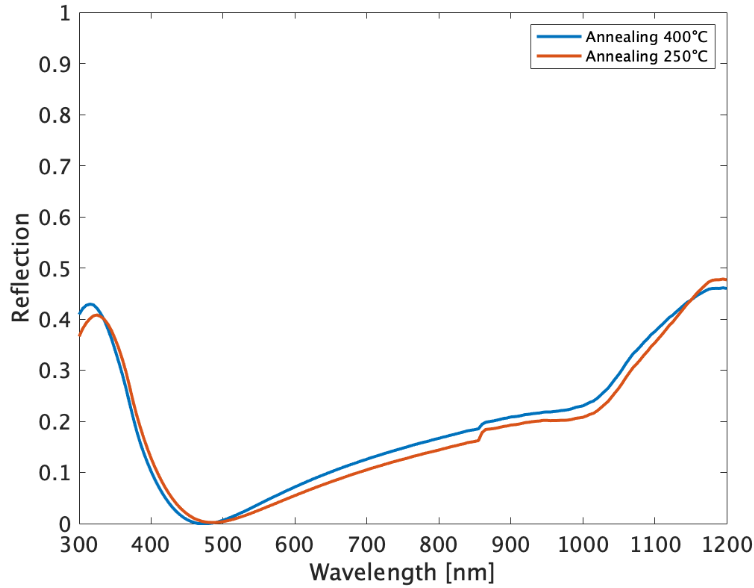


Figure 48: Comparison of the reflection of the initial solar cell with the TCO recovery annealing at 400 °C (blue) as fabricated in Chapter 5 and the solar cell with the improved TCO recovery annealing at 250 °C (orange). The sample with the improved TCO recovery annealing exhibits a reduced reflection between 500 and 1150 nm.

6.2 Variation of the p-doped poly-SiO_x layer thickness

A second method to reduce the sputtering damage and preserve the passivation properties of the device is altering the thickness of the doped poly-SiO_x layer. An change in sputtering damage has been observed in literature for poly-Si contacts with different thicknesses [130]. The doped layer acts as a protective buffer layer. In this section, the thickness variation of the p-type textured amorphous silicon oxide (a-SiO_x) layer, which is deposited by PECVD, is examined. Furthermore, it is possible to change the thickness of the intrinsic a-Si layer which also influences the passivation quality of the solar cell. This was investigated for textured p-type symmetric samples and the results are presented in Appendix A.4. The structure of the four different samples is given in Table 5. The standard structure utilised in the solar cells previously discussed corresponds to Sample 2.

Table 5: Overview of the structure of the p+ doped contact of the samples. The a-Si layer stays constant while the p+ a-SiO_x layer is varied. The last column describes the total thickness of the p+ poly-SiO_x layer after the crystallization.

Sample	a-Si [nm]	p+ a-SiO_x [nm]	p+ poly-SiO_x [nm]
1	10	15	25
2	10	20	30
3	10	25	35
4	10	30	40

In Figure 49, the iV_{OC} results of the quasi steady-state photoconductance (QSSPC) measurement after every processing step are presented. It can be observed that the passivation properties are relatively stable across all for samples after the crystallisation and hydro-

genation step. There is a slight increase in iV_{OC} with a thinner doped layer. This could be related to the change in oxygen concentration due to the lower a-Si/a-SiO_x thickness ratio. However, the most interesting observation is the difference in passivation after the ITO deposition. It is clearly visible that a thinner p-doped a-SiO_x negatively affects the passivation quality of the device. Sample 1 shows a decrease in passivation of more than 40 mV while the iV_{OC} of samples 3 and 4 with the thicker p-doped poly-SiO_x layer only decreases by about 10 mV. Sample 2 exhibits sputtering damage of about 25 mV. This trend can be explained by the fact that the thinner the layer is, the more severe the induced sputtering damage. The doped poly-SiO_x layer acts as a protective barrier from the high-energy particles during the ITO deposition [127, 128, 131]. A thinner layer results in more ruptured bonds and a higher defect density which directly influences the recombination and passivation properties of the solar cell. There seems to be a limit to reducing the sputtering damage since the passivation degradation of sample 3 and 4 are almost identical. However, as already discussed in much detail in the previous section, the damage can also be recovered by a thermal annealing step which can (partially) restore the damaged crystal structure. From the annealing process, a higher passivation recovery is expected for the samples with a thinner poly-SiO_x layers since the sputtering process induces a higher total damage to the thinner samples. This behaviour can be observed after the recovery annealing in Figure 49. Sample 1 recovers about 25 mV which corresponds to a percental recovery of just above 50% while samples 3 and 4 recover about 8-10 mV which is closer to a full recovery. This could indicate that the rupture of different bonds (i.e. Si-Si or Si-H) respond differently to the recovery annealing [128]. In conclusion, a thicker doped poly-SiO_x layer can potential reduce the sputtering damage during the ITO deposition.

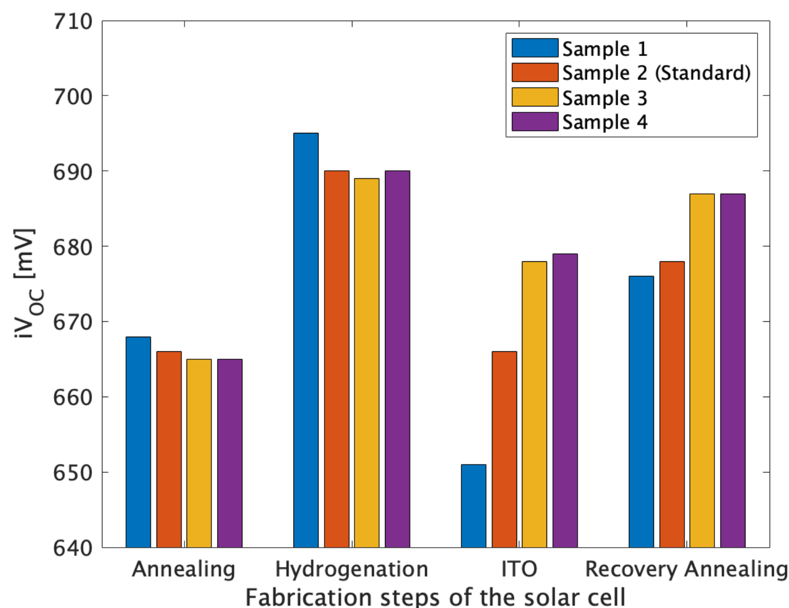


Figure 49: The change in iV_{OC} for the different samples with different poly-SiO_x layer thicknesses after every processing step.

In Figure 50, the results of the J-V measurements of the solar cells with different p+ poly-

SiO_x layer thicknesses are presented. For every thickness 5 samples have been fabricated which are displayed for every parameter. As shown in the top left, the open-circuit voltage follows the same trend as with the QSSPC measurement. The highest V_{OC} is observed for the samples with a thicker emitter layer. One the other hand, the short-circuit current density is reduced for the thicker samples. This probably results from an enhanced parasitic absorption. However, sample 1 also displays a slightly lower J_{SC} compared to the standard thickness. This might be related to a higher defect density and recombination which can influence the carrier extraction. The fill factor displays deviations for the second sample. The influence of the layer thickness seems to cancel out since an increase in thickness also enhances the V_{OC} but reduces the J_{SC}. Therefore, the median efficiency is almost identical at about 17.5 % for all samples. Hence, it was decided to not vary the thickness of the p-doped poly-SiO_x layer in the following experiments.

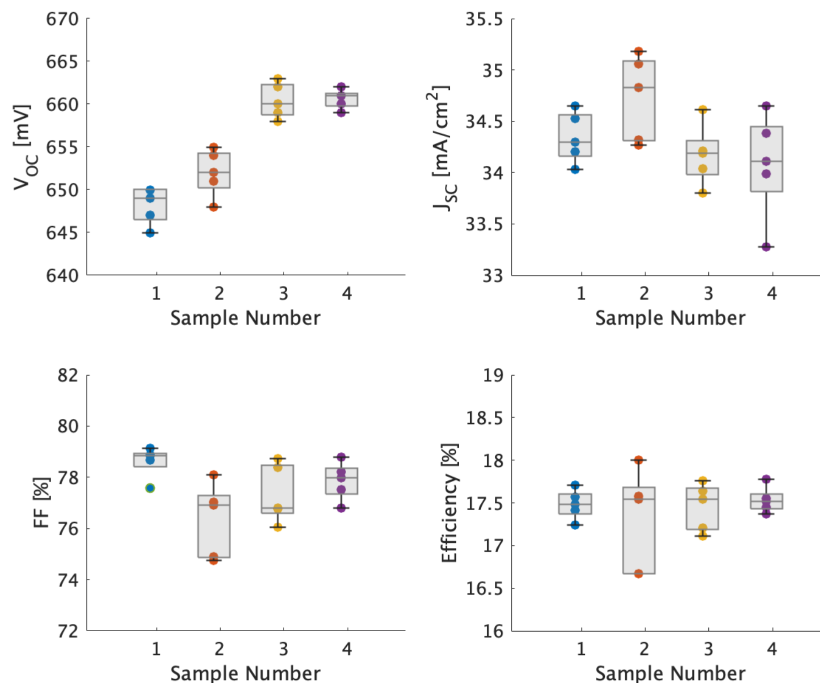


Figure 50: The V_{OC}, J_{SC}, fill factor and efficiency of solar cells with different p+ poly-SiO_x layer thicknesses as measured with a J-V setup. 5 solar cells were fabricated for every sample.

6.3 Two-step annealing scheme

Previous experiments have shown that the introduction of an extra annealing step after the deposition of the a-Si layer at 950 °C for 1 minute, can improve the passivation quality of poly-SiO_x solar cells after the crystallization annealing [140]. Hence, an experimental series has been conducted to investigate if this approach can potentially enhance the V_{OC} of the single-junction FBC solar cell fabricated in this work. A schematic overview of the relevant fabrication steps is displayed in Figure 51 with the annealing step being introduced after the a-Si deposition. Previously, annealing at 950 °C for 1 minute achieved an increase of 20 mV for textured p-type poly-SiO_x lifetime samples. Hence, temperatures between 900

and 1000 °C were chosen to investigate the effect. The different processing conditions are summarized in Table 6 with sample 1 being a reference sample without an extra annealing step. Sample 2-4 are annealed in a horizontal Tempress furnace between 900 to 1000 °C. The ramping rates for the Tempress furnace were 10 °C per minute starting at 600 °C. On the other hand, sample 5 was annealed in a rapid thermal processing (RTP) setup at 950 °C for 1 minute.

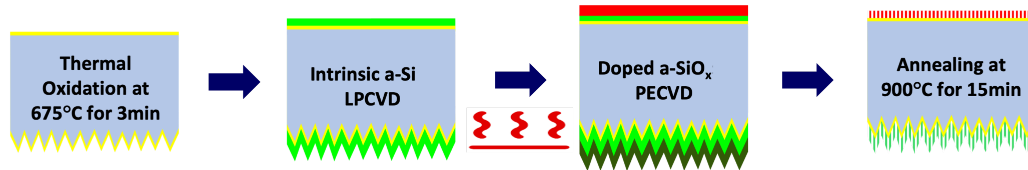


Figure 51: Fabrication steps of the single-junction FBC solar cell from the thermal oxidation until the high temperature annealing. An extra annealing step is incorporated between the deposition of the a-Si and the doped a-SiO$_x$ depositions.

Table 6: Overview of the different samples for the two-step annealing study. Sample 1 acts as a reference sample and does not have an extra annealing step incorporated

Sample	Furnace Type	Temperature [°C]	Time [min]
1	-	-	-
2	Tempress	900	1
3	Tempress	950	1
4	Tempress	1000	0.5
5	RTP	950	1

The change in passivation after the various processing steps from this experimental series is presented in Figure 52. It can be observed that the passivation of sample 4 and 5 is slightly higher after the high temperature annealing step. This could also just be an artefact of the process variability. However, after the hydrogenation step, sample 1 without any additional annealing step exhibits the highest iV_{OC}. The extra annealing step even seems to be detrimental for the passivation quality after hydrogenation for sample 2 and 3 compared to the reference sample. This might be related to a higher degree of crystallization of the a-Si and reduced dopant diffusion which also reduces the hydrogen diffusion [147, 148]. This hinders the passivation of dangling bonds at the interface. This would also explain the reduced sputtering damage to those samples since the total number of passivated defects is reduced and hence the sputtering damaged is limited. Following the ITO sputtering deposition all samples except for sample 4 practically exhibit the same passivation with samples 1 and 5 outperforming the other samples during the TCO recovery annealing. Sample 5 generally displays a similar behaviour compared to the reference sample which is plausible since RTP is defined by a very fast ramping which reduces the diffusion and crystallisation potential of the material and is thus most similar to the standard process without additional annealing step. The reason why sample 4 exhibits a higher sputtering damage is not clear. It might be related to the increased thermal degradation of the SiO$_x$ tunneling layer at those high processing temperatures and the corresponding enhanced defect formation [82, 83].

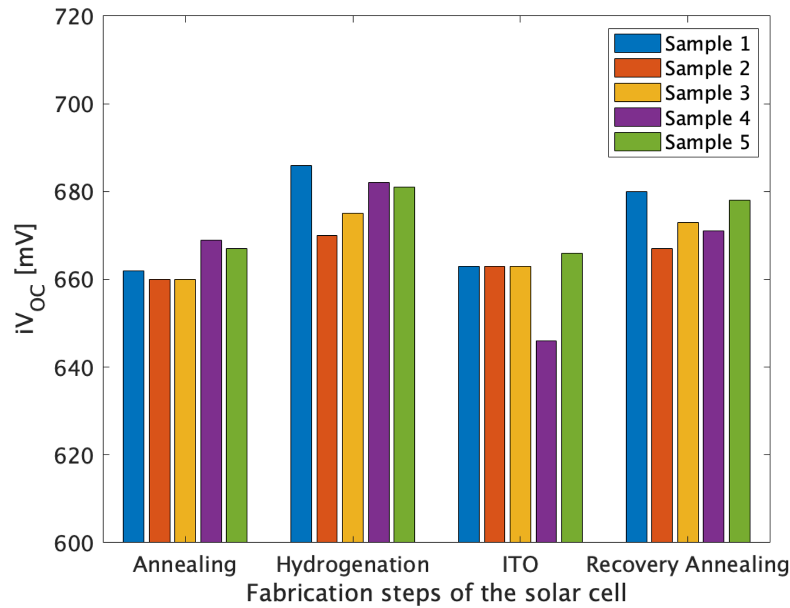


Figure 52: Development of the iV_{OC} after every processing step comparing the 5 samples with the varying annealing schemes.

The results of the J-V measurements of the solar cells are displayed in Figure 53. Most noticeable is the lower V_{OC} of sample 2 and 3. Previously, an increase in V_{OC} has been observed. However, it seems that the additional annealing step has a negative impact on the passivation quality, especially for Sample 2 and 3. Interestingly, the two-step annealing has a positive influence on the J_{SC}, displaying an optimum for the third sample which exhibits a short-circuit current density of almost 36 mA/cm^2. However, we do not observe an overall improvement in efficiency.

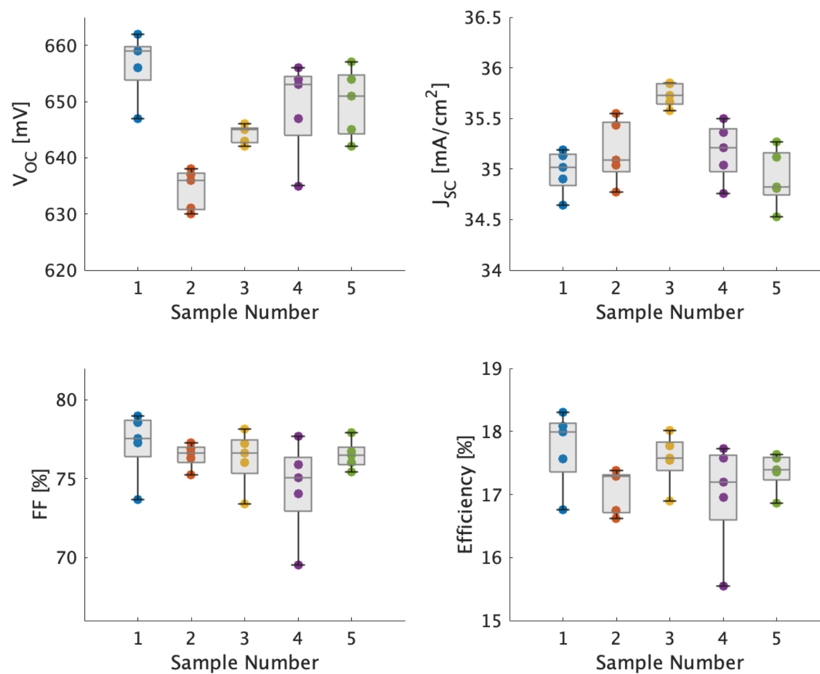


Figure 53: The V_{OC}, J_{SC} , fill factor and efficiency of solar cells with different annealing schemes as measured with a J-V setup. 5 solar cells were fabricated for every sample.

6.4 Different TCO schemes

In this project, ITO is used as the standard TCO layer. However, tungsten-doped indium oxide (IWO) is also sometimes utilized as a TCO in solar cells because it potentially has a higher charge carrier mobility and lower absorption coefficient over the relevant wavelength range [72]. A lower absorption coefficient could theoretically decrease parasitic absorption in the TCO layers and improve the current density in the device. The series resistance is also decreased due to the higher charge carrier mobility. This stems from a better screening of the effective charge of tungsten in indium oxide compared to tin. Thus, the dopants scattering power is reduced. Furthermore, a higher degree of crystallinity can be achieved due to similar atomic radii of tungsten and indium [72]. This can lead to an improved J_{SC} and fill factor when applying IWO in a solar cell instead of ITO. To investigate the effect of IWO instead of ITO in a solar cell, different architectures were fabricated. Samples with an IWO layer at the front and a ITO layer at the rear (IWO/ITO) and samples with an IWO at the front and rear (IWO/IWO) were fabricated. Moreover, a solar cell without rear ITO was fabricated. By eliminating the TCO on the rear side the sputtering damage on the textured p-type contact can be avoided which could improve the passivation quality. However, this can affect the back reflection into the absorber material and the series resistance. The standard solar cell with an ITO at the front and rear side (ITO/ITO) is also fabricated as a reference sample. The four different structures are shown in Figure 54.

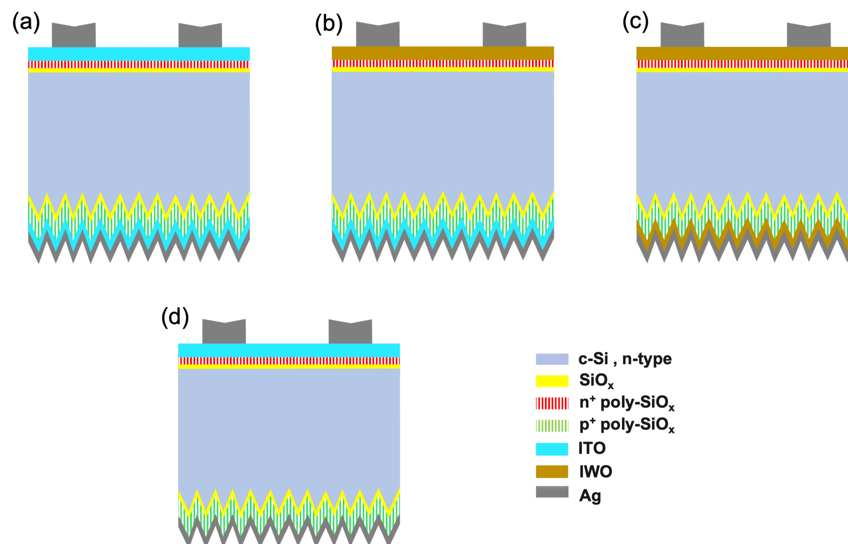


Figure 54: The architecture of the four different structures: ITO/ITO (a), IWO/ITO (b), IWO/IWO (c) and no rear ITO (d).

In Figure 55, the passivation properties of the different samples after every processing step are displayed. The samples are prepared identically until the TCO deposition. We observe that the passivation after the hydrogenation step varies by almost 15 mV between the samples. The reason for this might be the deposition of the SiO_x where minuscule deviations can decisively alter the thickness which influences the interface quality and the defect density. Furthermore, uniformity issues during the deposition of the a-SiO_x and the high temperature annealing process are also possible reasons for this process variability. As ex-

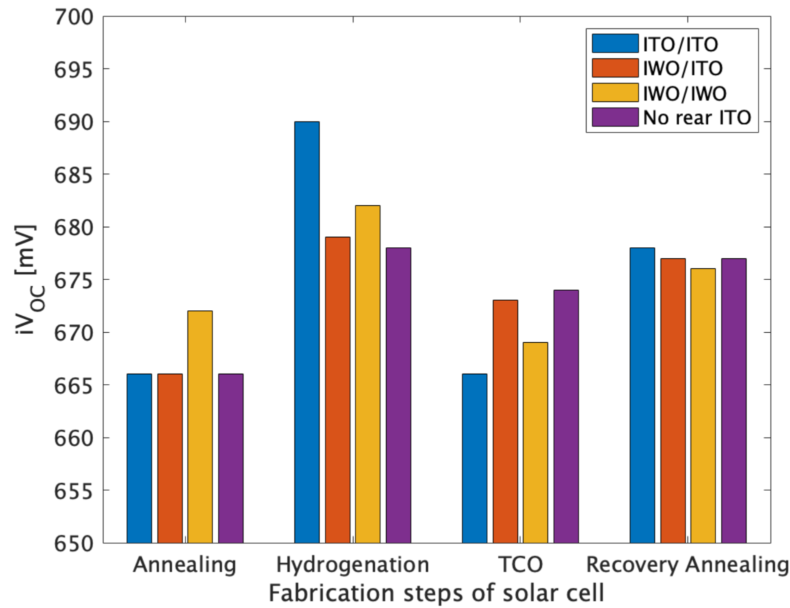


Figure 55: The change in iV_{OC} after every processing step for the different TCO designs. The samples have TCO at the front and rear (ITO/ITO), IWO at the front and ITO at the rear (IWO/ITO), IWO at the front at rear (IWO/IWO) and no ITO at the rear.

pected, the sample without rear ITO displays the smallest sputtering damage of all samples because the TCO was only deposited on one side. The two samples with IWO also display a reduced sputtering damage which probably also stems from the fact that the gain in hydrogenation was smaller compared to the ITO/ITO sample. However, after the recovery annealing the iV_{OC} of all samples is between 675 and 680 mV.

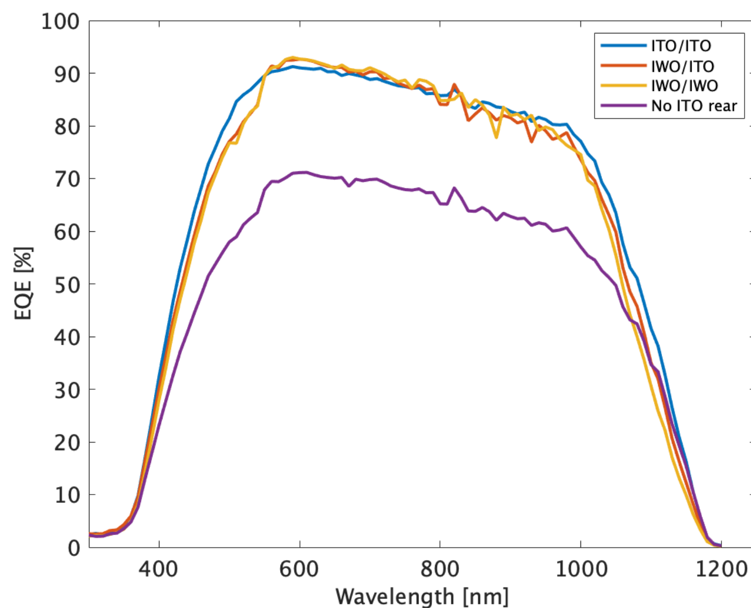


Figure 56: Comparison of the EQE curves of the solar cells with different TCO designs. The samples have TCO at the front and rear (ITO/ITO), IWO at the front and ITO at the rear (IWO/ITO), IWO at the front at rear (IWO/IWO) and no ITO at the rear.

In Figure 56, the EQE curves of the samples are compared. The most striking difference is the low EQE of the sample without rear TCO. This is most likely due to two reasons.

First, the rear ITO acts as a back reflector [104]. Without it the parasitic absorption in the silver electrode will strongly increase which will reduce the light absorption in the c-Si bulk. Second, direct contact between the emitter and the metal can result in large contact resistance because of Fermi level pinning [78]. This hinders charge carrier extraction. Comparing the other samples, one can notice that the IWO samples have a lower EQE except for the wavelength range between 550 and 800 nm. The exact reason for this is unclear since the opposite trend was expected.

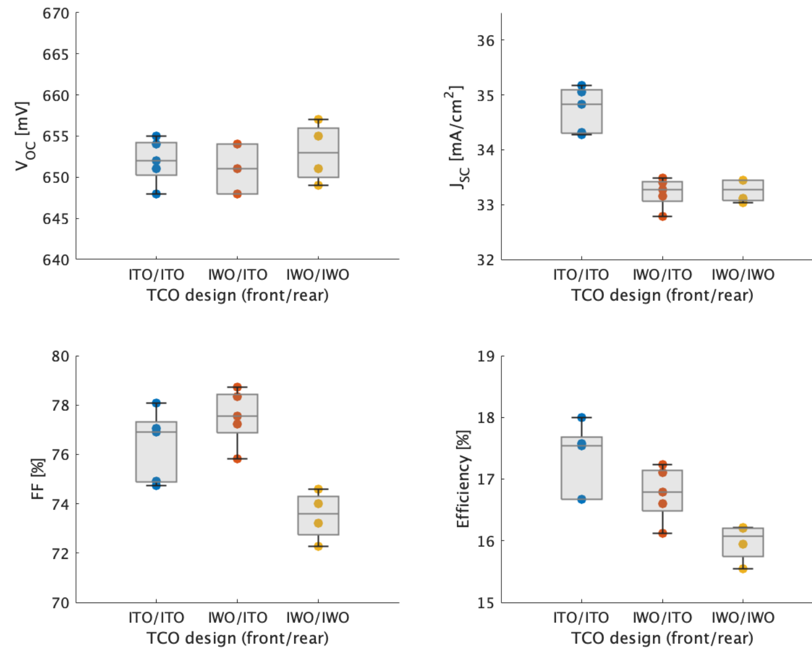


Figure 57: The V_{OC}, J_{SC}, fill factor and efficiency of solar cells with different TCO designs as measured with a J-V setup. The samples have TCO at the front and rear (ITO/ITO), IWO at the front and ITO at the rear (IWO/ITO), IWO at the front at rear (IWO/IWO) and no ITO at the rear. 5 samples of every design were fabricated and are depicted in the graph.

The final parameters of the devices are displayed in Figure 57. It should be noted that the sample without rear TCO was not functional and no J-V curve could be measured. This might be related to a high contact resistance. As already observed from the EQE curves the J_{SC} is lower for the IWO samples. The difference between the ITO/ITO sample and the samples with an IWO layer is quite high with more than 2 mA/cm^2. The J_{SC} from the EQE measurement for samples 1-3 is 35.43, 33.97 and 33.75 mA/cm^2, respectively. Furthermore, the sample with the IWO front side exhibits a lower V_{OC}. It is interesting to observe the different response of the V_{OC} to the post metallization annealing. After the screen printing process, the J-V curve of the solar cell is measured. This first measurement is shown in the Appendix in Figure 83. Subsequently, the post metallization annealing is applied where the solar cell is annealed at 250 °C for 5 min and then the J-V curve is measured again. The final performance of the samples after the post-metallization annealing is shown in Figure 57. It has been observed that the samples behave differently upon the post metallization annealing. The second sample shows no improvement in V_{OC} which is probably due to a saturation

in passivation after the TCO recovery annealing or related to the contact formation after the screen printing process [19]. The low fill factor of the third sample can not be explained as the cause is not clear. Possible reasons are a higher contact resistance at the the rear side and a lower carrier mobility which can be related to the processing conditions. Moreover, the J-V curves of the final solar cells and the device parameters are given in Appendix A.5 in Figure 84.

6.5 Optical simulations of the FBC solar cell

In this section, the optical simulation of the single-junction poly-SiO_x passivated c-Si solar cell is examined. GenPro4 is used to model the optical properties of the solar cell [23]. A description of the software can be found in Section 3.3. The absorptance vs. wavelength graph of the single-junction solar cell modelled with GenPro4 is presented in Figure 58. This structure is based on the standard single-junction FBC solar cell discussed in Chapter 5. It can be observed that the reflection losses and the parasitic absorption make up a significant amount. The reflection losses are especially pronounced around 400 nm. Furthermore, the reflection increases strongly from 600 to 1000 nm. Losses due to parasitic absorption can be observed in the ITO and the doped poly-SiO_x layers. The losses are particularly high in the n-doped poly-SiO_x contact at the front side. The reflection losses can be reduced by implementing an anti-reflection coating (ARC) at the front to improve the light in-coupling. Parasitic absorption can be decreased by reducing the thickness of the non-absorber layers. Those two approaches are investigated in more detail in this section.

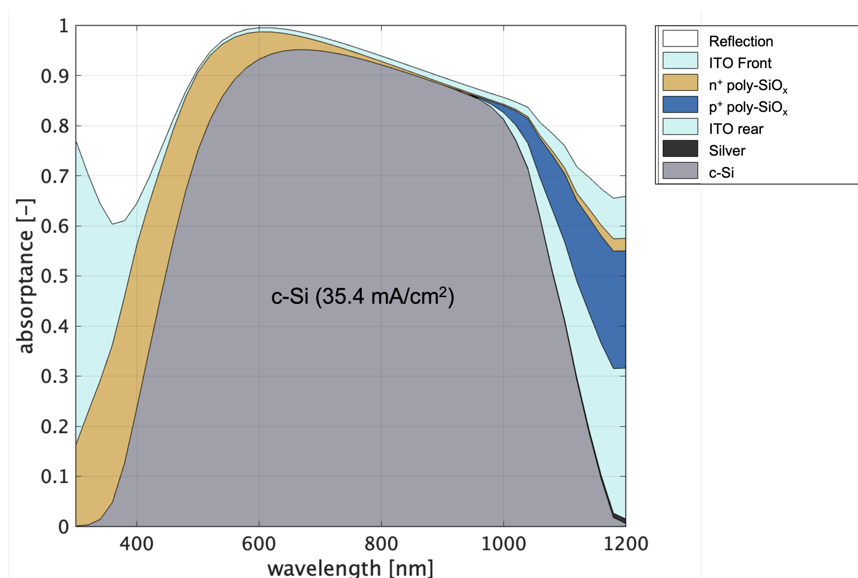


Figure 58: The optical simulation of the FBC single-junction solar cell structure as discussed in Chapter 5.

In Figure 59, the EQE curves of the simulation (dashed line), the FBC solar cell as discussed in Chapter 5 (solid blue line) and the improved FBC solar cell (solid orange line) with a different recovery annealing scheme as discussed in Section 6.1, are compared. The light absorption in the c-Si absorber material is slightly shifted to the the longer wavelength range in the simulation compared to the measured sample. This irregularity might result

from small errors during the EQE measurement, due to deviations from the expected ITO thickness of 75 nm or possibly by inaccuracies during the determination of the complex refractive index of the poly-SiO_x or the ITO which acts as the input data for the simulation. From Figure 59, it is clear that the first fabricated solar cell (solid blue line) exhibits a lower EQE than the simulated solar cell. This is most likely related to the relatively low passivation quality which facilitates recombination and hinders the efficient extraction of the charge carriers. By altering the recovery annealing scheme and enhancing the V_{OC}, the EQE of the solar cell, depicted as the solid orange line, also strongly increased between 500 and 1200 nm. A lower defect density, which possibly stems from the reduced diffusion of dopants, also reduces charge carrier recombination and enhances carrier extraction. Further studies of the solar cell regarding the TCO recovery annealing are needed to determine the exact reasons. Improvements might still be possible since the simulation shows that in the wavelength range of 600 - 1000 nm the theoretical limit is not reached yet.

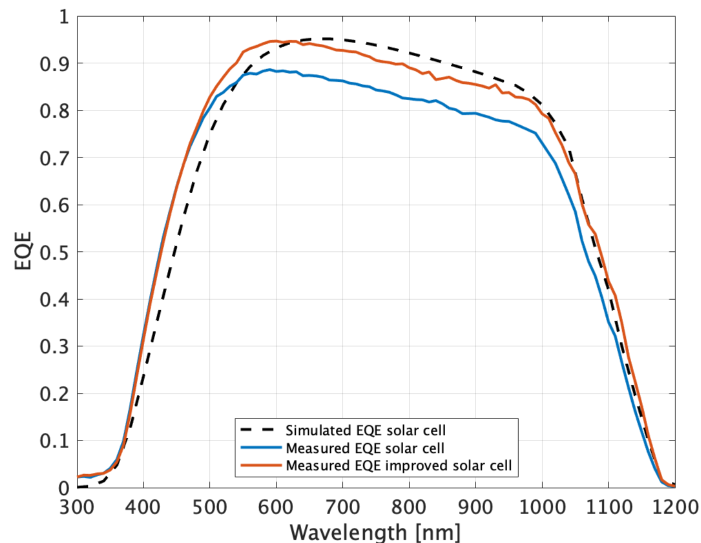


Figure 59: A comparison of the EQE curves of the simulation (dashed), the FBC single-junction solar cell as fabricated in Chapter 5 (solid blue line) and the FBC single-junction solar cell as fabricated in Section 6.1 with the improved TCO recovery annealing (solid orange line).

To further increase the J_{SC}, the following approaches could be chosen. The light incoupling can be enhanced by introducing refractive index grading and adding an ARC like MgF_2 [5]. An improvement of the absorption in the c-Si layer can be observed in Figure 60 by implementing a 60 nm MgF_2 layer as an ARC at the front side. The photocurrent density strongly increases in the mentioned wavelength range between 600 - 1000 nm. This improves the simulated photocurrent density to 38 mA/cm^2 while the reflection losses are reduced. A comparison of the photocurrent density, the reflection and parasitic absorption losses is shown in Figure 62.

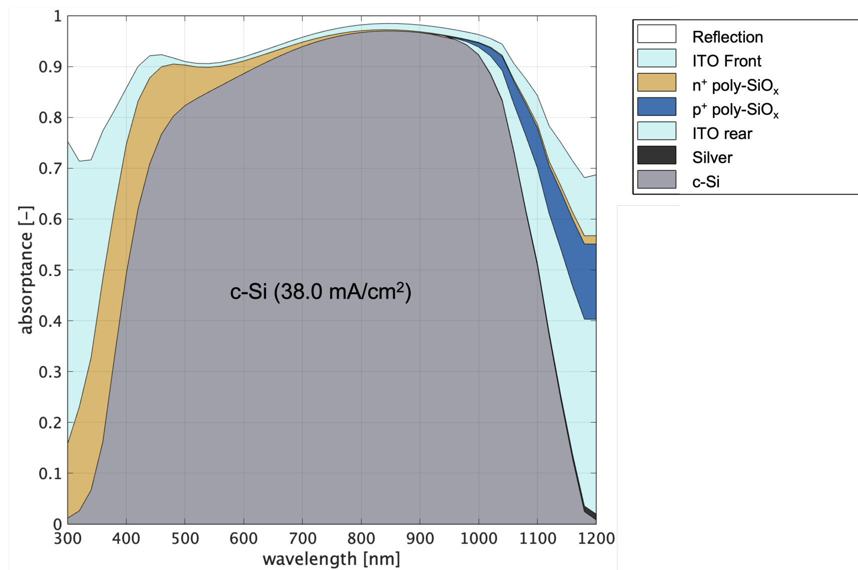


Figure 60: The optical simulation of the FBC single-junction solar cell structure as discussed in Chapter 5 with an additional 60 nm MgF_2 layer acting as an ARC.

Another option to improve the photocurrent density is the reduction of parasitic absorption losses in the non-absorber layers. Since the thickness of the ITO has been optically optimized to reduce reflection at the front surface and maximise back reflection at the poly-SiO_x/ITO interface at the rear, the doped poly-SiO_x contacts are investigated. In the standard structure in Figure 58 the poly-SiO_x emitters are each 30 nm thick and together absorb 3.7 mA/cm^2 as shown in Figure 62. By reducing the thickness to 15 nm the parasitic absorption can be reduced to 1.4 mA/cm^2 and the absorptance in the c-Si layer can be enhanced from 35.4 to 36.9 mA/cm^2. However, GenPro4 only considers the optical properties without taking the electrical characteristics and processing conditions into account. As discussed in Section 6.2, the thickness of the doped layer plays an important role for the electrical properties of the device in the reduction of sputtering damage and hence preventing a strong decrease in degradation.

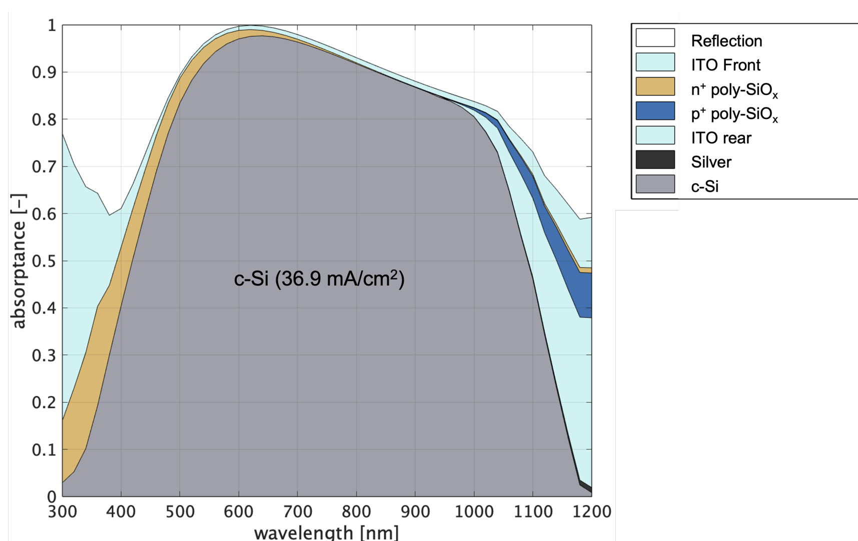


Figure 61: The optical simulation of the FBC single-junction solar cell structure as discussed in Chapter 5 with a reduction of the doped poly-SiO_x from 30 to 15 nm.

Therefore, the exact thickness of the poly-SiO_x and the processing conditions during the deposition have to be properly studied to achieve an optimal trade-off between optical and electrical properties. A detailed overview of the photocurrent density in the various layers for all three structures is given in Figure 62.

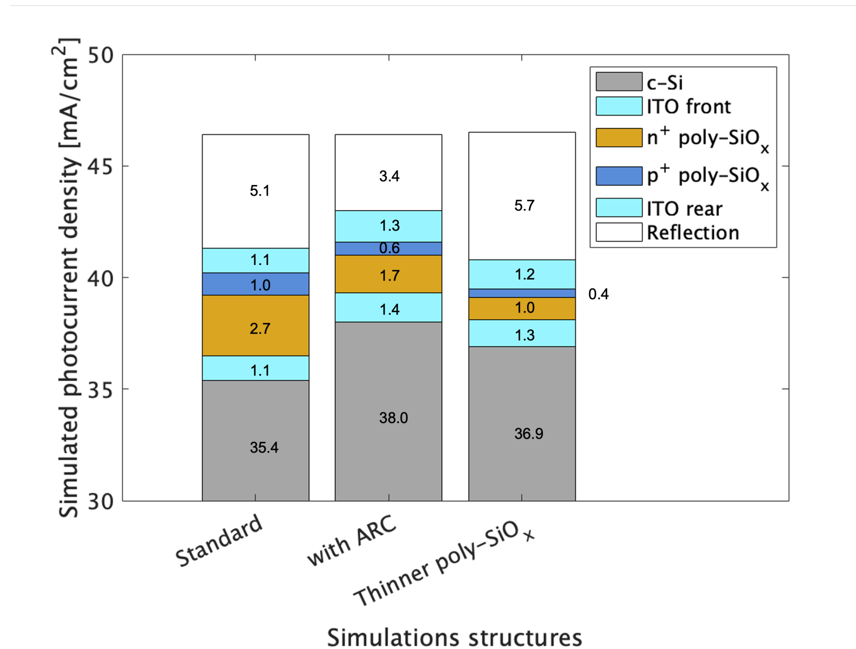


Figure 62: A comparison of the simulated photocurrent density in every layer. Three different structures are simulated. The solar cell as discussed in Chapter 5 is used as a reference (standard). The implementation of a MgF_2 layer as an ARC (with ARC) and the reduction of the emitter thickness (thinner poly-SiO_x) are compared to the standard structure.

6.6 Summary

The passivation recovery after the TCO recovery annealing was improved by lowering the thermal budget during the annealing process to 250 °C for 5 minutes. This might be related to lower dopant diffusion into the c-Si bulk which improves the field effect passivation and reduces the formation of boron-oxygen complexes which promotes recombination. By applying this annealing scheme the device performance was improved from 16.67 % to 18.76 %. By slightly increasing the thickness of the p-doped a-SiO_x layer, the sputtering damage was reduced. However, this goes along with an increased parasitic absorption in the emitter layer which results in a lower J_{SC}. Thus, the final parameters of the device do not improve but stay relatively constant. The introduction of an additional annealing step after the a-Si deposition has previously shown an increase in iV_{OC} which could not be reproduced during this work. The extra annealing step sometimes even seemed detrimental for the passivation quality of the samples. However, there are signs for an improvement in the J_{SC} which should be further investigated. The implementation of different TCO designs also did not lead to an improvement in the device performance. Omitting the deposition of the rear TCO resulted in a non-functional sample, possibly related to high recombination losses and high contact resistivity at the semiconductor/metal interface. The utilization of IWO instead of ITO was expected to increase the J_{SC} due to its improved transparency. However, a strong decrease

in J_{SC} was observed. The reasons for this are not completely clear. Lastly, optical simulation have been performed using GenPro4. It was found that there is still potential to improve the current density of the solar cell. Moreover, the reflection losses and parasitic absorption in the emitter layers are the main limitations of the device. Possible solutions are the implementation of an ARC coating and the thickness reduction of the doped poly-SiO_x layers although this will also have implications on the electrical properties of the solar cell.

7

Integration of the solar cell in a perovskite/c-Si tandem device

In this chapter the fabrication process of the crystalline silicon (c-Si) bottom cell with high temperature carrier selective passivating contacts is described in Section 7.1. After that, the structure and results of the tandem device are discussed in Section 7.2. The bottom cell used to fabricate the tandem cell does not include any improvements explored in Chapter 6 but is based on the FBC solar cell in Chapter 5.

7.1 Fabrication process of the c-Si bottom cell

The fabrication steps are depicted in Figure 63 and are similar to the process introduced in Chapter 5 for the single-junction solar cell except for a few changes. For the sake of completeness, the fabrication process is discussed again with the variations for the bottom cell pointed out in bold letters. Again, n-type float zone $< 100 >$ oriented silicon wafers with a diameter of 100 mm, a thickness of 280 µm (+/- 20 µm) and a resistivity of 1-5 Ω cm are utilised.

- To obtain single-side textured wafers, a 500 nm thick silicon nitride (SiN_x) layer is first deposited on one side to protect it against the texturing process. The wafers are then submerged into an aqueous Tetramethylammonium Hydroxide (TMAH) solution for 15 minutes at 85 °C. The solution consists of 4L of water, 1L of TMAH and 120ml of AlkaTex8. After the texturing step, the wafer is dipped into a solution of hydrofluoric acid (HF) and nitric acid (HNO_3) two minutes to smoothen the tips of the pyramids. Finally, the single-side textured wafers are dipped into BHF to remove the protective SiN_x layer.

- To prepare the wafers for the depositions, they undergo a standard cleaning procedure to remove organic and inorganic contaminations. First, the wafers are immersed into a 99% HNO_3 solution for 10 minutes and then rinsed with deionised (DI) water for 5 minutes. Subsequently, the wafers are immersed into a 69.5% HNO_3 solution for 10 minutes at 110 °C and again rinsed for 5 minutes with DI water. This is followed by a Marangoni drying to remove the native oxide layer.

- Next, the ultra-thin silicon oxide (SiO_x) tunneling layer is deposited via dry thermal oxidation. As discussed in the previous chapter, the processing conditions for the dry thermal oxidation are 675 °C for 3 minutes.

- To protect the ultra-thin SiO_x passivation layer, a 10 nm intrinsic amorphous silicon (a-Si) layer is deposited immediately afterwards in a LPCVD furnace with a silane flow rate of 45 sccm.

- Before the next step, the samples again undergo a Marangoni drying to remove the native oxide layer to obtain a good contact between the intrinsic a-Si and the doped amorphous silicon oxide (a-SiO_x) layers. A 20 nm n-doped a-SiO_x layer is then deposited on the polished side of while the 20 nm p-doped a-SiO_x layer is deposited on the textured side of the sample. The processing conditions are shown in Table 7.

Table 7: Final thickness and gas flow during the PECVD deposition of the doped a-SiO_x layers in sccm

Contact type	Thickness	SiH_4	CO_2	B_2H_6	PH_3	H_2
polished n-type	20 nm	4	6.4	-	4.8	35
textured p-type	20 nm	8	2	5	-	100

- Subsequently, the wafers are annealed at 900 °C for 15 minutes as discussed in Chapter 4 to crystallize the amorphous layers and activate the dopants for the diffusion from the doped to the intrinsic layer. From now on the passivation quality of the solar cell is determined using the Sinton WCT-120 photoconductance lifetime measurement setup after every processing step.

- To further improve the passivation quality of the sample a hydrogenation step is incorporated. This is done to passivate defects like dangling bonds at the interfaces. A 120 nm SiN_x layer is deposited via PECVD on both sides of the sample which is followed by forming gas annealing (FGA) for 30 min at 400 °C. During the annealing step the silicon nitride layer acts as a hydrogen source and the hydrogen diffuses into the previously deposited layers. After the hydrogenation, the SiN_x layer is etched away by a HF/BHF dip.

- Next, the transparent conductive oxide (TCO) is deposited via RF-Magnetron sputtering. **A 30 nm and 150 nm thick layer is deposited on the front and rear side, respectively. The 30 nm indium tin oxide (ITO) at the front acts as a tunnel recombination junction. No mask is used compared to the single-junction solar cell but a full-area deposition is utilized.**

- To recover the passivation degradation due to the ITO, deposition an annealing step at 400 °C in a hydrogen environment for 1 hour is incorporated. This was already discussed in more detail in Section 6.1. The improved annealing scheme at 250 °C was not yet incorporated during the fabrication of this tandem device.

- **The silver (Ag) metal contacts are applied via full-area thermal evaporation at the rear. No metal contacts are applied at the front side.**

- **Finally, the wafers are diced into 2.5 x 2.5 cm^2 pieces and shipped to TU Eindhoven in a nitrogen filled bag for the integration with the perovskite solar cell**.

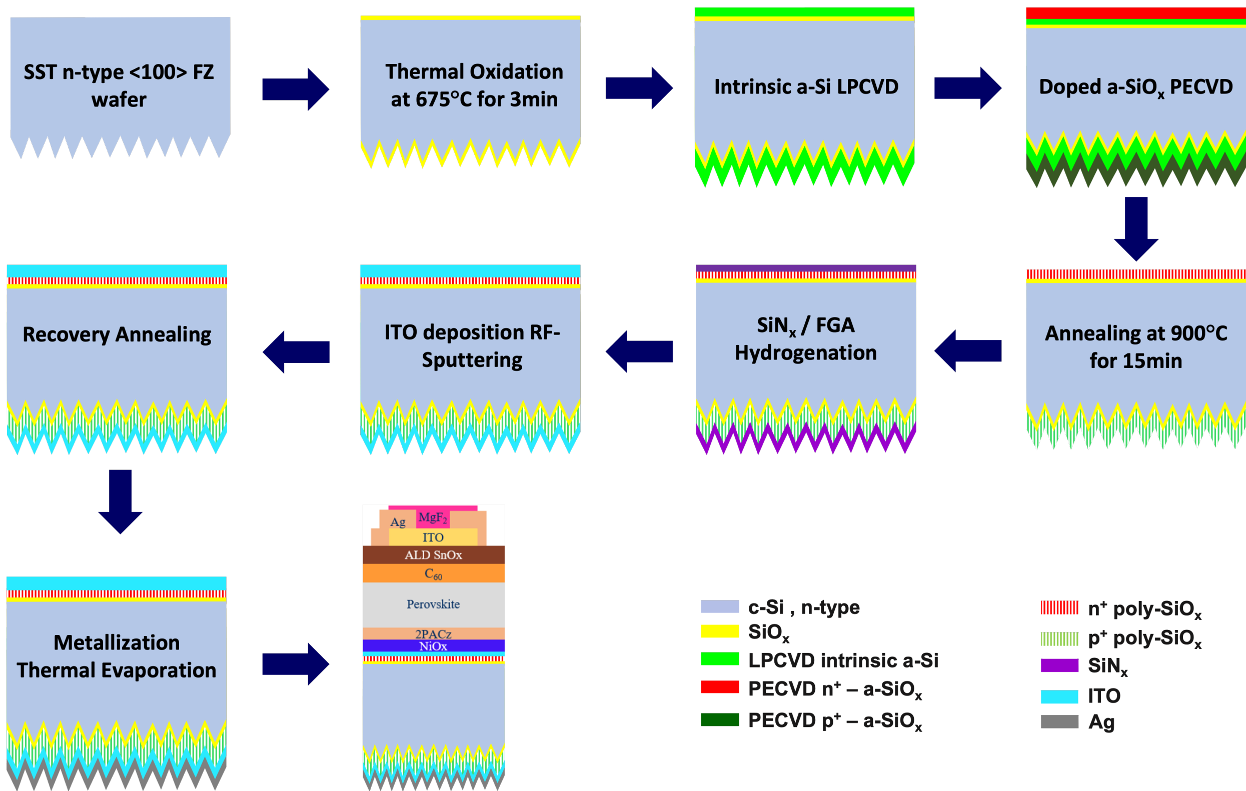
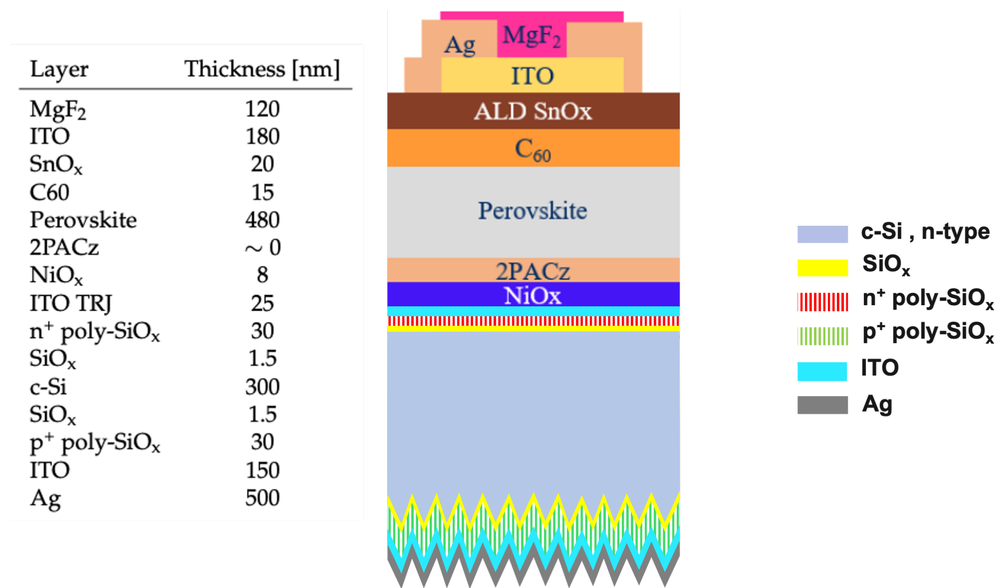


Figure 63: Fabrication process of a poly-SiO_x bottom cell solar cell and the final integration with the perovskite device.

7.2 Results

The final structure of the monolithic perovskite/c-Si tandem device with poly-SiO_x contacts is presented in Figure 64. The top cell is directly processed onto the c-Si bottom cell in an inverted p-i-n architecture which simplifies the fabrication and reduces the costs. However, the deposition of a conformal perovskite layer is difficult on textured surfaces. Hence, the bottom cell needs to have a flat front surface. This increases reflection losses and thus decreases the current density in the bottom cell. As already mentioned, the layers of the top cell are deposited directly onto the ITO tunnel recombination junction. Together, the NiO_x and the 2PACz layers form the hole transport layer (HTL). The main function of the NiO_x layer is to improve the adsorption of the organic 2PACz layer. This results in more compact binding and less defects and pinholes compared to a direct deposition of 2PACz onto ITO [149]. The NiO_x layer is about 7 nm thick while the 2PACz layer is a monolayer. Next, the perovskite is deposited with a thickness of about 480 nm which is chosen due to previous experience with perovskite/SHJ 2T tandem solar cells to achieve optimal current matching between the top and the bottom cell. The ALD SnO_x and C_{60} layer compose the electron transport layer (ETL). The C_{60} layer is about 15 nm thick. The purpose of the SnO_x (20 nm) is to act as a buffer layer and protect the C_{60} from potential sputtering damage during the

ITO deposition [150]. The front side consists of silver electrodes and an anti-reflection coating (ARC) which combines a layer of MgF_2 (120 nm) and ITO (180 nm). The ARC ensures optimal light in-coupling.



Layer	Thickness [nm]
MgF_2	120
ITO	180
SnO_x	20
C60	15
Perovskite	480
2PACz	~ 0
NiO_x	8
ITO TRJ	25
n^+ poly-SiO_x	30
SiO_x	1.5
c-Si	300
SiO_x	1.5
p^+ poly-SiO_x	30
ITO	150
Ag	500

Figure 64: Final structure and layer thickness of the perovskite/c-Si monolithic tandem device with poly-SiO_x high temperature carrier selective passivating contacts.

The J-V curve of the monolithic perovskite/c-Si tandem device with poly-SiO_x is presented in Figure 65. A final device efficiency of 23.1 % is achieved with a V_{OC} of 1.76 V, a J_{SC} of 17.81 mA/cm^2 and a fill factor of 74.0 %. As shown in Table 8, the current density between the top and bottom cell is not matched and the perovskite subcell strongly limits the performance. By adjusting the absorption in the two subcells, the J_{SC} can be enhanced. However, even though this will likely increase overall device performance, matching the current density can negatively influence the fill factor. It has been shown that the fill factor exhibits lower values when the mismatch is approximately zero. [49, 151, 152, 153, 154, 155]. The aim is to validate the experimental data using GenPro4 and then use the software to match the current density between the top and the bottom cell of the solar cell. This simulation can then be used to optimize the fabrication of the next tandem device. The simulation of the 2T tandem solar cell is discussed below.

Table 8: Comparison of the measured and simulated current density in the top and bottom cell of the tandem device. The current density of the modified simulation refers to the altered structure given in Table 9. The simulated EQE of this structure is displayed in Figure 67

	Current density [mA/cm^2]		
	Experiment	Simulation	Modified Simulation
Perovskite	17.8	19.7	17.9
c-Si	19.2	17.3	19.0

The EQE of the 2T tandem solar cell is given in Figure 66. The solid lines are the experimental data while the dashed lines represent the simulated solar cell in GenPro4. GenPro4

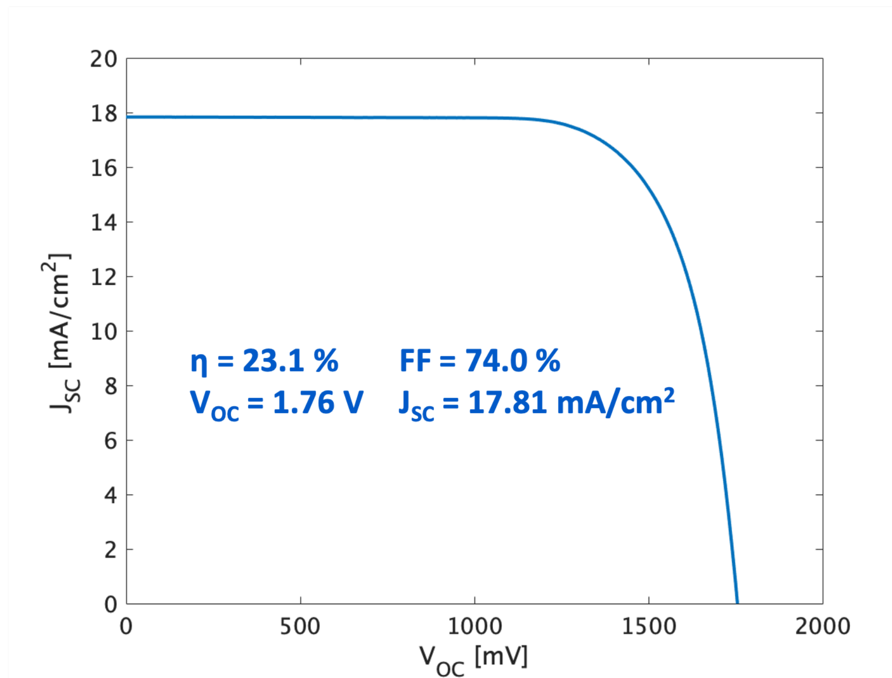


Figure 65: J-V curve of the monolithic perovskite/c-Si tandem device with the performance parameters.

is very convenient to current match tandem devices since the photocurrent density in every layer can easily be modelled. However, one can observe that the simulation does not properly match the experimental results. The simulation of the perovskite solar cell does not match the measured data between 500 and 800 nm and the c-Si solar cell simulation is inaccurate over almost the entire wavelength range. One reason could be errors in the complex refractive index of the perovskite top cell or the ARC which is used as an input for the simulation.

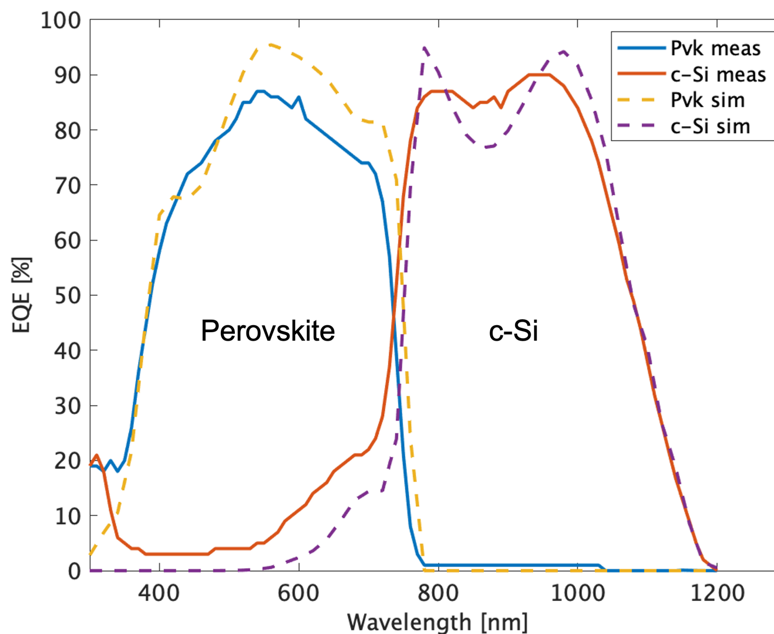


Figure 66: Measured and simulated EQE curves of the perovskite/c-Si 2T tandem solar cell with a poly-SiO_x bottom cell.

Other possible reasons could be problems with the EQE measurement or the perovskite

absorber layer thickness. Measuring the EQE of both subcells of a monolithic tandem device is not trivial [156]. The subcell under investigation has to be current limiting during the measurement to produce a valid result. This can be done by bias illumination, i.e to measure the top cell one can illuminate the device with 800 nm light which will bias the bottom cell but the wide band gap cell is insensitive to. Furthermore, a forward bias voltage often has to be applied to correct for the effect of the reverse voltage of the optically biased subcell which is not under investigation [156]. It is obvious that the EQE measurement in Figure 66 is flawed since the c-Si bottom cell exhibits an EQE of 20% at a wavelength of 300 nm which is not realistic because the perovskite layer will absorb all non-reflected light in this range. Hence, a measurement error might be the main problem which makes it difficult to validate the experimental data in GenPro4 and hinders further investigations.

However, it was attempted to match the measured EQE curve with GenPro4. To match the measured and simulated EQE curves, the simulation structure has to be drastically changed as shown in Table 9. The thickness of the ARC coatings has to be altered and the perovskite thickness strongly reduced to achieve current densities in each subcell that are similar to the measurement. The current density of each subcell is given in Table 8. One can see that the simulation with a modified thickness approximately matches the experimental data even in the wavelength range between 500 - 800 nm. However, this simulation is not realistic since the perovskite layer thickness is still about 480 nm and not 340 nm as assumed in the model. Moreover, the simulation still shows inaccuracies especially for the c-Si solar cell below 700 nm. Since the measurement of the EQE can not be fully trusted it is difficult to validate the curves using optical simulations.

Table 9: A comparison of the experimental layer structure and the modified structure used to simulate the tandem device as shown in Figure 67

Layer	Thickness [nm]	Modified Thickness [nm]
MgF_2	120	150
ITO	180	130
SnO_x	20	20
C_{60}	15	15
Perovskite	480	340
2PACz	0	0
NiO_x	8	8
ITO TRJ	25	20
n+ poly-SiO_x	30	30
SiO_x	1.5	1.5
c-Si	300	300
SiO_x	1.5	1.5
p+ poly-SiO_x	30	30
ITO	150	150
Ag	500	500

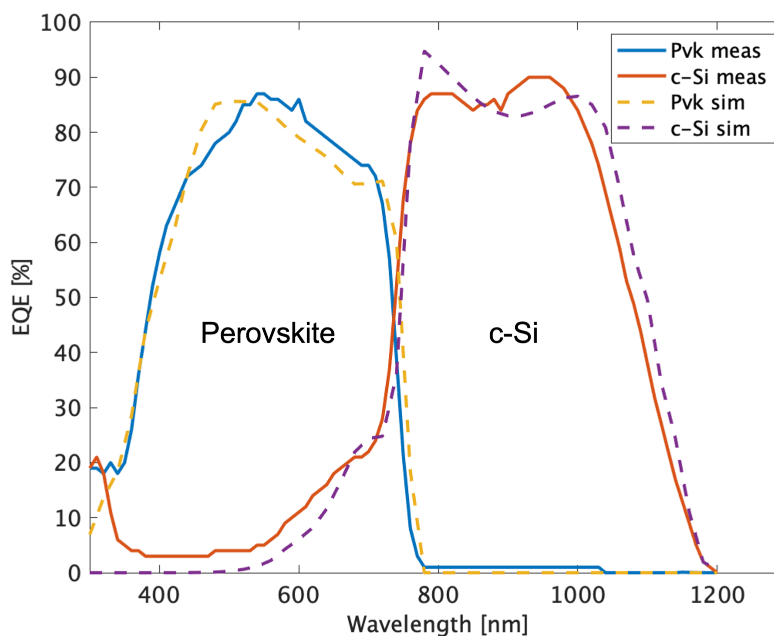


Figure 67: A comparison of the measured EQE and the simulated EQE of the perovskite/c-Si 2T tandem solar cell with a poly-SiO_x bottom cell with the modified thickness as shown in Table 9.

7.3 Summary

A poly-SiO_x c-Si solar cell was fabricated and integrated into a monolithic perovskite/c-Si tandem device in cooperation with TU Eindhoven. A final solar cell efficiency of 23.1 % was achieved with a fill factor of 74.0 %, a V_{OC} of 1.76 V and a J_{SC} of 17.81 mA/cm^2. The solar cell was limited by the current density in the perovskite top cell. The c-Si bottom cell exhibited a current density of 19.2 mA/cm^2. It is attempted to current match the top and the bottom cell by simulating the structure of the tandem device in GenPro4. However, it was not possible to validate the simulation. Possible reasons for this problem are the inaccuracy of the refractive index data of the perovskite top cell which is used as an input parameter for the simulation, measurement errors during the EQE measurement or problems with the perovskite layer thickness during the deposition process. Current matching could only be achieved by strongly altering the layer thickness in the simulation which does not represent the expected solar cell structure.

8

Conclusion

In this master thesis the fabrication of a c-Si solar cell with high temperature CSPC based on poly-SiO_x for integration into a multijunction device was investigated. The research objectives were the passivation optimisation of the doped poly-SiO_x contacts and subsequently the fabrication of a n-type front polished/p-type rear textured single-junction solar cell. Finally, the main objective was the fabrication of a perovskite/c-Si 2T tandem device based on poly-SiO_x passivating contacts. In this chapter the most important learnings and results regarding those objectives will be reported and discussed.

8.1 Passivation optimisation of the poly-SiO_x contacts

The SiO_x passivating layer and the high temperature annealing process are crucial steps to achieve a high V_{OC} and an excellent efficiency in CSPC solar cells. Thus, the process conditions during those important steps were optimized to ensure excellent surface passivation. It was found that a dry thermal oxidation at 675 °C for 3 minutes results in an optimal SiO_x passivating layer for polished n-type and textured p-type surfaces. Furthermore, an optimal thermal budget for the high temperature annealing process has to be determined to achieve crystallisation of the amorphous layers and the desired dopant diffusion. It was found that the optimal annealing conditions for a polished n-type lifetime sample are 900 °C and 15 minutes. After the crystallisation it resulted in an iV_{OC} of 727 mV. The optimal annealing conditions of textured p-type symmetric samples were determined to be 850 °C and 45 minutes. This resulted in a maximal iV_{OC} of 643 mV. However, one can notice that different optimised processing conditions for the high temperature annealing step are found regarding the n-type and p-type lifetime sample. Since the difference in iV_{OC} between the 850 °C and 900 °C annealing conditions for the textured p-type symmetric sample is relatively small with 640 and 643 mV, it was decided to move forward with the an annealing budget of 900 °C and 15 minutes for the fabrication of a solar cell with polished n-type and textured p-type contacts. After hydrogenation, the polished n-type lifetime samples exhibits an iV_{OC} of 745 mV and a minority carrier lifetime of more than 10 ms at a minority carrier density of 10^{15} per cm^3. The textured p-type symmetric sample exhibits a final iV_{OC} of 670 mV and a minority charge carrier lifetime of about 1.1 ms at 10^{15} per cm^3 after hydrogenation.

8.2 Fabrication of a single-junction poly-SiO_x solar cell

A single-junction solar cell with a polished n-type front and a textured p-type rear architecture was fabricated based on high temperature poly-SiO_x contacts. A maximum efficiency of 16.67 % with an V_{OC} of 649 mV, a J_{SC} of 34.28 mA/cm^2 and a fill factor of 74.93 % was obtained. The limiting factor to achieve a better device performance seems to be the textured p-type contact. From the lifetime measurements after every processing step, it was observed that the TCO recovery annealing at 400 °C for 60 min after the ITO deposition did not restore the passivation as expected. The iV_{OC} only recovered around 5-8 mV which corresponds to about 20-30 % and the annealing process even proved detrimental for the minority charge carrier lifetime. The reason for this is believed to be the diffusion of dopant into the c-Si bulk during the TCO recovery annealing which lowers the field effect passivation and promotes Auger recombination and the formation of oxygen-boron complexes.

Hence, a series of experiments with reduced annealing temperatures was undertaken to investigate the influence of the thermal budget on the passivation quality. It was found that annealing at 250 °C for 5 min drastically improved the iV_{OC} recovery and about 95% of the sputtering damage in terms of iV_{OC} could be recovered. By implementing the improved annealing scheme into the single-junction solar cell fabrication process, the final device performance was increased to 18.76 % with improvements in V_{OC}, J_{SC} and fill factor of 15 mV, 1.53 mA/cm^2 and 3.97 %, respectively. The increase in V_{OC} can be attributed to the reduced defect density which strongly influences the recombination losses and also increases the fill factor. This will also enhance the carrier extraction and thus, the J_{SC}. Moreover, from reflection measurements it can be observed that the reflection losses are also reduced with the new annealing scheme. This is also a reason for the enhancement in J_{SC}.

More experiments were performed to potentially improve the performance of the single-junction solar cell. The variation of the p+ a-SiO_x thickness showed that the layer thickness plays a significant role in the induced sputtering damage after the TCO deposition. Increasing the thickness leads to a decrease in sputtering damage but also leads to higher parasitic absorption. Hence, the positive and negative effects balance out when analyzing the overall device performance. The previously beneficial two-step annealing scheme with an additional annealing step after the amorphous silicon (a-Si) deposition also did not show any improvements regarding the solar cell efficiency. Furthermore, different TCO architectures were tested. An improvement of J_{SC} was expected when applying IWO instead of ITO. However, the J_{SC} did not improve but even decreased. The reason is not completely clear; problems with the processing conditions or the influence of the new TCO recovery annealing could be the responsible. Omitting the rear TCO to reduce the sputtering damage induced by the ITO deposition resulted in a non-functional device, which might be related to a high contact resistivity at the semiconductor/metal interface. Lastly, optical simulations were performed to investigate the optical performance of the solar cell. It is shown that the absorptance in the optical simulation is higher than the measured EQE in the fabricated poly-SiO_x solar cells. Hence, the carrier extraction can still be improved. Further

improvements of the photocurrent density are possible by reducing the reflection losses and parasitic absorption in the emitter layers which are the limiting factors. The reflection losses could be reduced by implementing a MgF_2 layer to increase light in-coupling. To reduce parasitic absorption, the thickness of the doped poly-SiO_x layers has to be decreased which has to be carefully engineered with respect to the deposition process to not deteriorate the electrical properties of the device.

8.3 Fabrication of a perovskite/c-Si tandem solar cell with high temperature carrier selective passivating contacts

Lastly, a c-Si solar cell with poly-SiO_x contacts was integrated into a monolithic perovskite/c-Si tandem device. The fabrication process of the c-Si bottom cell which was integrated into the tandem device only differs in a few aspects from the single-junction solar cell like the ITO layer thickness at the front side and the metallization method. The perovskite top cell utilizes C_{60} as an ETL, 2PACz as an HTL and an ARC made from ITO and MgF_2. This structure resulted in a tandem efficiency of 23.1 % with an V_{OC} of 1.76 V, a J_{SC} of 17.81 mA/cm^2 and a fill factor of 74.0 %. It is important to mention that the integrated c-Si bottom cell does not include any of the improvements discussed in Chapter 6 like the improved TCO recovery annealing conditions. The overall efficiency was limited by an unmatched current density in the top and bottom cell. The perovskite solar cell was current limiting with a J_{SC} of 17.8 mA/cm^2 while the c-Si bottom cell exhibits a current density of 19.2 mA/cm^2. Current matching was investigated using the optical simulation software GenPro4. However, it was not successful since the experimental EQE data from the tandem device could not be validated. This might stem from an EQE measurement error, inaccurate data of the complex refractive index or a different thickness than expected of the perovskite layer.

9

Recommendations for further research

In this last chapter, recommendations are given based on the results and the experience obtained during the project. Since this thesis investigated a completely novel tandem structure with poly-SiO_x passivating contacts, a device efficiency of 23.1 % is very promising and tempts further investigation. Regarding the passivation quality of the solar cell, the textured p-type contact seems to be the limiting factor. Hence, the main focus should be to either improve the passivation properties of the textured p-type contact or intrinsically alter the structure or composition of the device.

First, the different options which could potentially help to characterize and improve the textured p-type poly-SiO_x contact are inspected. A more detailed study of the ultra-thin SiO_x passivating layer would enhance the understanding of the current transport and defect formation at the interface. Currently, the exact thickness of the layer after the dry thermal oxidation can not be determined. Spectroscopic ellipsometry can be used, but depending on the exact model, the measured thickness varies between 1 to 2.5 nm. Therefore, the layer thickness should be accurately determined to create a model specifically for this process. Measuring the thickness could potentially be done by determining the step size after a HF etching step with atomic force microscopy (AFM) or methods like X-ray photoelectron spectroscopy (XPS) [157, 158]. XPS can also be used to determine the composition of the SiO_x. The different silicon oxidation states give indications about the density and the thermal stability of the film which is important for the subsequent processing steps. Furthermore, capacitance-voltage measurements could be used to determine the interface defect density which is an important parameter for the recombination properties of the device.

To further optimize the p-doped emitter layer, secondary-ion mass spectroscopy (SIMS) measurements can be performed to get a better understanding of the dopant diffusion and interface accumulation of the various elements. A focus could be put on the two-step annealing scheme. This approach has exhibited an increase in passivation of 20 mV after the high temperature annealing step in the past during other projects at the PVMD group but could not be reproduced. Hence, additional experiments like the characterisation of the crystal structure using Raman spectroscopy before and after the extra annealing step and contact resistivity measurements could shed light on the process. Moreover, the influence of the additional annealing step after the high temperature annealing can be analyzed by contact resistivity and SIMS measurements to see if the altered processing scheme changes the dopant diffusion.

Also, more studies about the influence of the TCO deposition and the subsequent re-

covery annealing on the doped poly-SiO_x contact layers should be done to enhance the knowledge of the process. It would be especially interesting to investigate the dopant diffusion, formation of defect phases and change of the contact resistivity during the recovery annealing since strong variation in passivation quality depending on the exact processing conditions were observed during this project. Furthermore, the influence of the atmosphere during the annealing process and the introduction of a thin buffer layer before the TCO sputtering can be examined.

Another important step during the fabrication of the solar cell is the hydrogenation process after the high temperature annealing. This step includes the deposition of an hydrogenated silicon nitride layer which acts as a hydrogen source and has to be etched again after the process. This etching process is relatively volatile and introduces uncertainty into the fabrication process since it depends on the exact mixing ratio of the chemicals and the subjective optical assessment of the etching progress by the researcher. The progress of the etching is especially hard to determine for flat interfaces. Hence, other options like a hydrogen plasma could be evaluated to stabilise the fabrication process and make it more reproducible.

Moreover, the optimal conditions for the contact formation after the metallization process have to be studied. In the past the contact formation was done at at 170 °C for 30 minutes. However, it was found that higher annealing temperatures between 250-350 °C for 5-15 minutes can further improve the properties of the solar cells.

However, a more efficient solution would be to circumvent the use of the textured p-doped poly-SiO_x contact. By altering the polarity of the tandem device, a polished p-type front/textured n-type rear architecture can be adopted. Since the stability and passivation quality of textured n-doped poly-SiO_x has been shown to be significantly better than that of its p-doped counterpart the open-circuit voltage of the bottom cell could be substantially increased. This might be a very efficient solution to further increase the performance of a monolithic perovskite/poly-SiO_x tandem device. If the polarity can not be changed due to boundary conditions during the perovskite processing, other options can be investigated. One could be the adoption of gallium as a dopant instead of boron. It has been shown that the use of gallium instead of boron in poly-Si passivating contacts can achieve similar iV_{OC} values even though simultaneously an increase in contact resistivity was observed [159]. Gallium is becoming increasingly important and and might replace boron as the main dopant for p-type semiconductors in the future due to the light-induced degradation (LID) observed in boron-doped materials [160]. In this work it is speculated that the main problem of the textured p-doped poly-SiO_x stems from the diffusion of boron into the c-Si bulk and the interaction of boron and oxygen which leads to the formation of boron-oxygen defects during the various annealing steps. This has already been observed in mono- and polycrystalline silicon and is possibly one of the reasons for LID [117]. Hence, it is believed that the high amount of oxygen in the poly-SiO_x layer intensifies the formation of those defects. This could potentially be prevented by the selection of gallium as a p-type dopant.

References

[1] H. Ritchie and M. Roser, “CO_2 and greenhouse gas emissions,” *Our World in Data*, 2020. https://ourworldindata.org/co2-and-other-greenhouse-gas-emissions.

[2] C. Kost, S. Shammugan, V. Fluri, D. Peper, A. Davoodi Memar, and T. Schlegl, “Levelized cost of electricity renewable energy technologies,” tech. rep., Frauenhofer Institute for Solar Energy Systems (ISE), Freiburg, Deutschland, 2021.

[3] V. Badilita, “Study of vertical coupled-cavity laser structures,” *PhD Dissertation, EPFL*, 2004.

[4] R. Limpens, “Spectroscopical investigations of the space-separated quantum cutting mechanism,” *Master Thesis, University of Amsterdam*, 2015.

[5] A. H. Smets, K. Jäger, O. Isabella, R. A. Swaaij, and M. Zeman, *Solar Energy: The physics and engineering of photovoltaic conversion, technologies and systems*. UIT Cambridge, 2015.

[6] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, H. Uzu, *et al.*, “Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%,” *Nature energy*, vol. 2, no. 5, pp. 1–8, 2017.

[7] L. Tous, “Nickel/copper plated contacts as an alternative to silver screen printing for the front side metallization of industrial high efficiency silicon solar cells,” *PhD Dissertation, KU Leuven*, 2014.

[8] L. Mazzarella, “Nanocrystalline silicon and silicon oxide contact layers for silicon heterojunction solar cells,” *PhD Dissertation, TU Berlin*, 2017.

[9] Y. Ko, H. Park, C. Lee, Y. Kang, and Y. Jun, “Recent progress in interconnection layer for hybrid photovoltaic tandems,” *Advanced Materials*, vol. 32, no. 51, p. 2002196, 2020.

[10] B. Bilal and H. Najeeb-ud Din, “Fundamentals of and recent advances in carrier selective passivating contacts for silicon solar cells,” *Journal of Electronic Materials*, pp. 1–12, 2021.

[11] C. Henderson, “Infotracks,” *Semitracks monthyl newsletter*, vol. 64, 2014.

[12] N. C. Mandal, S. Biswas, S. Acharya, T. Panda, S. Sadhukhan, J. R. Sharma, A. Nandi, S. Bose, A. Kole, G. Das, *et al.*, “Study of the properties of SiO_x layers prepared by different techniques for rear side passivation in TOPCon solar cells,” *Materials Science in Semiconductor Processing*, vol. 119, p. 105163, 2020.

[13] A. K. Senapati and M. B. Singh, "High efficiency multi-junction solar cell design," *International Journal of Engineering and Applied Sciences*, vol. 2, no. 4, p. 257958.

[14] Z. Zhang, Z. Li, L. Meng, S.-Y. Lien, and P. Gao, "Perovskite-based tandem solar cells: get the most out of the sun," *Advanced Functional Materials*, vol. 30, no. 38, p. 2001904, 2020.

[15] M. De Bastiani, A. S. Subbiah, E. Aydin, F. H. Isikgor, T. G. Allen, and S. De Wolf, "Recombination junctions for efficient monolithic perovskite-based tandem solar cells: physical principles, properties, processing and prospects," *Materials Horizons*, vol. 7, no. 11, pp. 2791–2809, 2020.

[16] S. Kazmi, B. Rangarajan, T. Aarnink, C. Salm, and J. Schmitz, "Low stressed in-situ boron doped poly-SiGe layers for high-Q resonators," in *2010 STW. ICT Conference on Research in Information and Communication Technology*, pp. 109–113, STW, 2010.

[17] J. Melskens, "Optimisation of a protocrystalline hydrogenated amorphous silicon top solar cell for highest stabilised efficiency," *Master Thesis, TU Delft*, 2007.

[18] D. Muller, "Introduction to vacuum coating by sputter technology," *vacuumscience-world.com*, 2021. (https://www.vacuumscienceworld.com/blog/vacuum-coating-sputter-technology [7.4.2022]).

[19] J. Schube, *Metallization of silicon solar cells with passivating contacts*. PhD thesis, Universität Freiburg, 2020.

[20] K. Bothe, "Oxygen-related trapping and recombination centres in boron-doped crystalline silicon," *PhD Dissertation, University of Hannover*, 2006.

[21] A. Rosenberg, D. Hu, H. Chouaib, Z. Tan, and N. Malkova, "Tracking the defects and the band gap of ultra-thin HfO_2 using a multi-oscillator cody lorentz model," vol. 10585, Proc. SPIE, 2018.

[22] Perkin Elmer Inc., "Applications and use of integrating spheres with the La 650 and 850 UV/Vis and Lambda 950 UV/Vis/NIR spectrophotometers," 2004.

[23] R. Santbergen, T. Meguro, T. Suezaki, G. Koizumi, K. Yamamoto, and M. Zeman, "GenPro4 optical model for solar cell simulation and its application to multijunction solar cells," *IEEE journal of photovoltaics*, vol. 7, no. 3, pp. 919–926, 2017.

[24] R. An, M. Ji, and S. Zhang, "Global warming and obesity: a systematic review," *Obesity Reviews*, vol. 19, no. 2, pp. 150–163, 2018.

[25] M. L. Grieneisen and M. Zhang, "The current status of climate change research," *Nature Climate Change*, vol. 1, no. 2, pp. 72–73, 2011.

[26] J. R. Fleming, *Historical perspectives on climate change*. Oxford University Press, 2005.

[27] V. H. Dale, "The relationship between land-use change and climate change," *Ecological applications*, vol. 7, no. 3, pp. 753–769, 1997.

[28] O. G. Sorokhtin, L. F. Khilyuk, and G. Chilingarian, *Global warming and global cooling: Evolution of climate on earth*. Elsevier, 2007.

[29] S. Fawzy, A. I. Osman, J. Doran, and D. W. Rooney, "Strategies for mitigation of climate change: a review," *Environmental Chemistry Letters*, pp. 1–26, 2020.

[30] S. Kumar, S. Himanshu, and K. Gupta, "Effect of global warming on mankind," *Int Res J Environ Sci*, vol. 1, no. 4, pp. 56–9, 2012.

[31] D. Wallace-Wells, *The uninhabitable earth: Life after warming*. Tim Duggan Books, 2020.

[32] Climeworks, "Orca, direct air capture and storage." `https://climeworks.com/orca`, 2021. [Accessed on 23/09/2021].

[33] bp, "Statistical review of world energy 2021." `https://www.bp.com/en/global/corporate/energy-economics/statistical-review-of-world-energy.html`, 2021. [Accessed on 23/09/2021].

[34] D. Feldman, V. Ramasamy, R. Fu, A. Ramdas, J. Desai, and R. Margolis, "US solar photovoltaic system and energy storage cost benchmark: Q1 2020," tech. rep., National Renewable Energy Lab.(NREL), Golden, CO (United States), 2021.

[35] D. M. Powell, M. T. Winkler, H. Choi, C. B. Simmons, D. B. Needleman, and T. Buonassisi, "Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs," *Energy & Environmental Science*, vol. 5, no. 3, pp. 5874–5883, 2012.

[36] A. C. Goodrich, D. M. Powell, T. L. James, M. Woodhouse, and T. Buonassisi, "Assessing the drivers of regional trends in solar photovoltaic manufacturing," *Energy & Environmental Science*, vol. 6, no. 10, pp. 2811–2821, 2013.

[37] M. Victoria, N. Haegel, I. M. Peters, R. Sinton, A. Jäger-Waldau, C. del Cañizo, C. Breyer, M. Stocks, A. Blakers, I. Kaizuka, *et al.*, "Solar photovoltaics is ready to power a sustainable future," *Joule*, 2021.

[38] M. A. Green, E. D. Dunlop, J. Hohl-Ebinger, M. Yoshita, N. Kopidakis, and X. Hao, "Solar cell efficiency tables (version 58)," *Progress in Photovoltaics: Research and Applications*, vol. 29, no. 7, pp. 657–667, 2021.

[39] A. Richter, M. Hermle, and S. W. Glunz, "Reassessment of the limiting efficiency for crystalline silicon solar cells," *IEEE journal of photovoltaics*, vol. 3, no. 4, pp. 1184–1191, 2013.

[40] N. Cherradi, "Solar PV technolgies, what's next?." `https://www.f10.org/pdf/Solar-PV-technologies-whats-next-Nabih-Cherradi.pdf`, 2019. [Accessed on 27/09/2021].

[41] J. Melskens, B. W. van de Loo, B. Macco, L. E. Black, S. Smit, and W. Kessels, "Passivating contacts for crystalline silicon solar cells: From concepts and materials to prospects," *IEEE Journal of Photovoltaics*, vol. 8, no. 2, pp. 373–388, 2018.

[42] P. Tockhorn, J. Sutter, A. Cruz, P. Wagner, K. Jäger, D. Yoo, F. Lang, M. Grischek, B. Li, A. Al-Ashouri, *et al.*, "Nano-optical designs enhance monolithic perovskite/silicon tandem solar cells toward 29.8% efficiency," 2022.

[43] E. Köhnen, P. Wagner, F. Lang, A. Cruz, B. Li, M. Roß, M. Jošt, A. B. Morales-Vilches, M. Topič, M. Stolterfoht, *et al.*, "27.9% efficient monolithic perovskite/silicon tandem solar cells on industry compatible bottom cells," *Solar RRL*, p. 2100244, 2021.

[44] A. Al-Ashouri, E. Köhnen, B. Li, A. Magomedov, H. Hempel, P. Caprioglio, J. A. Márquez, A. B. M. Vilches, E. Kasparavicius, J. A. Smith, *et al.*, "Monolithic perovskite/silicon tandem solar cell with $> 29\%$ efficiency by enhanced hole extraction," *Science*, vol. 370, no. 6522, pp. 1300–1309, 2020.

[45] P. S. Schulze, A. J. Bett, M. Bivour, P. Caprioglio, F. M. Gerspacher, Ö. Ş. Kabaklı, A. Richter, M. Stolterfoht, Q. Zhang, D. Neher, *et al.*, "25.1% high-efficiency monolithic perovskite silicon tandem solar cell with a high bandgap perovskite absorber," *Solar RRL*, vol. 4, no. 7, p. 2000152, 2020.

[46] B. Chen, J. Y. Zhengshan, S. Manzoor, S. Wang, W. Weigand, Z. Yu, G. Yang, Z. Ni, X. Dai, Z. C. Holman, *et al.*, "Blade-coated perovskites on textured silicon for 26%-efficient monolithic perovskite/silicon tandem solar cells," *Joule*, vol. 4, no. 4, pp. 850–864, 2020.

[47] J. Zheng, H. Mehrvarz, C. Liao, J. Bing, X. Cui, Y. Li, V. R. Gonçales, C. F. J. Lau, D. S. Lee, Y. Li, *et al.*, "Large-area 23%-efficient monolithic perovskite/homojunction-silicon tandem solar cell with enhanced UV stability using down-shifting material," *ACS Energy Letters*, vol. 4, no. 11, pp. 2623–2631, 2019.

[48] A. J. Bett, P. S. Schulze, K. M. Winkler, Ö. S. Kabakli, I. Ketterer, L. E. Mundt, S. K. Reichmuth, G. Siefer, L. Cojocaru, L. Tutsch, *et al.*, "Two-terminal perovskite silicon tandem solar cells with a high-bandgap perovskite absorber enabling voltages over 1.8 V," *Progress in Photovoltaics: Research and Applications*, vol. 28, no. 2, pp. 99–110, 2020.

[49] E. Köhnen, M. Jošt, A. B. Morales-Vilches, P. Tockhorn, A. Al-Ashouri, B. Macco, L. Kegelmann, L. Korte, B. Rech, R. Schlatmann, *et al.*, "Highly efficient monolithic perovskite silicon tandem solar cells: analyzing the influence of current mismatch on device performance," *Sustainable Energy & Fuels*, vol. 3, no. 8, pp. 1995–2005, 2019.

[50] G. Nogay, F. Sahli, J. Werner, R. Monnard, M. Boccard, M. Despeisse, F. Haug, Q. Jeangros, A. Ingenito, and C. Ballif, "25.1%-efficient monolithic perovskite/silicon tandem solar cell based on a p-type monocrystalline textured silicon wafer and high-temperature passivating contacts," *ACS Energy Letters*, vol. 4, no. 4, pp. 844–845, 2019.

[51] L. Mazzarella, Y.-H. Lin, S. Kirner, A. B. Morales-Vilches, L. Korte, S. Albrecht, E. Crossland, B. Stannowski, C. Case, H. J. Snaith, *et al.*, "Infrared light management using a nanocrystalline silicon oxide interlayer in monolithic perovskite/silicon heterojunction tandem solar cells with efficiency above 25%," *Advanced Energy Materials*, vol. 9, no. 14, p. 1803241, 2019.

[52] F. Hou, L. Yan, B. Shi, J. Chen, S. Zhu, Q. Ren, S. An, Z. Zhou, H. Ren, C. Wei, *et al.*, "Monolithic perovskite/silicon-heterojunction tandem solar cells with open-circuit voltage of over 1.8 V," *ACS Applied Energy Materials*, vol. 2, no. 1, pp. 243–249, 2019.

[53] M. A. Green, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, M. Yoshita, and A. W. Y. Ho-Baillie, "Solar cell efficiency tables (version 54)," *Progress in Photovoltaics: Research and Applications*, vol. 27, no. 7, pp. 565–575, 2019.

[54] H. Shen, S. T. Omelchenko, D. A. Jacobs, S. Yalamanchili, Y. Wan, D. Yan, P. Phang, T. Duong, Y. Wu, Y. Yin, *et al.*, "In-situ recombination junction between p-Si and TiO_2 enables high-efficiency monolithic perovskite/Si tandem cells," *Science advances*, vol. 4, no. 12, p. eaau9711, 2018.

[55] F. Hou, C. Han, O. Isabella, L. Yan, B. Shi, J. Chen, S. An, Z. Zhou, W. Huang, H. Ren, *et al.*, "Inverted pyramidally-textured PDMS antireflective foils for perovskite/silicon tandem solar cells with flat top cell," *Nano energy*, vol. 56, pp. 234–240, 2019.

[56] B. Chen, Z. Yu, K. Liu, X. Zheng, Y. Liu, J. Shi, D. Spronk, P. N. Rudd, Z. Holman, and J. Huang, "Grain engineering for perovskite/silicon monolithic tandem solar cells with efficiency of 25.4%," *Joule*, vol. 3, no. 1, pp. 177–190, 2019.

[57] M. Jošt, E. Köhnen, A. B. Morales-Vilches, B. Lipovšek, K. Jäger, B. Macco, A. Al-Ashouri, J. Krč, L. Korte, B. Rech, *et al.*, "Textured interfaces in monolithic perovskite/silicon tandem solar cells: advanced light management for improved efficiency and energy yield," *Energy & Environmental Science*, vol. 11, no. 12, pp. 3511–3523, 2018.

[58] J. Zheng, H. Mehrvarz, F.-J. Ma, C. F. J. Lau, M. A. Green, S. Huang, and A. W. Ho-Baillie, "21.8% efficient monolithic perovskite/homo-junction silicon tandem solar cell on 16 cm^2," *ACS Energy Letters*, vol. 3, no. 9, pp. 2299–2300, 2018.

[59] K. A. Bush, S. Manzoor, K. Frohna, Z. J. Yu, J. A. Raiford, A. F. Palmstrom, H.-P. Wang, R. Prasanna, S. F. Bent, Z. C. Holman, *et al.*, "Minimizing current and voltage losses to reach 25% efficient monolithic two-terminal perovskite–silicon tandem solar cells," *ACS Energy Letters*, vol. 3, no. 9, pp. 2173–2180, 2018.

[60] F. Sahli, J. Werner, B. A. Kamino, M. Bräuninger, R. Monnard, B. Paviet-Salomon, L. Barraud, L. Ding, J. J. D. Leon, D. Sacchetto, *et al.*, "Fully textured monolithic perovskite/silicon tandem solar cells with 25.2% power conversion efficiency," *Nature Materials*, vol. 17, no. 9, pp. 820–826, 2018.

[61] J. Zheng, C. F. J. Lau, H. Mehrvarz, F.-J. Ma, Y. Jiang, X. Deng, A. Soeriyadi, J. Kim, M. Zhang, L. Hu, *et al.*, "Large area efficient interface layer free monolithic perovskite/homo-junction-silicon tandem solar cell with over 20% efficiency," *Energy & Environmental Science*, vol. 11, no. 9, pp. 2432–2443, 2018.

[62] F. Sahli, B. A. Kamino, J. Werner, M. Bräuninger, B. Paviet-Salomon, L. Barraud, R. Monnard, J. P. Seif, A. Tomasi, Q. Jeangros, *et al.*, "Improved optics in monolithic perovskite/silicon tandem solar cells with a nanocrystalline silicon recombination junction," *Advanced Energy Materials*, vol. 8, no. 6, p. 1701609, 2018.

[63] Y. Wu, D. Yan, J. Peng, Y. Wan, S. P. Phang, H. Shen, N. Wu, C. Barugkin, X. Fu, S. Surve, *et al.*, "Monolithic perovskite/silicon-homojunction tandem solar cell with over 22% efficiency," *Energy & Environmental Science*, vol. 10, no. 11, pp. 2472–2479, 2017.

[64] K. A. Bush, A. F. Palmstrom, J. Y. Zhengshan, M. Boccard, R. Cheacharoen, J. P. Mailoa, D. P. McMeekin, R. L. Hoye, C. D. Bailie, T. Leijtens, *et al.*, "23.6%-efficient monolithic perovskite/silicon tandem solar cells with improved stability," *Nature Energy*, vol. 2, no. 4, pp. 1–7, 2017.

[65] J. Werner, A. Walter, E. Rucavado, S.-J. Moon, D. Sacchetto, M. Rienaecker, R. Peibst, R. Brendel, X. Niquille, S. De Wolf, *et al.*, "Zinc tin oxide as high-temperature stable recombination layer for mesoscopic perovskite/silicon monolithic tandem solar cells," *Applied Physics Letters*, vol. 109, no. 23, p. 233902, 2016.

[66] J. Werner, L. Barraud, A. Walter, M. Bräuninger, F. Sahli, D. Sacchetto, N. Tétreault, B. Paviet-Salomon, S.-J. Moon, C. Allebé, *et al.*, "Efficient near-infrared-transparent perovskite solar cells enabling direct comparison of 4-terminal and monolithic perovskite/silicon tandem cells," *ACS Energy Letters*, vol. 1, no. 2, pp. 474–480, 2016.

[67] J. Werner, C.-H. Weng, A. Walter, L. Fesquet, J. P. Seif, S. De Wolf, B. Niesen, and C. Ballif, "Efficient monolithic perovskite/silicon tandem solar cell with cell area > 1 cm^2," *The journal of physical chemistry letters*, vol. 7, no. 1, pp. 161–166, 2015.

[68] S. Albrecht, M. Saliba, J. P. C. Baena, F. Lang, L. Kegelmann, M. Mews, L. Steier, A. Abate, J. Rappich, L. Korte, *et al.*, "Monolithic perovskite/silicon-heterojunction tandem solar cells processed at low temperature," *Energy & Environmental Science*, vol. 9, no. 1, pp. 81–88, 2016.

[69] J. P. Mailoa, C. D. Bailie, E. C. Johlin, E. T. Hoke, A. J. Akey, W. H. Nguyen, M. D. McGehee, and T. Buonassisi, "A 2-terminal perovskite/silicon multijunction solar cell

enabled by a silicon tunnel junction," *Applied Physics Letters*, vol. 106, no. 12, p. 121105, 2015.

[70] P. Wuerfel, *Physics of Solar Cells*. Wiley-VCH, 2005.

[71] D. Neamen, *Semiconductor physics and devices*. McGraw-Hill Higher Education, 2012.

[72] H. Can, "High-mobility TCO-based contacting schemes for c-Si solar cells," *PhD Dissertation, TU Delft*, 2022.

[73] N. Balaji, S. Q. Hussain, C. Park, J. Raja, J. Yi, and R. Jeyakumar, "Surface passivation schemes for high-efficiency c-Si solar cells," *Transactions on Electrical and Electronic Materials*, vol. 16, no. 5, pp. 227–233, 2015.

[74] A. G. Aberle, "Surface passivation of crystalline silicon solar cells: a review," *Progress in Photovoltaics: Research and Applications*, vol. 8, no. 5, pp. 473–487, 2000.

[75] J. Schmidt, R. Peibst, and R. Brendel, "Surface passivation of crystalline silicon solar cells: Present and future," *Solar Energy Materials and Solar Cells*, vol. 187, pp. 39–54, 2018.

[76] S. W. Glunz, M. Bivour, C. Messmer, F. Feldmann, R. Müller, C. Reichel, A. Richter, F. Schindler, J. Benick, and M. Hermle, "Passivating and carrier-selective contacts-basic requirements and implementation," in *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)*, pp. 2064–2069, IEEE, 2017.

[77] F. Feldmann, M. Bivour, C. Reichel, H. Steinkemper, M. Hermle, and S. W. Glunz, "Tunnel oxide passivated contacts as an alternative to partial rear contacts," *Solar Energy Materials and Solar Cells*, vol. 131, pp. 46–50, 2014.

[78] T. G. Allen, J. Bullock, X. Yang, A. Javey, and S. De Wolf, "Passivating contacts for crystalline silicon solar cells," *Nature Energy*, vol. 4, no. 11, pp. 914–928, 2019.

[79] A. Cuevas, "The recombination parameter J_0," *Energy Procedia*, vol. 55, pp. 53–62, 2014.

[80] V. A. Dao, S. Kim, Y. Lee, S. Kim, J. Park, S. Ahn, and J. Yi, "High-efficiency heterojunction with intrinsic thin-layer solar cells: a review," *Current photovoltaic research*, vol. 1, no. 2, pp. 73–81, 2013.

[81] B. Bilal and H. Najeeb-ud Din, "Towards low cost, industrially compatible silicon heterojunction solar cells using hybrid carrier selective passivating contacts," *Optical Materials*, vol. 124, p. 111957, 2022.

[82] A. Čampa, F. Smole, N. Folchert, T. Wietler, B. Min, R. Brendel, and M. Topič, "Detailed analysis and understanding of the transport mechanism of poly-Si based carrier selective junctions," *IEEE Journal of Photovoltaics*, vol. 9, no. 6, pp. 1575–1582, 2019.

[83] R. Peibst, U. Römer, Y. Larionova, M. Rienäcker, A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, *et al.*, "Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?," *Solar energy materials and solar cells*, vol. 158, pp. 60–67, 2016.

[84] M. Köhler, M. Pomaska, F. Lentz, F. Finger, U. Rau, and K. Ding, "Wet-chemical preparation of silicon tunnel oxides for transparent passivated contacts in crystalline silicon solar cells," *ACS applied materials & interfaces*, vol. 10, no. 17, pp. 14259–14263, 2018.

[85] L. Lu, Y. Zeng, M. Liao, J. Zheng, Y. Lin, M. Feng, Y. Zhi, H. He, W. Ding, C. Shou, *et al.*, "Dopant diffusion through ultra-thin AlO_x and AlO_x/SiO_x tunnel layer in TOPCon structure and its impact on the passivation quality on c-Si solar cells," *Solar Energy Materials and Solar Cells*, vol. 223, p. 110970, 2021.

[86] F. Feldmann, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics," *Solar energy materials and solar cells*, vol. 120, pp. 270–274, 2014.

[87] Z. Zhang, Y. Zeng, C.-S. Jiang, Y. Huang, M. Liao, H. Tong, M. Al-Jassim, P. Gao, C. Shou, X. Zhou, *et al.*, "Carrier transport through the ultrathin silicon-oxide layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells," *Solar Energy Materials and Solar Cells*, vol. 187, pp. 113–122, 2018.

[88] S. P. Padi, M. Q. Khokhar, S. Chowdhury, E.-C. Cho, and J. Yi, "Nanoscale SiO_x tunnel oxide deposition techniques and their influence on cell parameters of TOPCon solar cells," *Transactions on Electrical and Electronic Materials*, vol. 22, no. 5, pp. 557–566, 2021.

[89] B. E. Deal and A. Grove, "General relationship for the thermal oxidation of silicon," *Journal of applied physics*, vol. 36, no. 12, pp. 3770–3778, 1965.

[90] T. Hattori, "Chemical structures of the SiO_2/Si interface," *Critical Reviews in Solid State and Material Sciences*, vol. 20, no. 4, pp. 339–382, 1995.

[91] H. Z. Massoud, J. D. Plummer, and E. A. Irene, "Thermal oxidation of silicon in dry oxygen growth-rate enhancement in the thin regime: I. experimental results," *Journal of the electrochemical society*, vol. 132, no. 11, p. 2685, 1985.

[92] H. Z. Massoud, J. D. Plummer, and E. A. Irene, "Thermal oxidation of silicon in dry oxygen: Growth-rate enhancement in the thin regime: II. physical mechanisms," *Journal of The Electrochemical Society*, vol. 132, no. 11, p. 2693, 1985.

[93] C. K. Fink, K. Nakamura, S. Ichimura, and S. J. Jenkins, "Silicon oxidation by ozone," *Journal of Physics: Condensed Matter*, vol. 21, no. 18, p. 183001, 2009.

[94] T. Nishiguchi, S. Saitoh, N. Kameda, Y. Morikawa, M. Kekura, H. Nonaka, and S. Ichimura, "Rapid oxidation of silicon using UV-light irradiation in low-pressure, highly concentrated ozone gas below 300 °C," *Japanese journal of applied physics*, vol. 46, no. 5R, p. 2835, 2007.

[95] H. Angermann, K. Wolke, C. Gottschalk, A. Moldovan, M. Roczen, J. Fittkau, M. Zimmer, and J. Rentsch, "Electronic interface properties of silicon substrates after ozone based wet-chemical oxidation studied by SPV measurements," *Applied surface science*, vol. 258, no. 21, pp. 8387–8396, 2012.

[96] A. Moldovan, F. Feldmann, K. Kaufmann, S. Richter, M. Werner, C. Hagendorf, M. Zimmer, J. Rentsch, and M. Hermle, "Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO_2 layers grown by photo-oxidation or wet-chemical oxidation in ozonized water," in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, pp. 1–6, IEEE, 2015.

[97] L. Martinu and D. Poitras, "Plasma deposition of optical films and coatings: A review," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 18, no. 6, pp. 2619–2645, 2000.

[98] B. Kafle, B. S. Goraya, S. Mack, F. Feldmann, S. Nold, and J. Rentsch, "TOPCon - technology options for cost efficient industrial manufacturing," *Solar Energy Materials and Solar Cells*, vol. 227, p. 111100, 2021.

[99] S. Reiter, N. Koper, R. Reineke-Koch, Y. Larionova, M. Turcu, J. Krügener, D. Tetzlaff, T. Wietler, U. Höhne, J.-D. Kähler, *et al.*, "Parasitic absorption in polycrystalline Si-layers for carrier-selective front junctions," *Energy Procedia*, vol. 92, pp. 199–204, 2016.

[100] S. C. Baker-Finch, K. R. McIntosh, D. Yan, K. C. Fong, and T. C. Kho, "Near-infrared free carrier absorption in heavily doped silicon," *Journal of Applied Physics*, vol. 116, no. 6, p. 063106, 2014.

[101] F. Feldmann, C. Reichel, R. Müller, and M. Hermle, "The application of poly-Si/SiO_x contacts as passivated top/rear contacts in Si solar cells," *Solar Energy Materials and Solar Cells*, vol. 159, pp. 265–271, 2017.

[102] G. Yang, P. Guo, P. Procel, A. Weeber, O. Isabella, and M. Zeman, "Poly-crystalline silicon-oxide films as carrier-selective passivating contacts for c-Si solar cells," *Applied Physics Letters*, vol. 112, no. 19, p. 193904, 2018.

[103] R. Santbergen, G. Yang, P. Procel, G. Limodio, A. Weeber, O. Isabella, and M. Zeman, "Optical analysis of poly-Si and poly-SiO_x carrier-selective passivating contacts for c-Si solar cells," in *Optical Nanostructures and Advanced Materials for Photovoltaics*, pp. PW3A–5, Optical Society of America, 2017.

[104] Z. C. Holman, M. Filipič, A. Descoeudres, S. De Wolf, F. Smole, M. Topič, and C. Ballif, "Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells," *Journal of Applied Physics*, vol. 113, no. 1, p. 013107, 2013.

[105] K. Chopra, S. Major, and D. Pandya, "Transparent conductors—a status review," *Thin solid films*, vol. 102, no. 1, pp. 1–46, 1983.

[106] H. Park, Y.-J. Lee, J. Park, Y. Kim, J. Yi, Y. Lee, S. Kim, C.-K. Park, and K.-J. Lim, "Front and back TCO research review of a-Si/c-Si heterojunction with intrinsic thin layer (HIT) solar cell," *Transactions on Electrical and Electronic Materials*, vol. 19, no. 3, pp. 165–172, 2018.

[107] R. T. Tung, "Chemical bonding and Fermi level pinning at metal-semiconductor interfaces," *Physical review letters*, vol. 84, no. 26, p. 6078, 2000.

[108] R. T. Tung, "The physics and chemistry of the Schottky barrier height," *Applied Physics Reviews*, vol. 1, no. 1, p. 011304, 2014.

[109] J. Werner, B. Niesen, and C. Ballif, "Perovskite/silicon tandem solar cells: Marriage of convenience or true love story?–an overview," *Advanced Materials Interfaces*, vol. 5, no. 1, p. 1700731, 2018.

[110] L. Yan, C. Han, B. Shi, Y. Zhao, and X. Zhang, "A review on the crystalline silicon bottom cell for monolithic perovskite/silicon tandem solar cells," *Materials Today Nano*, vol. 7, p. 100045, 2019.

[111] E. L. Warren, W. E. McMahon, M. Rienacker, K. T. VanSant, R. C. Whitehead, R. Peibst, and A. C. Tamboli, "A taxonomy for three-terminal tandem solar cells," *ACS Energy Letters*, vol. 5, no. 4, pp. 1233–1242, 2020.

[112] T. de Vrijer, D. van Nijen, H. Parasramka, P. A. P. Moya, Y. Zhao, O. Isabella, and A. H. Smets, "The fundamental operation mechanisms of nc-SiO_x:H based tunnel recombination junctions revealed," *Solar Energy Materials and Solar Cells*, vol. 236, p. 111501, 2022.

[113] Z. C. Holman, A. Descoeudres, L. Barraud, F. Z. Fernandez, J. P. Seif, S. De Wolf, and C. Ballif, "Current losses at the front of silicon heterojunction solar cells," *IEEE Journal of Photovoltaics*, vol. 2, no. 1, pp. 7–15, 2012.

[114] D. Grant, K. Catchpole, K. Weber, and T. White, "Design guidelines for perovskite/silicon 2-terminal tandem solar cells: an optical study," *Optics express*, vol. 24, no. 22, pp. A1454–A1470, 2016.

[115] L. Mazzarella, A. B. Morales-Vilches, L. Korte, R. Schlatmann, and B. Stannowski, "Versatility of nanocrystalline silicon films: From thin-film to perovskite/c-Si tandem solar cell applications," *Coatings*, vol. 10, no. 8, p. 759, 2020.

[116] A. Tomasi, B. Paviet-Salomon, Q. Jeangros, J. Haschke, G. Christmann, L. Barraud, A. Descoeudres, J. P. Seif, S. Nicolay, M. Despeisse, *et al.*, "Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth," *Nature Energy*, vol. 2, no. 5, pp. 1–8, 2017.

[117] K. Bothe, R. Sinton, and J. Schmidt, "Fundamental boron-oxygen related carrier lifetime limit in mono-and multicrystalline silicon," *Progress in photovoltaics: Research and Applications*, vol. 13, no. 4, pp. 287–296, 2005.

[118] J. Cotter, J. Guo, P. Cousins, M. Abbott, F. Chen, and K. Fisher, "p-type versus n-type silicon wafers: prospects for high-efficiency commercial silicon solar cells," *IEEE Transactions on Electron Devices*, vol. 53, no. 8, pp. 1893–1901, 2006.

[119] D. Iencinella, E. Centurioni, R. Rizzoli, and F. Zignani, "An optimized texturing process for silicon solar cell substrates using TMAH," *Solar energy materials and solar cells*, vol. 87, no. 1-4, pp. 725–732, 2005.

[120] H. Ge, "Development of high efficiency SHJ/poly-Si passivating contact hybrid solar cells," *Master Thesis, TU Delft*, 2017.

[121] M. G. Kang, S. Tark, J. C. Lee, C.-S. Son, and D. Kim, "Changes in efficiency of a solar cell according to various surface-etching shapes of silicon substrate," *Journal of Crystal Growth*, vol. 326, no. 1, pp. 14–18, 2011.

[122] S. Choi, O. Kwon, K. H. Min, M. S. Jeong, K. T. Jeong, M. G. Kang, S. Park, K. K. Hong, H.-e. Song, and K.-H. Kim, "Formation and suppression of hydrogen blisters in tunnelling oxide passivating contact for crystalline silicon solar cells," *Scientific Reports*, vol. 10, no. 1, pp. 1–14, 2020.

[123] Y. Hamedani, P. Macha, T. J. Bunning, R. R. Naik, and M. C. Vasudev, "Plasma-enhanced chemical vapor deposition: Where we are and the outlook for the future," *Chemical Vapor Deposition-Recent Advances and Applications in Optical, Solar Cells and Solid State Devices*, vol. 4, pp. 243–280, 2016.

[124] S. Choi, K. H. Min, M. S. Jeong, J. I. Lee, M. G. Kang, H.-E. Song, Y. Kang, H.-S. Lee, D. Kim, and K.-H. Kim, "Structural evolution of tunneling oxide passivating contact upon thermal annealing," *Scientific reports*, vol. 7, no. 1, pp. 1–11, 2017.

[125] B. J. Hallam, P. G. Hamer, A. M. Ciesla née Wenham, C. E. Chan, B. Vicari Stefani, and S. Wenham, "Development of advanced hydrogenation processes for silicon solar cells via an improved understanding of the behaviour of hydrogen in silicon," *Progress in Photovoltaics: Research and Applications*, vol. 28, no. 12, pp. 1217–1238, 2020.

[126] A. Cruz, E.-C. Wang, A. B. Morales-Vilches, D. Meza, S. Neubert, B. Szyszka, R. Schlatmann, and B. Stannowski, "Effect of front TCO on the performance of rear-junction

silicon heterojunction solar cells: Insights from simulations and experiments," *Solar Energy Materials and Solar Cells*, vol. 195, pp. 339–345, 2019.

[127] R. Street, D. Biegelsen, and J. Stuke, "Defects in bombarded amorphous silicon," *Philosophical Magazine B*, vol. 40, no. 6, pp. 451–464, 1979.

[128] B. Demaurex, S. De Wolf, A. Descoeudres, Z. Charles Holman, and C. Ballif, "Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering," *Applied Physics Letters*, vol. 101, no. 17, p. 171604, 2012.

[129] K. Tao, S. Jiang, R. Jia, Y. Zhou, P. Zhang, X. Dai, H. Sun, Z. Jin, and X. Liu, "The impact of indium tin oxide deposition and post annealing on the passivation property of TOPCon solar cells," *Solar Energy*, vol. 176, pp. 241–247, 2018.

[130] L. Tutsch, F. Feldmann, J. Polzin, C. Luderer, M. Bivour, A. Moldovan, J. Rentsch, and M. Hermle, "Implementing transparent conducting oxides by DC sputtering on ultrathin SiO_x/poly-Si passivating contacts," *Solar Energy Materials and Solar Cells*, vol. 200, p. 109960, 2019.

[131] W. Yoon, D. Scheiman, Y.-W. Ok, Z. Song, C. Chen, G. Jernigan, A. Rohatgi, Y. Yan, and P. Jenkins, "Sputtered indium tin oxide as a recombination layer formed on the tunnel oxide/poly-Si passivating contact enabling the potential of efficient monolithic perovskite/Si tandem solar cells," *Solar Energy Materials and Solar Cells*, vol. 210, p. 110482, 2020.

[132] J. Plawsky, A. Fedorov, S. Garimella, H. Ma, S. Maroo, L. Chen, and Y. Nam, "Nano- and microstructures for thin-film evaporation—a review," *Nanoscale and microscale thermophysical engineering*, vol. 18, no. 3, pp. 251–269, 2014.

[133] H. Nagel, C. Berge, and A. G. Aberle, "Generalized analysis of quasi-steady-state and quasi-transient measurements of carrier lifetimes in semiconductors," *Journal of Applied Physics*, vol. 86, no. 11, pp. 6218–6221, 1999.

[134] A. Cuevas and R. A. Sinton, "Prediction of the open-circuit voltage of solar cells from the steady-state photoconductance," *Progress in Photovoltaics: Research and Applications*, vol. 5, no. 2, pp. 79–90, 1997.

[135] H. Fujiwara and R. W. Collins, *Spectroscopic ellipsometry for photovoltaics*. Springer, 2018.

[136] R. A. Sinton, A. Cuevas, *et al.*, "A quasi-steady-state open-circuit voltage method for solar cell characterization," in *Proceedings of the 16th European photovoltaic solar energy conference*, vol. 1152, p. 4, 2000.

[137] R. A. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Applied Physics Letters*, vol. 69, no. 17, pp. 2510–2512, 1996.

[138] K. Jäger, M. Fischer, R. Van Swaaij, and M. Zeman, "A scattering model for nano-textured interfaces and its application in opto-electrical simulations of thin-film silicon solar cells," *Journal of Applied Physics*, vol. 111, no. 8, p. 083108, 2012.

[139] K. Jäger, "On the scalar scattering theory for thin-film solar cells," *PhD Dissertation, TU Delft*, 2012.

[140] A. Amarnath, "Fabrication of high efficiency poly-SiO_x passivated c-Si FBC solar cells," *Master Thesis, TU Delft*, 2021.

[141] P. Guo, "Development of in-situ doped poly-SiO_x passivating contacts for high-efficiency solar cells," *Master Thesis, TU Delft*, 2018.

[142] F. Feldmann, G. Nogay, J.-I. Polzin, B. Steinhauser, A. Richter, A. Fell, C. Schmiga, M. Hermle, and S. W. Glunz, "A study on the charge carrier transport of passivating contacts," *IEEE Journal of Photovoltaics*, vol. 8, no. 6, pp. 1503–1509, 2018.

[143] B. Han, H. Takamizawa, Y. Shimizu, K. Inoue, Y. Nagai, F. Yano, Y. Kunimune, M. Inoue, and A. Nishida, "Phosphorus and boron diffusion paths in polycrystalline silicon gate of a trench-type three-dimensional metal-oxide-semiconductor field effect transistor investigated by atom probe tomography," *Applied Physics Letters*, vol. 107, no. 2, p. 023506, 2015.

[144] A. Herguth and G. Hahn, "Kinetics of the boron-oxygen related defect in theory and experiment," *Journal of Applied Physics*, vol. 108, no. 11, p. 114509, 2010.

[145] J. Schube, L. Tutsch, T. Fellmeth, M. Bivour, F. Feldmann, T. Hatt, F. Maier, R. Keding, F. Clement, and S. W. Glunz, "Low-resistivity screen-printed contacts on indium tin oxide layers for silicon solar cells with passivating contacts," *IEEE Journal of Photovoltaics*, vol. 8, no. 5, pp. 1208–1214, 2018.

[146] D. Adachi, J. L. Hernández, and K. Yamamoto, "Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency," *Applied Physics Letters*, vol. 107, no. 23, p. 233506, 2015.

[147] S. Mirabella, D. De Salvador, E. Napolitani, E. Bruno, and F. Priolo, "Mechanisms of boron diffusion in silicon and germanium," *Journal of Applied Physics*, vol. 113, no. 3, p. 3, 2013.

[148] R. Street, C. Tsai, J. Kakalios, and W. Jackson, "Hydrogen diffusion in amorphous silicon," *Philosophical Magazine B*, vol. 56, no. 3, pp. 305–320, 1987.

[149] J. Sun, C. Shou, J. Sun, X. Wang, Z. Yang, Y. Chen, J. Wu, W. Yang, H. Long, Z. Ying, *et al.*, "NiO_x-seeded self-assembled monolayers as highly hole-selective passivating contacts for efficient inverted perovskite solar cells," *Solar RRL*, vol. 5, no. 11, p. 2100663, 2021.

[150] J. Wang, V. Zardetto, K. Datta, D. Zhang, M. M. Wienk, and R. A. Janssen, "16.8% monolithic all-perovskite triple-junction solar cells via a universal two-step solution process," *Nature communications*, vol. 11, no. 1, pp. 1–10, 2020.

[151] M. Boccard and C. Ballif, "Influence of the subcell properties on the fill factor of two-terminal perovskite–silicon tandem solar cells," *ACS Energy Letters*, vol. 5, no. 4, pp. 1077–1082, 2020.

[152] C. Ulbrich, C. Zahren, A. Gerber, B. Blank, T. Merdzhanova, A. Gordijn, and U. Rau, "Matching of silicon thin-film tandem solar cells for maximum power output," *International journal of photoenergy*, vol. 2013, 2013.

[153] M. Bonnet-Eymard, M. Boccard, G. Bugnon, F. Sculati-Meillaud, M. Despeisse, and C. Ballif, "Optimized short-circuit current mismatch in multi-junction solar cells," *Solar energy materials and solar cells*, vol. 117, pp. 120–125, 2013.

[154] W. McMahon, K. Emery, D. Friedman, L. Ottoson, M. Young, J. Ward, C. Kramer, A. Duda, and S. Kurtz, "Fill factor as a probe of current-matching for $GaInP_2$/GaAs tandem cells in a concentrator system during outdoor operation," *Progress in Photovoltaics: Research and Applications*, vol. 16, no. 3, pp. 213–224, 2008.

[155] M. Zeman, J. Willemen, L. Vosteen, G. Tao, and J. Metselaar, "Computer modelling of current matching in a-Si:H/a-Si:H tandem solar cells on textured TCO substrates," *Solar Energy Materials and Solar Cells*, vol. 46, no. 2, pp. 81–99, 1997.

[156] J. Gilot, M. M. Wienk, and R. A. Janssen, "Measuring the external quantum efficiency of two-terminal polymer tandem solar cells," *Advanced Functional Materials*, vol. 20, no. 22, pp. 3904–3911, 2010.

[157] C. J. Powell and A. Jablonski, "Measurement of silicon dioxide film thicknesses by X-ray photoelectron spectroscopy," in *AIP Conference Proceedings*, vol. 550, pp. 591–595, American Institute of Physics, 2001.

[158] J. Shallenberger, D. Cole, S. Novak, R. Moore, M. Edgell, S. Smith, C. Hitzman, J. Kirchhoff, E. Principe, S. Biswas, *et al.*, "Oxide thickness determination by XPS, AES, SIMS, RBS and TEM," in *1998 International Conference on Ion Implantation Technology. Proceedings (Cat. No. 98EX144)*, vol. 1, pp. 79–82, IEEE, 1998.

[159] T. N. Truong, T. T. Le, D. Yan, S. P. Phang, M. Tebyetekerwa, M. Young, M. Al-Jassim, A. Cuevas, D. Macdonald, J. Stuckelberger, *et al.*, "Investigation of gallium–boron spin-on codoping for poly-Si/SiO_x passivating contacts," *Solar RRL*, vol. 5, no. 12, p. 2100653, 2021.

[160] N. E. Grant, J. R. Scowcroft, A. I. Pointon, M. Al-Amin, P. P. Altermatt, and J. D. Murphy, "Lifetime instabilities in gallium doped monocrystalline PERC silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 206, p. 110299, 2020.

A

Appendix

A.1 Passivation quality of symmetric samples at different annealing conditions

In Figures 68 to 71, the iV_{OC} of the polished n-type and textured p-type symmetric samples annealed at 850 °C for 45 minutes and 950 °C for 15 minutes after hydrogenation are presented for all the different SiO_x layer processing conditions. It can be observed that both contacts display similar passivation properties at 850 °C 45 minutes for the 2 minute and 3 minute SiO_x sample compared to the 900 °C 15 minute annealing conditions which are presented in Section 4.4. This leads to the conclusion that for both annealing conditions a similar dopant diffusion behaviour takes place. However, as already observed in Section 4.2, the n-doped poly-Sio_x lifetime sample displays a greatly reduced iV_{OC} when annealed at 950 °C. This is most likely due to the higher dopant diffusion into the c-Si bulk at higher temperatures.

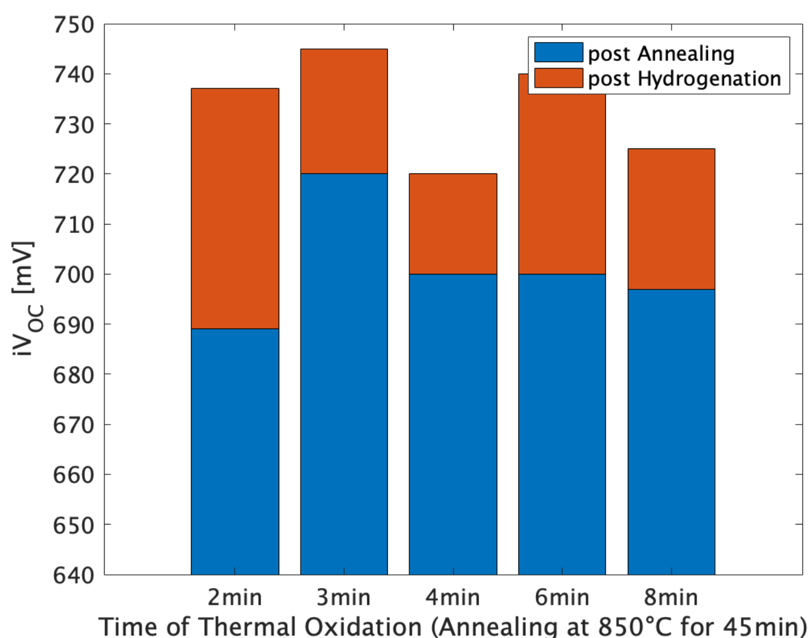


Figure 68: Comparison of the implied open-circuit voltage of polished n-type symmetric samples with different silicon oxide thickness after annealing at 850 °C (blue) and after hydrogenation (orange).

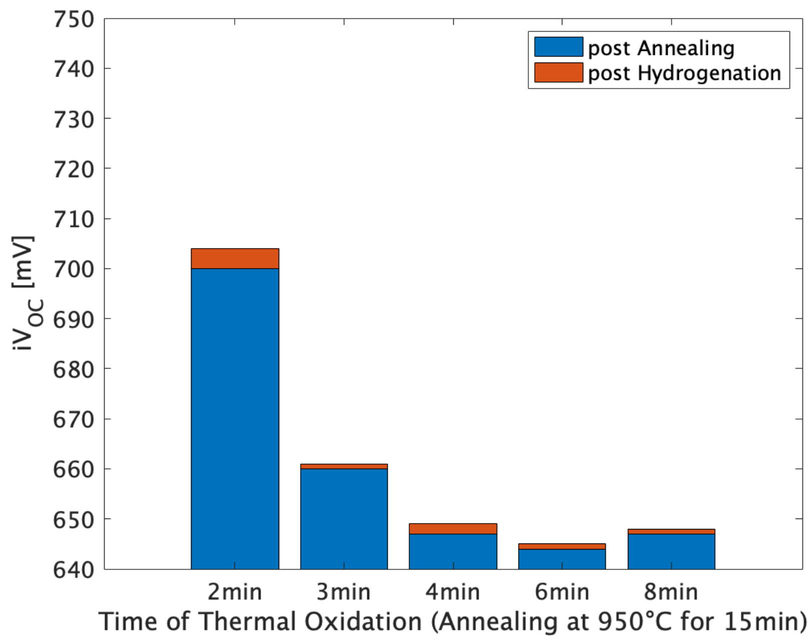


Figure 69: Comparison of the implied open-circuit voltage of polished n-type symmetric samples with different silicon oxide thickness after annealing at 950 °C (blue) and after hydrogenation (orange).

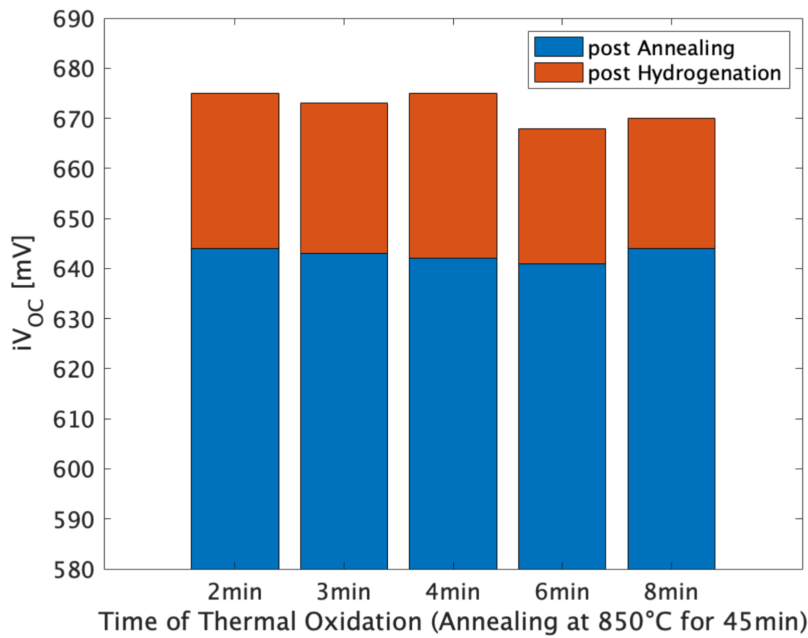


Figure 70: Comparison of the implied open-circuit voltage of textured p-type symmetric samples with different silicon oxide thickness after annealing at 850 °C (blue) and after hydrogenation (orange).

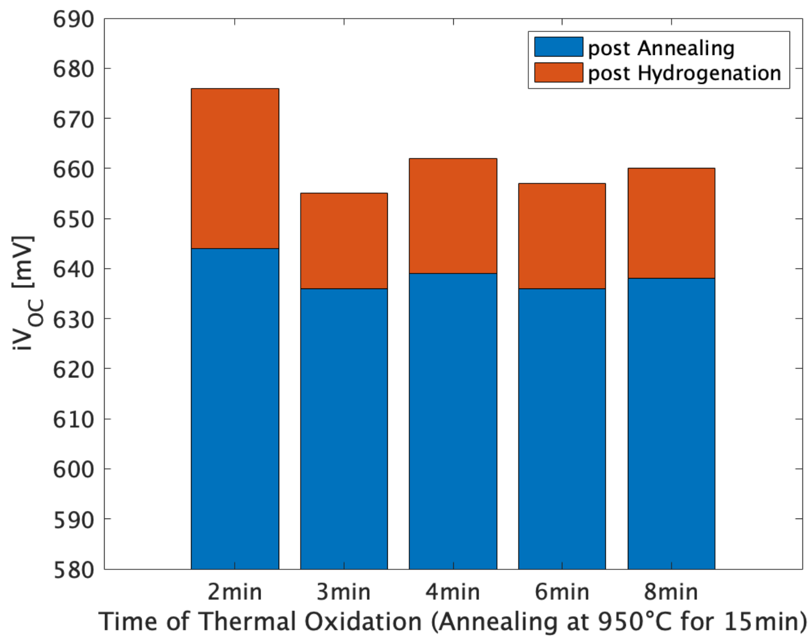


Figure 71: Comparison of the implied open-circuit voltage of textured p-type symmetric samples with different silicon oxide thickness after annealing at 950 °C (blue) and after hydrogenation (orange).

A.2 Polished p-type symmetric sample

At the beginning of the project, a double-side polished (DSP) solar cell was investigated since the textured p-type contact displays a lower open-circuit voltage. Therefore, polished p-type symmetric samples were fabricated. As shown in Figure 72, a trend of a slightly higher iV_{OC} was observed for higher annealing temperatures. However, since the passivation of the polished n-type symmetric sample deteriorates strongly above 900 °C it was decided to move forward with annealing conditions at 900 °C for 15 minutes. In Figure 73 and 74, the iV_{OC} after hydrogenation and the charge carrier minority lifetime after a high temperature annealing at 900 °C is given for different silicon oxide (SiO_x) thicknesses, respectively. The maximum iV_{OC} is about 712 mV and the maximum lifetime about 4 ms at processing conditions of 675 °C for 3 minutes.

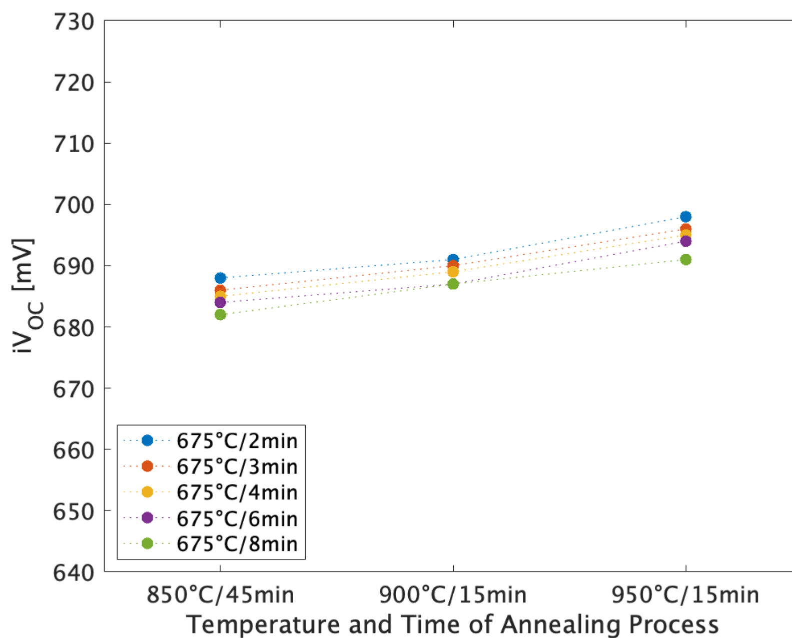


Figure 72: Comparison of the implied open-circuit voltage of polished p-type symmetric samples with different silicon oxide thickness and different annealing conditions.

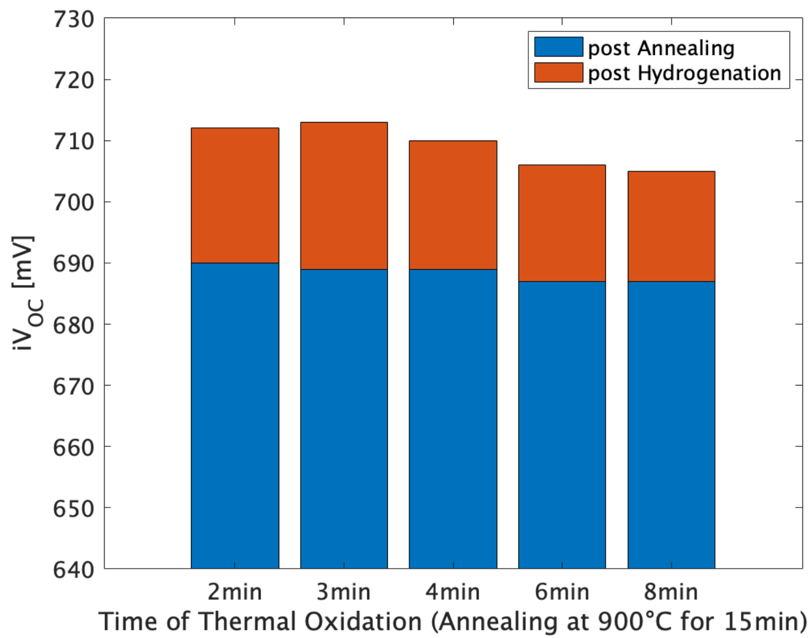


Figure 73: Comparison of the implied open-circuit voltage of polished p-type symmetric samples with different silicon oxide thickness after annealing (blue) and after hydrogenation (orange).

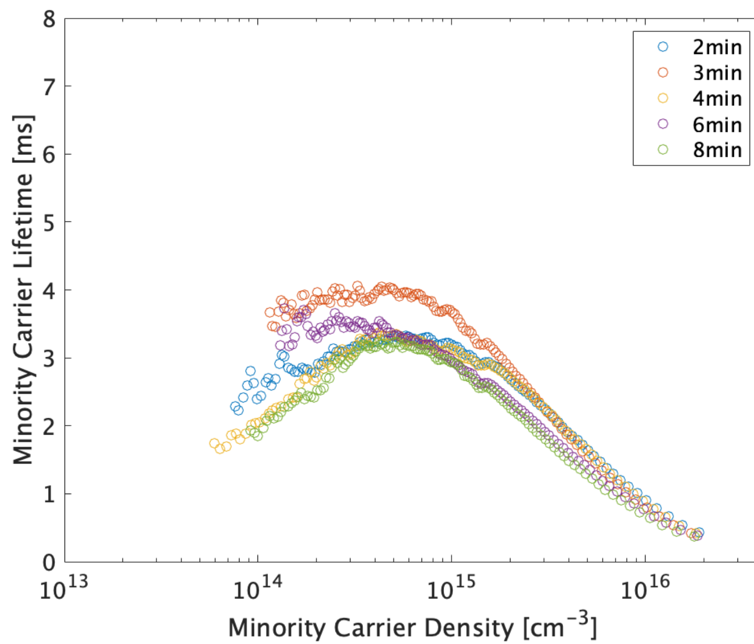


Figure 74: Comparison of the minority carrier lifetime as a function of the minority carrier density of polished p-type symmetric samples with different silicon oxide thickness after hydrogenation.

A.3 Double-side polished and textured solar cell

As mentioned in Section A.2, a double-side polished (DSP) solar cell was initially fabricated for integration in a tandem device. However, the tandem device displayed a low fill factor. Hence, the focus was directed on the single-side textured (SST) solar cell as the c-Si bottom cell. Moreover, a double-side textured (DST) solar cell was fabricated to investigate the influence on the J_{SC}. In this section, the J-V curves, the final device parameters and the EQE curves of the DSP, the DST, the SST solar cell as fabricated in Chapter 5 and the SST solar cell with the improved TCO recovery annealing as discussed in Section 6.1 are compared in Figure 75 and 76. As expected, the J_{SC} increases strongly from the DSP to the SST and the DST solar cell due to enhanced light in-coupling. This can also be observed in the EQE. Especially between 600 and 1200 nm a clear increase in EQE is observed which is mainly related to a decrease in reflection when compared to the optical simulations in Chapter 6. Even though the DST solar cell has a lower iV_{OC} the great increase in J_{SC} results in an overall efficiency of 20 %.

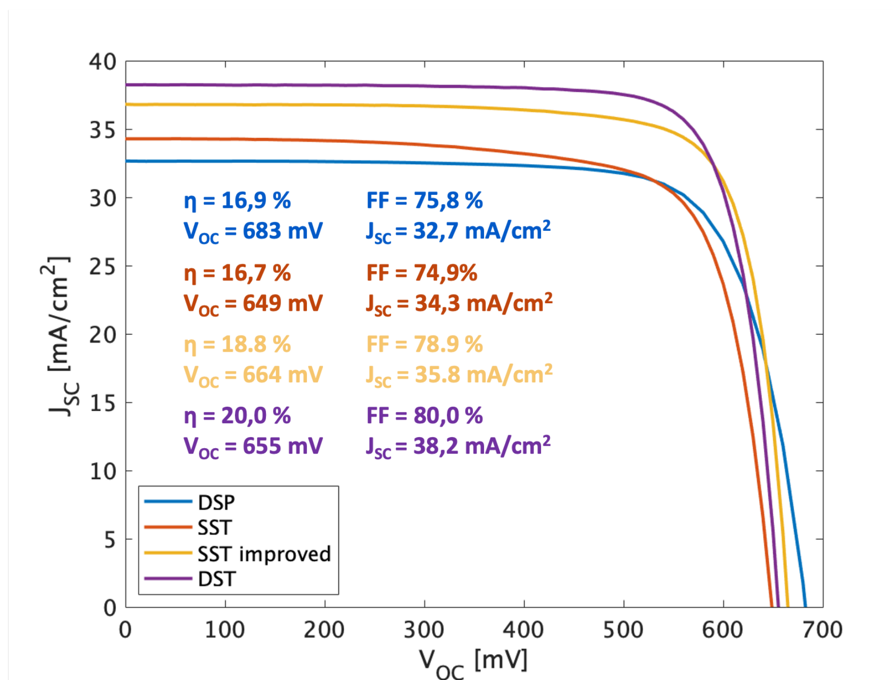


Figure 75: Comparison of the J-V curves and final device parameters for the different solar cell designs.

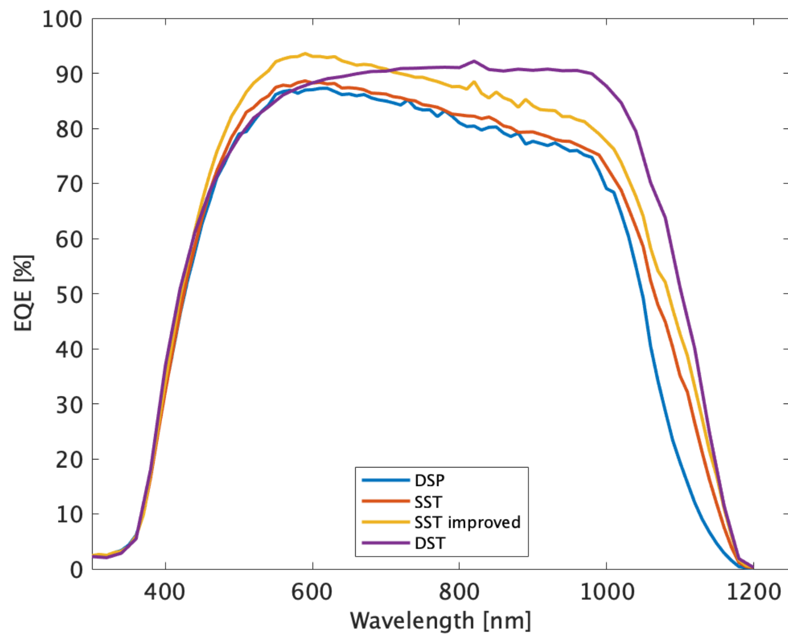


Figure 76: Comparison of the EQE curves for the different solar cell designs.

A.4 Thickness study of a-Si and a-SiO_x for textured p-type symmetric samples

An experimental series about the thickness of the amorphous silicon (a-Si) and the amorphous silicon oxide (a-SiO_x) layer in textured p-type symmetric samples was performed to investigate the influence on the passivation properties. The samples were prepared with three different a-Si layers (5, 10 and 30 nm) and three different a-SiO_x layers (10, 30 and 50 nm) and were annealed at three different annealing conditions as already described in Chapter 4. In Figures 77 - 82, the iV_{OC} before and after hydrogenation for those samples is presented. It is important to note that during the sample preparation, isopropyl alcohol (IPA) was not used during the Marangoni drying process. This might have influenced the samples and lowered the passivation quality. It can be observed that thicker layers display a higher iV_{OC}. Furthermore, the thickness of the a-Si layer, which is deposited directly onto the SiO_x passivating layer, seems to impact the iV_{OC} to a greater extent than the thickness of the a-SiO_x layer. For future research, it would be interesting to investigate the crystal structure and composition of the poly-SiO_x layer after the high temperature annealing and the influence of the transparent conductive oxide (TCO) sputtering process on the passivation quality of the different layer thicknesses.

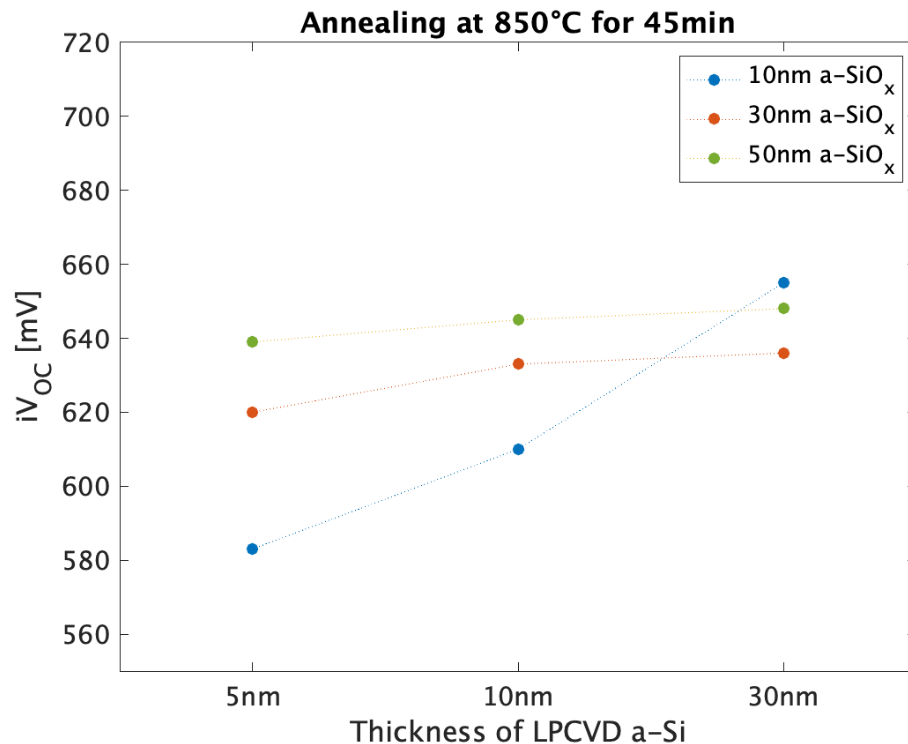


Figure 77: The change of the iV_{OC} with varying the thickness of the a-Si and the a-SiO_x layer at a high temperature annealing at 850 °C for 45 minutes.

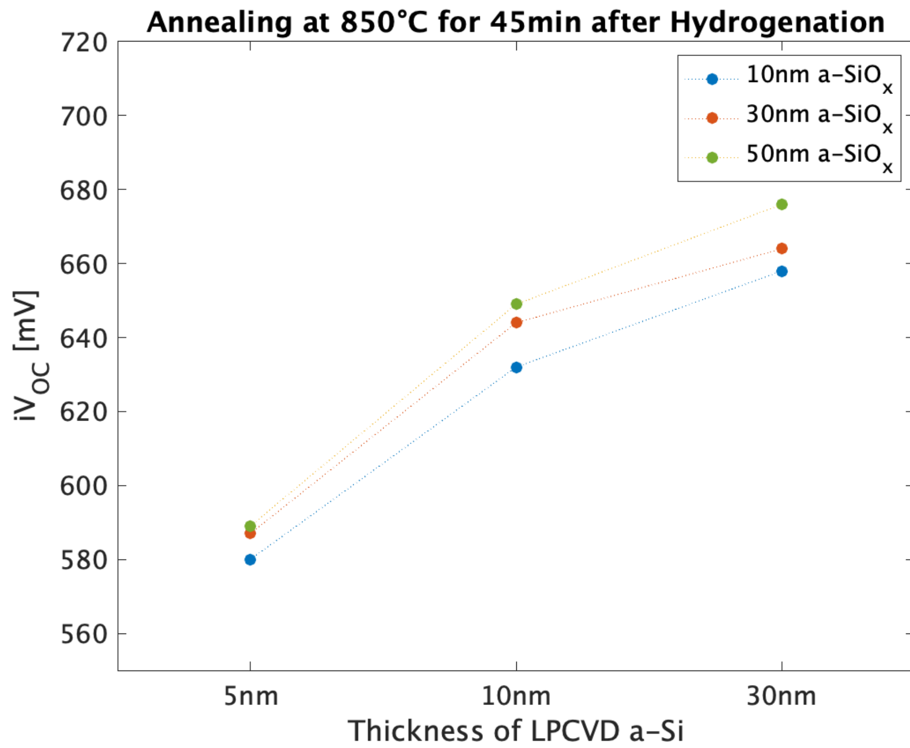


Figure 78: The change of the iV_{OC} with varying the thickness of the a-Si and the a-SiO_x layer at a high temperature annealing at 850 °C for 45 minutes after hydrogenation.

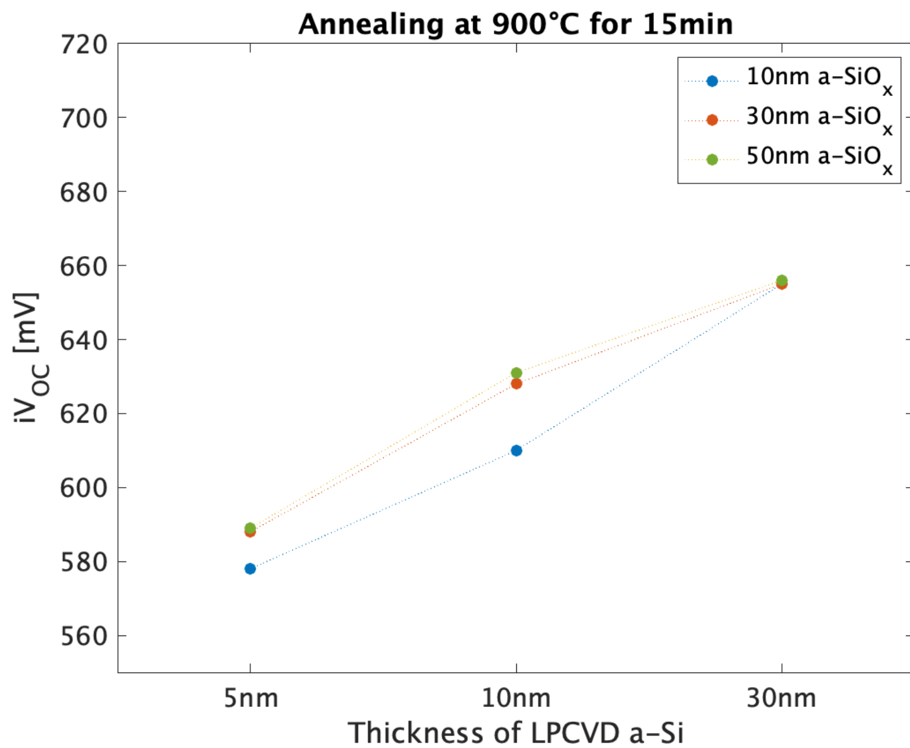


Figure 79: The change of the iV_{OC} with varying the thickness of the a-Si and the a-SiO_x layer at a high temperature annealing at 900 °C for 15 minutes.

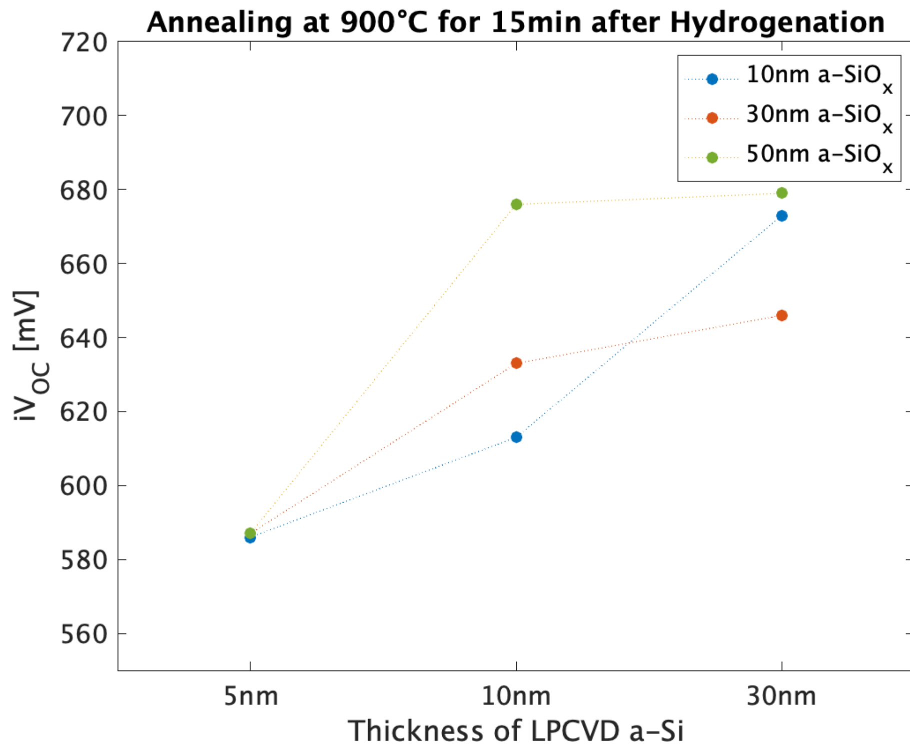


Figure 80: The change of the iV_{OC} with varying the thickness of the a-Si and the a-SiO_x layer at a high temperature annealing at 900 °C for 15 minutes after hydrogenation.

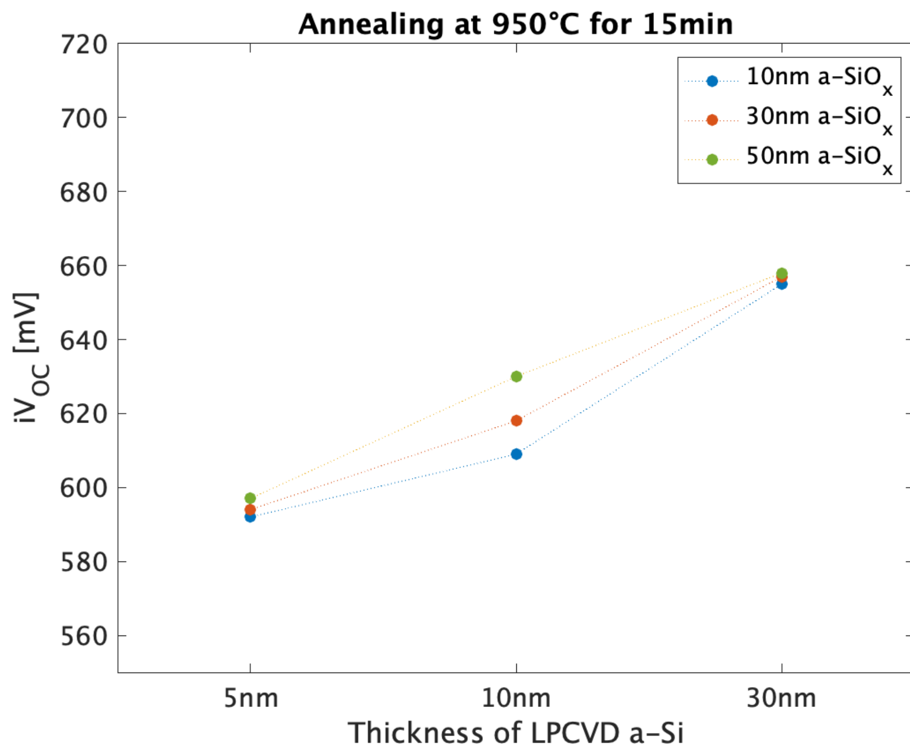


Figure 81: The change of the iV_{OC} with varying the thickness of the a-Si and the a-SiO_x layer at a high temperature annealing at 950 °C for 15 minutes.

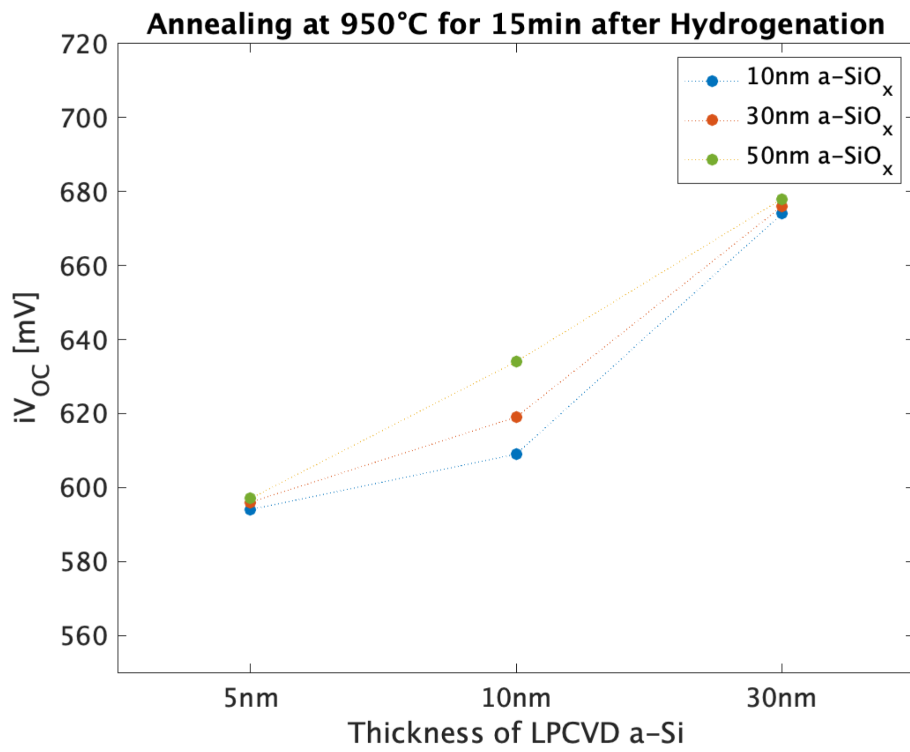


Figure 82: The change of the iV_{OC} with varying the thickness of the a-Si and the a-SiO_x layer at a high temperature annealing at 950 °C for 15 minutes after hydrogenation.

A.5 Comparison of J-V measurements of different TCO schemes

As described in Chapter 6, different TCO architectures were investigated. In Figure 83 the parameters of the solar cell after the metallization process but before the post metallization annealing at 250 °C are depicted. In comparison to Figure 57, the iV_{OC} of the three different samples is relatively similar between 650 and 655 mV. Therefore, the samples behave differently upon the annealing. It is not exactly clear why this is the case. A possible explanation are process related differences during the deposition of various layers, the uniformity of the polycrystalline silicon oxide (poly-SiO_x), the etching of the SiN_x or the sputtering damage. Furthermore, the J-V curves and the final parameters of the solar cells are given in Figure 84.

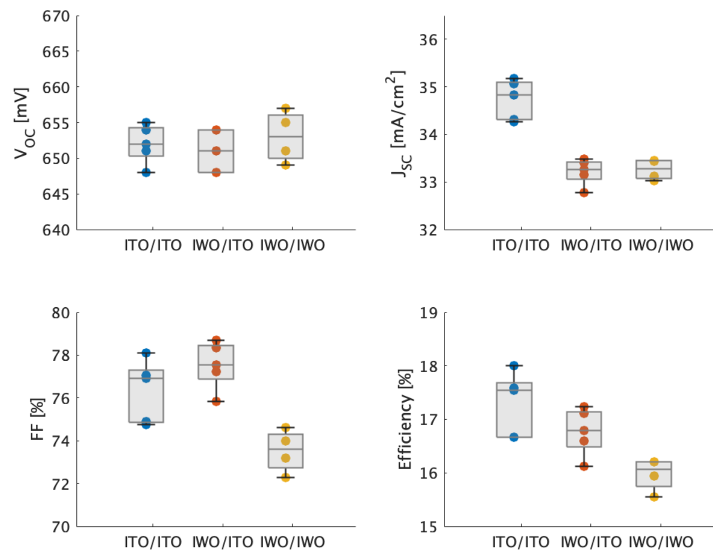


Figure 83: Comparison of the different TCO schemes after screen printing but before the post-metallization annealing.

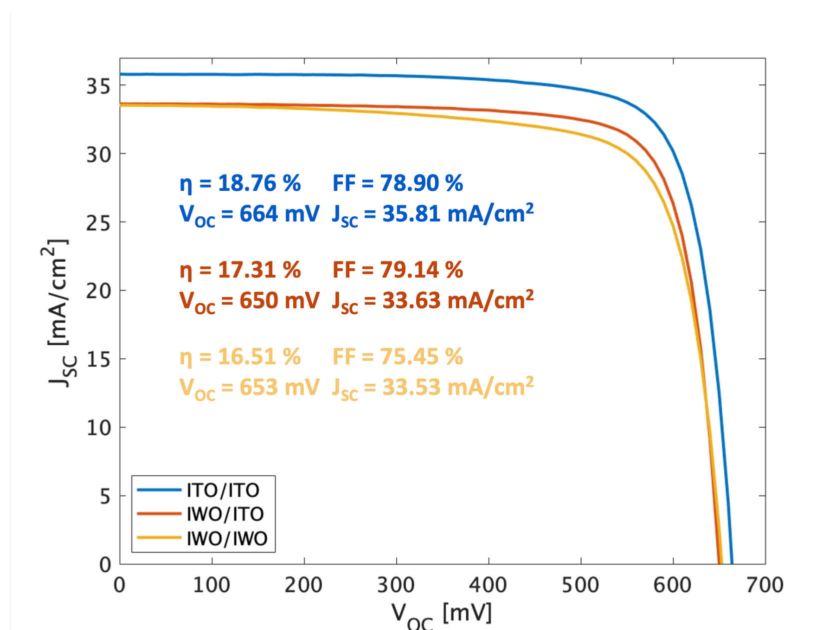


Figure 84: Comparison of the J-V curves for the different TCO schemes and final device parameters.