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5.8 A 20W CMOS/LDMOS All-Digital Transmitter with Dynamic Retiming and Glitch-Free Phase Mapper, Achieving 68%/62% Peak Drain/System Efficiency

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Base stations account for 73% of wireless-operators' energy consumption, mainly dominated by their analog-PA-based TXs [1]. All-digital transmitters (DTXs), leveraging custom low-V_T RF-power technologies [2], offer substantial energy savings by using switching operation and completely eliminating quiescent currents. In addition, DTXs enable extreme bandwidths since their circuit topology is frequency-agile up to the (power combining) output-matching network. To date, no high-power, high-efficiency DTX solutions have been reported that offer RF-power levels required for mMIMO base stations (P_{avg} >3W), with the essential fine-gate segmentation and glitch-free operation to support wideband modulated signals. In this work, an 8-phase multi-phase (MP) DTX upconversion with dynamic retiming and a glitch-free phase-mapper operation is proposed (Fig. 5.8.1). The required output power, resolution, and sampling speed are achieved via a high-density flip-chip DTX approach with a high-speed DTX controller placed on a custom low-V_T LDMOS MMIC featuring power switch banks with in-finger gate segmentation (Fig. 5.8.1).

The high-power DTX configuration uses current scaling in combination with a push-pull Class-B harmonic output match [3]. It uses reduced duty cycle (d=25%) current pulses to achieve an excellent trade-off between the peak drain efficiency (90%) and RF-power utilization of the switch banks, which is only 20% reduced compared to the analog Class-B operation [3]. In polar operation, the drain efficiency is independent of the modulation phase. In signed cartesian (SC) operation having four activation phases, or MP operation having eight possible activation phases, the current summation yields a complex loading for the switch bank segments due to the phase difference between the A and B activation vectors, restricting their theoretical phase-averaged drain efficiency (for d=25%) to 70.7% and 85.4% for the SC and MP, respectively [3]. Although a polar TX can be energy efficient, it is unable to handle wideband-modulated signals due to its bandwidth expansion [4]. In contrast, the push-pull SC operation benefits from its linear orthogonal I-Q summation, making it suitable for wideband-modulated signals [4,5]. However, the SC operation is considered less attractive for most TX applications due to its low phase-average drain efficiency. In contrast, the MP operation offers a significantly higher theoretical phase-average drain efficiency (85.4% for d=25%) but is more challenging in retiming the amplitude and phase data due to the higher-precision phase mapping (8 instead of 4 possible activation phases) and the non-orthogonal summing of the two (A and B) vectors causing glitches that affect the activation of the switch-bank gate segments and, as such, the achievable spectral purity. Conventional SC/MP implementations apply static retiming on the data at the edges of the banks using a fixed primary clock. Within their unit cells, the data is retimed based on the phase clocks to avoid data changes during the activation of a gate segment. However, after the phase mapper, the clock lines distributing the phases can no longer be retimed with a primary clock. Minimizing the mismatch between the phase clocks and digital primary clocks becomes critical in larger-power switch banks (e.g., see Fig. 5.8.7) due to the larger clock tree and longer data lines. Even with perfect timing at the edge of the bank, the data and clock paths within the bank differ, yielding an inevitable mismatch at the unit cells depending on the unit cell location within the bank. Moreover, the moment of activation of the RF cycle, provided by the phase clocks, depends on the selected phases. In multi-phase operation, the activation can start at any 45-degree shifted moment within an RF cycle, yielding a required timing alignment of $t=1/(8F_c)$.

So far, literature has not provided a solution for retiming a phase-dependent DTX activation. Consequently, we propose here the dynamic retiming schedule in Fig. 5.8.2. Depending on the phase information, retiming is applied on either the positive or the negative edge of the primary clock. By enabling retiming on both edges, the time between retiming the magnitude data at the bank edges and activation at the correct phase is at least half an RF cycle, limiting the retiming precision to $1/(2F_c)$. The advantage of dynamic retiming is shown in measurements using an SSB signal of 190MHz. This signal is constructed using only one activation phase per RF cycle (A or B), with a 45-degree decreasing phase for each RF cycle, yielding a different activation moment in each RF cycle (as illustrated in Fig. 5.8.2). Each ninth RF cycle should have no activation. With dynamic retiming, a perfect matching of the data and activation phase is obtained (Fig. 5.8.2). In contrast, conventional retiming results in mismatches, leading to large errors in the constellation diagram and a heavily compromised the spectral purity (Fig. 5.8.2).

The 25%-RF-duty-cycle activations for the gate segments are created in the unit cell from two pairs of 50%-duty-cycle global clocks (K_A[0:1] and K_B[0:1], representing phase A and phase B). These pseudo-differential clocks are fully symmetrical and benefit from their reduced even-harmonic content and speed requirements. This technique has been employed in an SC phase mapper but not yet in an 8-phase MP mapper [6]. Straightforward expansion of the 4-phase to 8-phase phase-mapper circuitry yields undesired 25%-duty-cycle events in K_A and K_B and glitches in the case of timing mismatch; in addition, it cannot provide correct switching from θ=90° to θ=0° (Fig. 5.8.3). Consequently, a new phase mapper is proposed (Fig. 5.8.3), offering glitch-free phase mapping based on a hold signal that keeps the output state high or low when the phase mapper switches from an input clock to its complementary clock (e.g., from CLK_0 to CLK_{180}, which relates to a 90-degree phase shift in the A vector). The hold signal is created from a phase-change detector, which checks if a modulation phase shift occurs (red outlined circuit, Fig. 5.8.3), and from a period-shift block (blue outlined). Doing so, we ensure that one 50% clock always defines the rising edge of the activation and another 90° phase-shifted 50% clock defines the falling edge, guaranteeing a constant gate-segment-activation time independent of a changing modulation phase. Lastly, the schedule prevents an activation at the end of the RF cycle from being succeeded directly by another activation, avoiding an undesired 50% activation and related significant error (Fig. 5.8.3).

All-digital-TX works primarily focus on low-power CMOS single-chip solutions. When targeting higher powers (e.g., >10W), the low breakdown voltage of CMOS proves problematic. For higher power, typically a two-chip approach is followed using a high-speed DTX CMOS controller and an LDMOS power MMIC, which allows full 'ON' and 'OFF' switching of its gate segments by the low-voltage CMOS drivers (e.g., 2.5V in [2]). Previously reported high-power DTX implementations used bond wires between the CMOS drivers and the gate segments on the power-MIMC, limiting the achievable DTX resolution and speed [2]. In this work, a high-power DTX high-density flip-chip approach is used (Fig. 5.8.1) [7], enabling gate segmentation directly within the fingers of an RF power device. Following this concept, a DTX push-pull switch bank is implemented in a custom low-V_T LDMOS technology (Fig. 5.8.7), which is driven by a 40nm CMOS controller. It provides 12 bits of resolution by adopting a two-level thermometer gate segmentation. The first layer consists of 255 LDMOS segments with a gate width (W_G) of 38µm, and the second layer consists of 2×7 segments with W_G=5µm.

The resulting power-DTX test configuration was characterized for maximum output power and drain/system efficiency directly at the RF-output connector, yielding 16W and 54/49%, respectively, as well as at the DTX output plane (Fig. 5.8.4) through de-embedding the losses of the balun and connecting traces, using a separate board that duplicates the output matching network, yielding 20W and 68/63%, respectively. The effectiveness of the fine-gate segmentation is reflected by the smoothness of the measured ACW-to-P_{RFout} transfer curve (Fig. 5.8.4), which outperforms [3]. The introduced dynamic-retiming concept with its proposed phase mapper was evaluated using a wideband (53MHz) single-sideband test, resulting in CIM3/IQ Image/LO Leakage of -38/-40/-46dBc after only a static calibration (Fig. 5.8.4). Using the same calibration, the power DTX was also characterized with modulated signals (Fig. 5.8.5). The EVM levels were found to be –35.7/–30.4dB for 13MHz 256-QAM and 53MHz 64-QAM signals, respectively. Both ACLR and EVM were limited mainly by imperfections in the 1.1V-supply-domain decoupling rather than by the resolution of the switch banks, as can be seen in Fig. 5.8.5, which shows constant ACLR and EVM levels vs. power back-off.

In conclusion, a new approach for realizing high-power, high-resolution DTX is proposed based on a CMOS controller, high-density flip-chip interconnected to a low-V_T LDMOS MMIC containing gate-segmented switch banks with low layout losses. By adopting the MP operation with 25%-duty-cycle current pulses, a high drain/system efficiency is achieved, with improved spectral purity for the large switch banks through dynamic retiming and a glitch-free phase-mapper.

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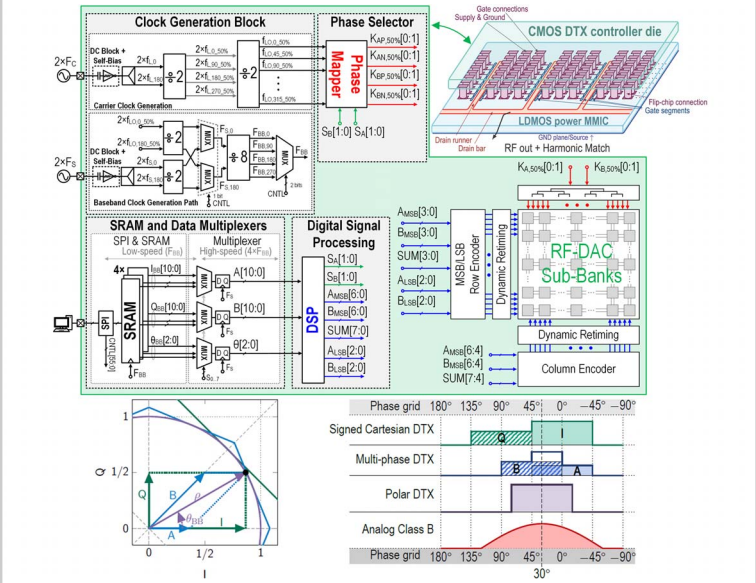
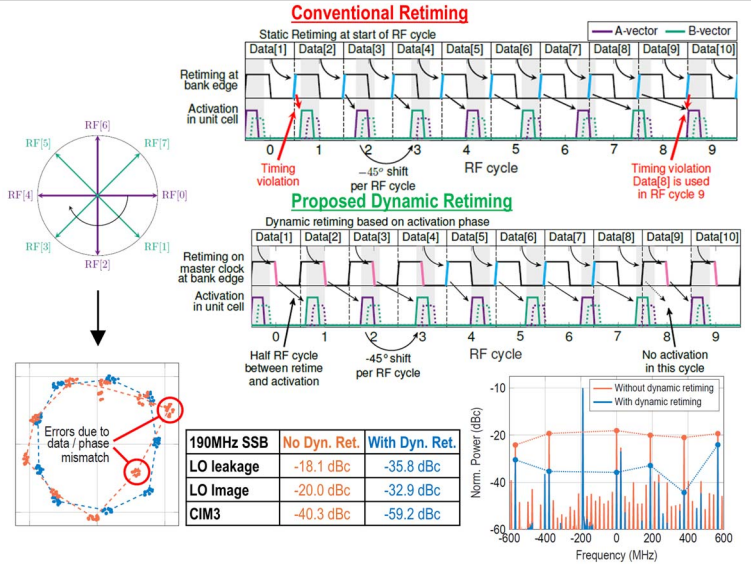


Figure 5.8.1: The block diagram of the proposed flip-chipped CMOS/LDMOS DTX and the operation principle of the multi-phase operation using 8 activation phases.



190MHz SSB	No Dyn. Ret.	With Dyn. Ret.
LO leakage	-18.1 dBc	-35.8 dBc
LO Image	-20.0 dBc	-32.9 dBc
CIM3	-40.3 dBc	-59.2 dBc

Figure 5.8.2: Conventional data retiming and proposed dynamic-data-retiming schedule at the bank edges (after row/column encoders) and the SSB measurement of both techniques.

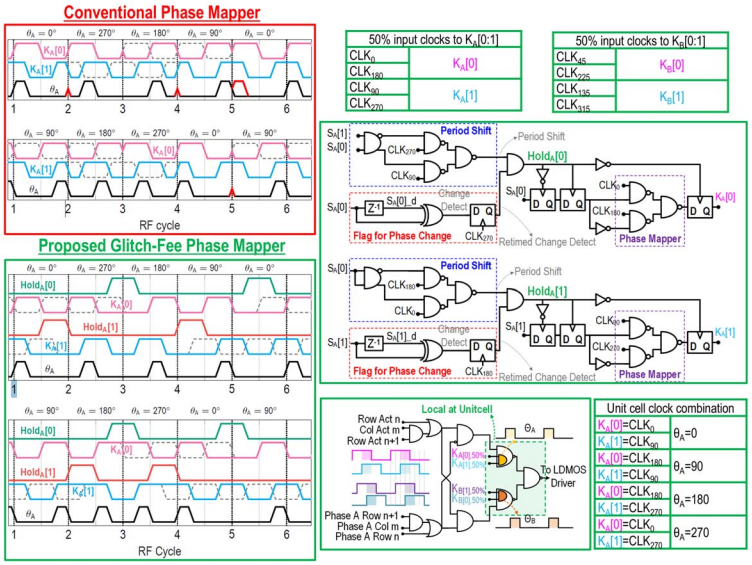


Figure 5.8.3: Timing diagram and circuit of the proposed phase mapper creating glitch-free switching between eight different phases.

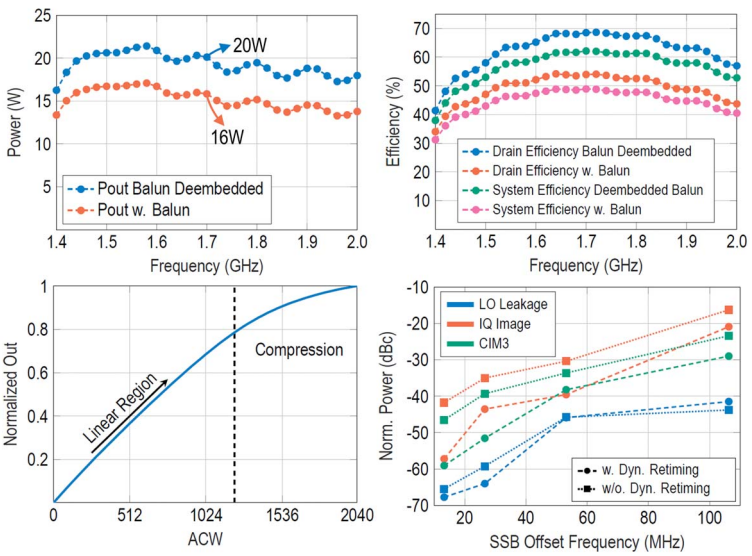


Figure 5.8.4: Peak power and peak efficiency vs. frequency (top), ACW-AM curves (bottom left), and single-sideband measurement results (bottom right).

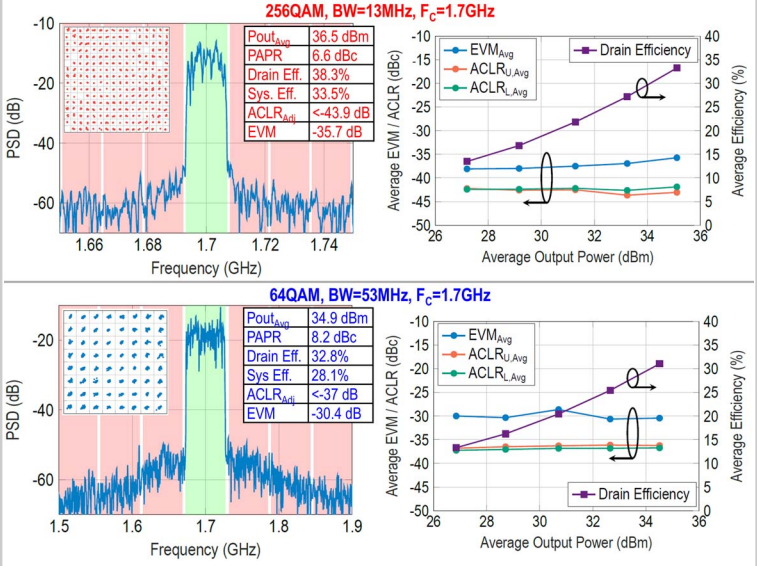


Figure 5.8.5: Measurements of 13MHz 256-QAM and 53MHz 64-QAM modulated signals.

	This Work		IMS2022 [12] R. Bootsman	ISSCC 2023 [8] J. Li	CSISC 2015 [9] V. Diddi	JSSC 2022 [4] C. Hu	ISSCC2021 [10] B. Yang	JSSC 2022 [11] Y. Li	JSSC 2021 [3] M. Beikmirza
Technology	CMOS 40nm / LDMOS		CMOS 40nm / LDMOS	28nm CMOS	0.18um SOI CMOS	40nm CMOS	40nm CMOS	55nm CMOS	40nm CMOS
Architecture	Multi-phase Current-Scaling		Polar Current-Scaling	I/Q Switched Capacitor	Polar Current Mode	Current Mode with Capacitive DAC	I/Q Switched Capacitor	I/Q Switched Capacitor	I/Q Current Mode
Die Area	3.5mm²		7.8mm²	3.6mm²	5.5mm²	1.96mm²	2.2mm²	1.2mm²	3.6mm²
Frequency	1.7 GHz		1.77 GHz	2.9 GHz	0.9 GHz	1.5 GHz	2.4 GHz	0.85 GHz	5.4 GHz
Peak P_{out}	43 dBm		45.9 dBm	36.1 dBm	31.6 dBm	20 dBm	30.3 dBm	29.3 dBm	27.4 dBm
Peak Efficiency Drain / System	68% / 63%		57% / 55%	N/A / 33.6%	65.9% / N/A	N/A / 23.7%	41.3% / 36.5%	N/A / 43.1%	47.4% / 30.6%
Modulation	13 MHz 256QAM	53MHz 64QAM	7 MHz 256QAM	20 MHz 64QAM LTE	5 MHz WCDMA	20 MHz 64QAM LTE	40 MHz 1024QAM	20 MHz 64QAM WLAN	320 MHz 512QAM OFDM
PAPR	6.6 dB	8.8 dB	5.5 dB	6.7 dB	3.3 dB	5.8 dB	9.9 dB	8.3 dB	9.41 dB
EVM	-35.7dB	-30.4dB	-48.0dB	-25 dB	N/A	-26.5 dB	-35.9 dB	-25 dB	-29.7 dB
ACLR	-43.9dB	-37dB	-52dB	N/A	N/A	N/A	N/A	N/A	-35 dB
Average Efficiency Drain / System	38% / 33%	33% / 28%	49% / 46%	N/A / 18.5%	49.5% / N/A	N/A / 12.1%	30.7% / N/A	N/A / 20.1%	22.17% / 20.52%

Figure 5.8.6: Performance summary and comparison to prior works.

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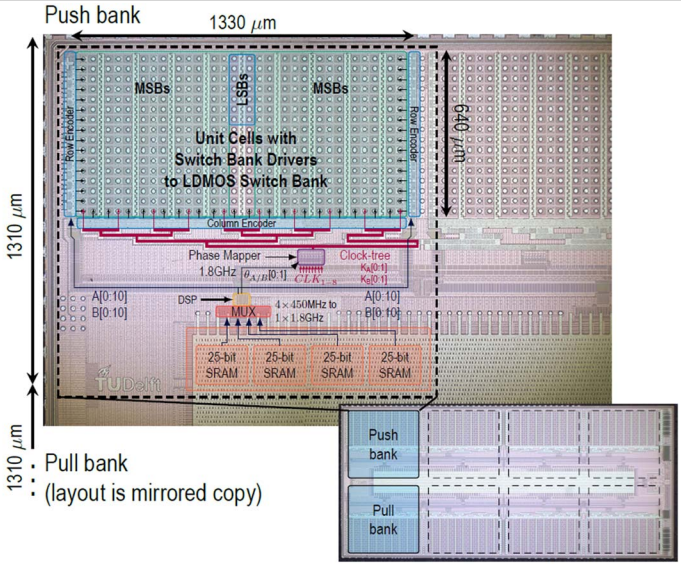


Figure 5.8.7: Micrograph of the CMOS die showing the push bank. The pull bank is a mirrored copy of the pull bank. The full die (bottom right) consists of 8 banks (6 are not used).

References:

[1] S. Wesemann, J. Du and H. Viswanathan, "Energy Efficient Extreme MIMO: Design Goals and Directions," in *IEEE Communications Magazine*, vol. 61, no. 10, pp. 132-138, October 2023.

[2] R. J. Bootsman et al., "High-Power Digital Transmitters for Wireless Infrastructure Applications (A Feasibility Study)," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 5, pp. 2835-2850, May 2022.

[3] D. P. N. Mul, R. J. Bootsman, M. Beikmirza, M. S. Alavi and L. C. N. de Vreede, "The Efficiency and Power Utilization of Current-Scaling Digital Transmitters," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 7, pp. 4350-4366, July 2024.

[4] C. Hu, Y. Yin, T. Li, Y. Liu, L. Xiong and H. Xu, "A Fully-Integrated Wideband Digital Polar Transmitter With 11-bit Digital-to-Phase Converter in 40nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 2, pp. 462-473, Feb. 2023.

[5] M. Mehrpoo, M. Hashemi, Y. Shen, R. van Leuken, M. S. Alavi and L. C. N. de Vreede, "A wideband linear direct digital RF modulator using harmonic rejection and I/Q-interleaving RF DACs," *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, USA, 2017, pp. 188-191.

[6] M. Beikmirza, Y. Shen, L. C. N. de Vreede and M. S. Alavi, "A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3768-3783, Dec. 2021.

[7] R.J. Bootsman, et al, "A Switch-Bank Approach for High-Power, High-Resolution, Fully-Digital Transmitters," *2024 54th European Microwave Conference (EuMC)*, Paris, France, 2024, pp. 23-26.

[8] J. Li et al., "A 4.1 W Quadrature Doherty Digital Power Amplifier with 33.6% Peak PAE in 28nm Bulk CMOS," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 1-3.

[9] V. Diddi, H. Gheidi, Y. Liu, J. Buckwalter and P. Asbeck, "A Watt-Class, High-Efficiency, Digitally-Modulated Polar Power Amplifier in SOI CMOS," *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, New Orleans, LA, USA, 2015, pp. 1-4.

[10] B. Yang, H. J. Qian and X. Luo, "A Watt-Level Quadrature Switched/Floated-Capacitor Power Amplifier with Back-Off Efficiency Enhancement in Complex Domain Using Reconfigurable Self-Coupling Canceling Transformer," *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021, pp. 362-364.

[11] Y. Li et al., "A 15-Bit Quadrature Digital Power Amplifier With Transformer-Based Complex-Domain Efficiency Enhancement," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1610-1622, June 2022.

[12] R. Bootsman et al., "A 39 W Fully Digital Wideband Inverted Doherty Transmitter," 2022 IEEE/MTT-S International Microwave Symposium - IMS 2022, Denver, CO, USA, 2022, pp. 979-982.

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