HIGH EFFICIENCY, HIGHLY INTEGRATED DC-DC CONVERTER FOR 48V DATA CENTERS WITH STANDARD CMOS AND GAN DEVICES

A thesis submitted to the Delft University of Technology in partial fulfillment
of the requirements for the degree of

Master of Science in Electrical Engineering

by

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August 2022

Yuan Hua: *High efficiency, highly integrated DC-DC converter for 48V data centers with standard CMOS and GaN devices* (2022)

The work in this thesis was made in the:

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Department of Microelectronics
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ABSTRACT

This thesis presents a 48V-to-1V 10-level dual inductor hybrid converter (DIHC) containing 11 on-chip switches and an off-chip Gallium Nitride (GaN) switch. Thanks to the 10-level Dickson switched-capacitor (SC) circuit, most of the voltage stress will be taken over by off-chip capacitors, which reduces the voltage stress of each switch to 4.8 V and takes full advantage of the voltage pressure on the 5-V on-chip transistors. This proposed structure is implemented in a 0.18-μm BCD process to convert 48-V input to 1-V output with up to 18-A current load. The post-layout simulations show that a peak power efficiency of 90.6% can be achieved at 5.2-A loading and the power density is about 2093 W/in^3 considering the power stage volume.

This thesis also proposes a 48V/3V multi-resonant DC-DC converter for data center applications, consisting of a 3Φ-SC stage and a 4-to-1 series-parallel stage. Thanks to the multi-phase resonant operation mode, the converter uses fewer components to achieve the same voltage conversion ratio as the conventional two-phase SC converters, and can further improve the efficiency by realising soft-charging. This topology is simulated in cadence spectre, and achieves a peak efficiency of 96.94%, and 95.0% full load efficiency at 30-A load.

Keywords: hybrid dc-dc converter, 10-level, 48V-to-1V, switched capacitor, GaN switch, 5-V on-chip, resonant, multi-phase, voltage conversion ratio, soft-charging

ACKNOWLEDGEMENTS

Two years are about to pass, and my master study is coming to an end. Over the past two years, I have spent an extremely fulfilling and happy time in TU Delft. I really appreciate all things that have happened and everyone I have met.

The deepest gratitude goes to my supervisor Dr. Sijun Du for his guidance and advice on my thesis research. It is a great honor for me to be able to complete my thesis under his supervision. I want to express my gratitude for his patience and tolerance. In addition, I am also thankful to Prof.dr.ir. Wouter A. Serdijn and Dr. Tomás Manzaneque to be my committee.

Besides, I would like to thank my beloved friends. Thanks Qi Lu and Shuangmu Li for their help on my thesis project. Thanks Rui Gong and Zhiyu Chen for accompanying me and chatting with me on so many late nights. Thanks my princess Xiaowei Duan to bring me a lot of happiness.

Furthermore, I am extremely grateful to my families for their supports, not only financial support, but also mental support, especially my sister, who always inspires me to pursue my interests. She graduates this year as well. Here I would like to wish her a happy graduation.

Finally, I want to express a gratitude to myself. Thanks for having the courage to study abroad during the Covid period. Thanks for never giving up in the past two years. I appreciate every choice I made and every attempt I made. Success or failure, it has shaped who I am now. I wish I could continue to be enthusiastic and happy in the future.

Yuan Hua
August 2022, Delft

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ACRONYMS

1 INTRODUCTION

1.1 RESEARCH BACKGROUND

With the rapid development of the new generation of information and communication technologies such as the Internet, cloud computing, big data and artificial intelligence, all kinds of data are showing explosive growth. As the main storage and computing entity for massive data, the data center is expanding in scale, and the resulting energy consumption is also increasing. Estimated by the International Energy Agency, data centers consume 1% of the global energy and by 2025, 1/5 of world's electricity will be used by data centers [1].

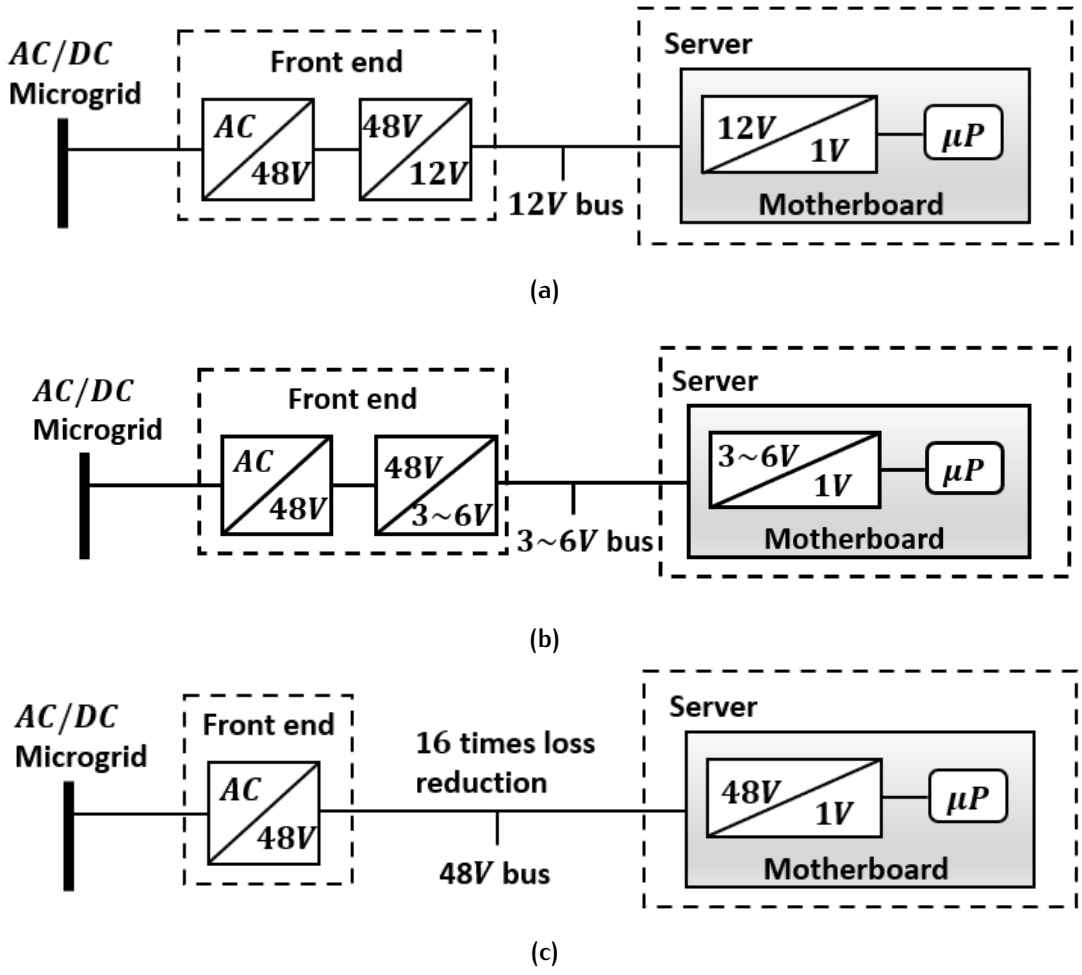

Figure 1.1: Data center power architecture [13]. (a) 12-V intermediate bus architecture. (b) 3∼6-V intermediate bus architecture. (c) Direct 48V-to-1V architecture.

Over last 20 years, 12-V intermediate bus architecture has been widely used in data centers, consisting of one 48V/12V converter and one 12V/1V converter, shown in Fig.1.1a. However according to current study [32], when both the two stages are taken into account, a lower intermediate bus voltage could offer superior overall efficiency (Fig.1.1b). To reduce the distribution loss on the 12-V power bus, the direct 48V-to-1V architecture has been proposed (Fig.1.1c). Compared to the conventional 12V/1V converter, the direct 48V/1V converter can reduce the distribution loss (I^2R) by 16 times [13].

However, for high voltage converters, achieving high efficiency and high power density has always been a nontrivial task, due to two key challenges [13].

- Extremely short on-time. For half-bridge buck converter, on-time can be calculated as:

$$t_{on} = V_{out}/(V_{in} * f_{sw}) \tag{1.1}$$

  The accuracy of on-time is affected by t_{on} and t_{off} of the power switches, the driver delay, the deadtime to avoid simultaneous conduction in both high-side and low-side switches, and elements delay in the feedback loop. The on-time can be as low as tens of nanoseconds with high input voltage and high switching frequency, making it susceptible to any delay mentioned above. Besides, the high voltage difference between the input and the output of the converter translates into high voltage stress on the power switches. Bulkier power devices have to be used, further increasing those delays. To keep enough on-time, it is necessary to utilize a low frequency. But using low frequency will necessitate larger passive components, which will increase system volume and decrease power density [34].

- Increased power losses. Switching loss scales with the input voltage.

1.2 ADVANTAGES OF GALLIUM NITRIDE POWER DEVICE

In traditional circuits, the design of power converters heavily relies on Si power devices. Such devices, however, are limited in their ability to operate efficiently when operating at high switching frequency and high voltage due to large conduction loss and switching loss. Besides, the issue of heat generation has also grown more serious as circuits become increasingly integrated [3].

As an emerging semiconductor material, GaN has the characteristics of wide bandgap, high saturation velocity, large breakdown field, high mobility, and stable chemical properties [18].

Fig.1.2 contrasts power electronic devices made of GaN materials with traditional Si devices. It can be seen that GaN devices features low on-resistance and low gate charge. This can result in low conduction and switching losses.

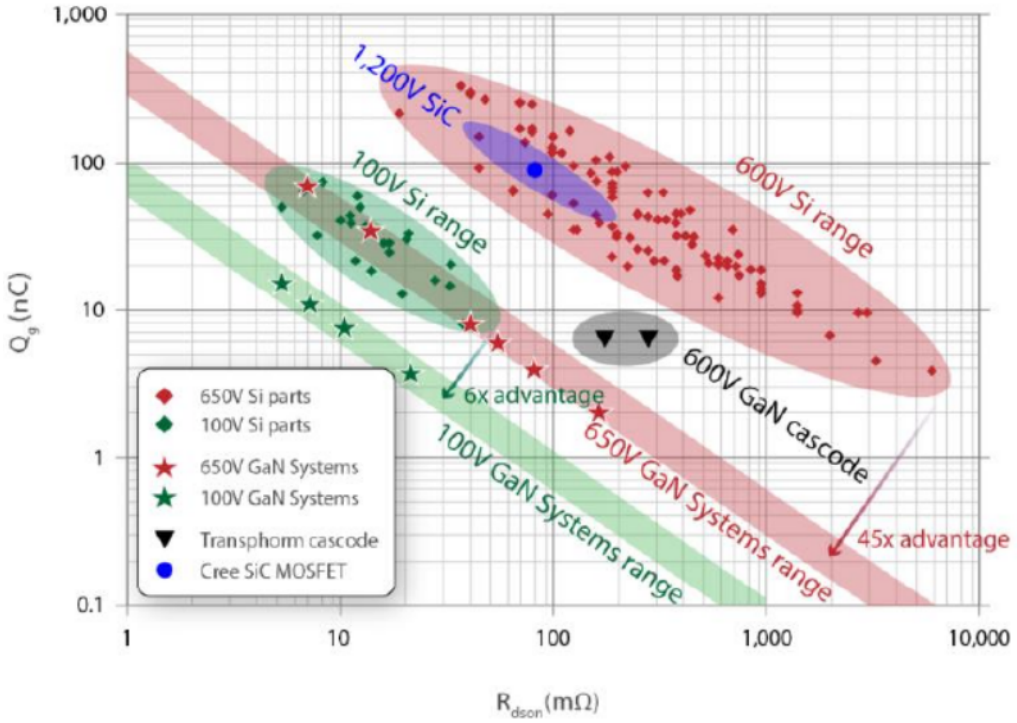

Figure 1.2: Comparison of GaN device with Si device [31]

1.3 ANALYSIS OF PRIOR-ART DC-DC CONVERTER TOPOLOGIES FOR 48-V DATA CENTERS

1.3.1 Prior arts for direct 48V/1V architecture

The most widely used topology for direct 48V/1V architecture is SC based hybrid converter, which merges a SC stage with an inductive load to achieve both high power density and soft switching [27]. In this subsection, two hybrid SC converter topologies: FCML converter and hybrid Dickson SC converter are described. A quantitative comparison between them and the basic buck converter is made to show that the hybrid converters have the potential to reduce the volume of passive components.

Flying capacitor multilevel converter

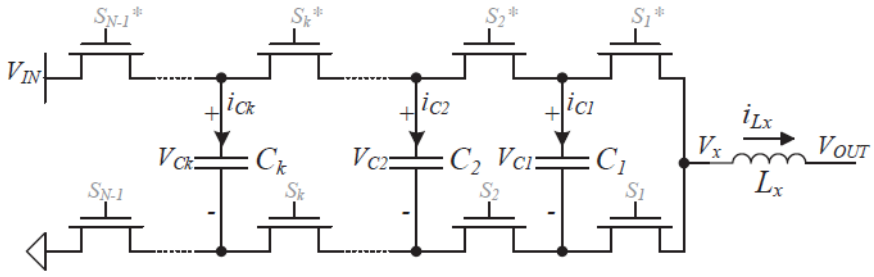

Figure 1.3: Generic N-level FCML converter [27]

Fig.1.3 shows a generic N-level FCML converter presented in [27]. $2(N-1)$ switches and $(N-2)$ flying capacitors are needed. Each pair of switches turn on and off with a $\frac{360^\circ}{N-1}$ phase shift and the voltage stress of each switch is $\frac{V_{in}}{N-1}$ [37]. $(N-1)$ times the switching frequency of switches is obtained for the switching node frequency. Thanks to the conversion ratio of the SC stage and the increase of the effective switching frequency, the size of the passive components can be significantly reduced. An example five-level FCML converter is drawn in Fig.1.4 with its operation states shown in Fig.1.5. A typical switching sequence is 1a-0-1b-0-1c-0-1d-0-1a.

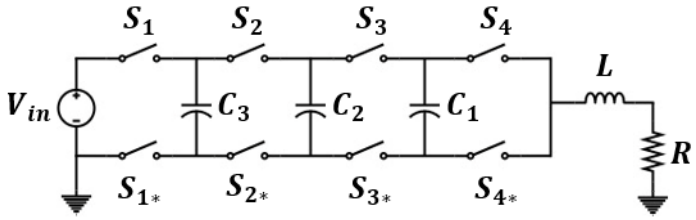

Figure 1.4: 5-level FCML converter

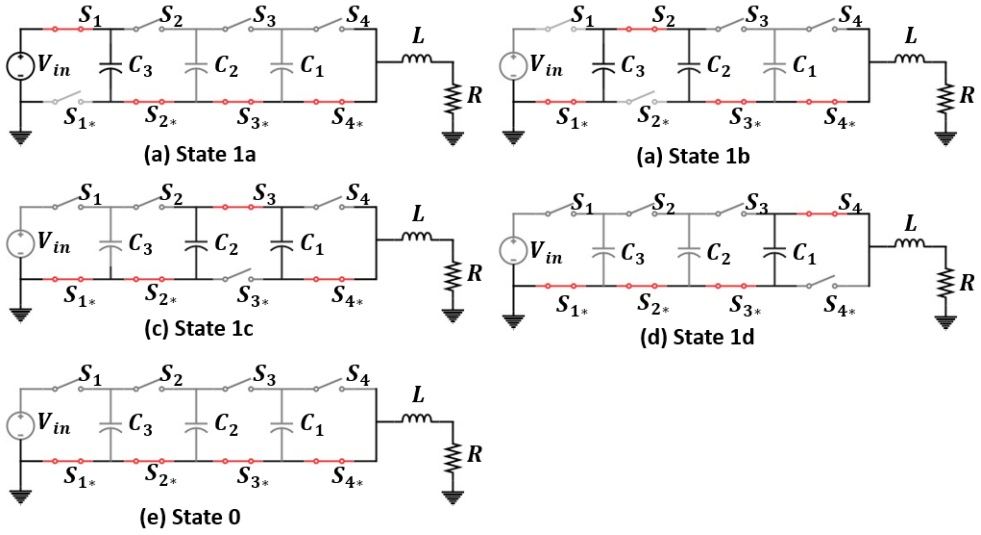

Figure 1.5: Operation states of 5-level FCML converter

The following is a quantitative comparison of the FCML converter with the buck converter [20]:

1) Determine the required switch conductance to maintain the same conduction losses:

An N-level FCML converter always has $(N-1)$ switches conducting in each state, while a buck converter always has one switch on. Thus, in order to have the same conduction loss, the relationship of the switch conductance between FCML converter and buck converter is stated as:

$$\frac{G_{FCML}}{G_{buck}} = N-1 \tag{1.2}$$

where G_{FCML} and G_{buck} are the switch conductance of FCML converter and buck converter, respectively.

2) Establish the switching frequency to have the same switching losses among all converters:

Assuming the same switch technology, switching loss is roughly proportional to the switch's GV^2 product, where G is the conductance and V is the switch blocking voltage. Thus, to achieve the same switching loss:

$$\sum(GV^2)_{FCML} \times f_{FCML} = \sum(GV^2)_{buck} \times f_{buck} \tag{1.3}$$

$$\frac{f_{buck}}{f_{FCML}} = \frac{G_{FCML}}{G_{buck}} \times \frac{2(N-1) \times (\frac{1}{N-1}V_{in})^2}{2 \times V_{in}^2} = 1 \tag{1.4}$$

Same switching frequency as the basic buck converter can be used to achieve equal conduction and switching loss.

3) Determine the inductance value:

The inductance value is often determined by the inductor current ripple. Smaller inductance is made possible by larger ripple, but the trade-off is higher core loss and ac conduction loss. The calculation of inductor value of both buck converter and FCML converter is given in Eq.1.5 and Eq.1.6, respectively.

$$L_{buck} = \frac{(1 - \frac{V_{out}}{V_{in}})V_{out}}{\Delta I_L f_{buck}} \tag{1.5}$$

$$L_{FCML} = \frac{(1 - \frac{V_{out}(N-1)}{V_{in}})V_{out}}{\Delta I_L f_{FCML}(N-1)} \tag{1.6}$$

Thus,

$$\frac{L_{FCML}}{L_{buck}} = \frac{(1 - \frac{V_{out}(N-1)}{V_{in}})}{1 - \frac{V_{out}}{V_{in}}} \frac{1}{N-1} \tag{1.7}$$

The first term on the right side of Eq.1.7 is due to the fact that the duty ratio of FCML converter is $(N-1)$ times larger than that of the buck converter, while the second term is because of the $(N-1)$ times switching frequency seen by the inductor of FCML converter. Observed from Eq.1.7, a significantly reduced inductance is needed by using FCML topology.

Energy stored in the inductor can be calculated as:

$$\begin{aligned} E_{L,FCML} &= \frac{1}{2} L_{FCML} I_L^2 \\ &= \frac{1}{2}(1 - \frac{V_{out}(N-1)}{V_{in}}) \frac{P_{out}}{\alpha_I (N-1) f_{FCML}} \end{aligned} \tag{1.8}$$

where, α_I represents the current ripple factor. Since the buck converter and FCML converter see equal inductor current, the energy ratio is the same as the inductance ratio, given in Eq.1.9.

$$\frac{E_{L,FCML}}{E_{L,buck}} = \frac{L_{FCML}}{L_{buck}} \tag{1.9}$$

Neglecting core loss and ac loss, same inductor DC conduction loss can be achieved by selecting same inductor DC resistance (DCR).

4) Determine the flying capacitance value:

For FCML converter, the voltage rating of the flying capacitors is given by:

$$V_{C,i} = \frac{i}{N-1} V_{in} \tag{1.10}$$

where, $V_{C,i}$ is the voltage rating of i-th capacitor. Assuming equal value C for all flying capacitors, thus, the energy stored in all flying capacitors can be obtained as:

$$\begin{aligned} E_{C,FCML} &= \frac{1}{2}\sum_{i}^{m} C_i V_{C,i}^2 \\ &= \frac{(N-2)(2N-3)}{12(N-1)} C V_{in}^2 \end{aligned} \tag{1.11}$$

Similar to the inductor, the capacitance value is often determined by the capacitor voltage ripple. Smaller capacitance is made possible by larger ripple, but the trade-off is higher voltage rating of capacitors and switches. Here, the capacitor ripple is selected to be a portion of minimum capacitor voltage rating, given as Eq.1.12.

$$\Delta V_C = \alpha_V \frac{V_{in}}{N-1} \tag{1.12}$$

where, α_V represents the voltage ripple factor. Thus, the capacitance value can be calculated:

$$\begin{aligned} C &= \frac{\Delta Q_C}{\Delta V_C} \\ &= \frac{(N-1) V_{out} I_{out}}{\alpha_V V_{in}^2 f_{FCML}} \end{aligned} \tag{1.13}$$

Substituting Eq.1.13 into Eq.1.11, flying capacitor energy can be obtained:

$$E_{C,FCML} = \frac{(N-2)(2N-3)}{12} \frac{P_{out}}{\alpha_V f_{FCML}} \tag{1.14}$$

5) Derive a volume metric by combining the inductance and capacitance:

To get the volume metric, $\rho_{E,L}$ and $\rho_{E,C}$ are introduced, which represent the energy density of inductors and capacitors, respectively. Thus, the volume ratio between FCML converter and buck converter can be obtained as:

$$\begin{aligned}\frac{V_{tot,FCML}}{V_{tot,buck}} &= \frac{(\frac{E_L}{\rho_{E,L}} + \frac{E_C}{\rho_{E,C}})_{FCML}}{(\frac{E_L}{\rho_{E,L}})_{buck}} \\ &= \frac{E_{L,FCML}}{E_{L,buck}}(1 + \frac{E_{C,FCML}}{E_{L,FCML}}\frac{\rho_{E,L}}{\rho_{E,C}})\end{aligned} \tag{1.15}$$

where,

$$\frac{E_{C,FCML}}{E_{L,FCML}} = \frac{(N-1)(N-2)(2N-3)}{6(1-\frac{V_{out}(N-1)}{V_{in}})} \times \frac{\alpha_I}{\alpha_V} \tag{1.16}$$

Observed from Eq.1.15, properly choosing the $\rho_{E,L}$, $\rho_{E,C}$, α_I and α_V, at a lower number of levels, the flying capacitor volumes do not contribute too much to the total volume.

However, this topology has a key challenge of flying capacitor voltage balance. In [27], current limit control is proposed to stabilise the voltage of the flying capacitor. A peak efficiency of 85% can be achieved for a 48V/2V converter. Besides, high conduction loss in the FCML converter due to multi switches in series limits its output current [13]. To reduce the conduction loss, the size of the power switches needs to be increased.

Hybrid Dickson SC converter

To efficiently utilize the switches, the hybrid Dickson SC converter is proposed. For an N-to-1 hybrid Dickson converter, $(N+4)$ switches and $(N-1)$ capacitors are needed. Fig.1.6 shows the schematic of a four-to-one Dickson topology ($M = 5$ levels) example, with its operation states shown in Fig.1.7. A typical switching sequence is 1a-0-1b-0-1a.

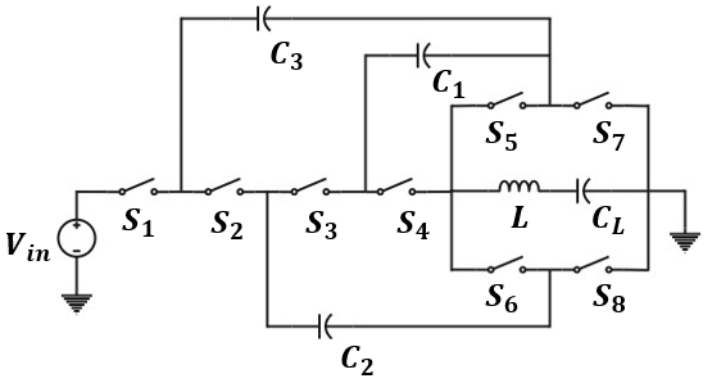

Figure 1.6: 4-to-1 Dickson SC converter

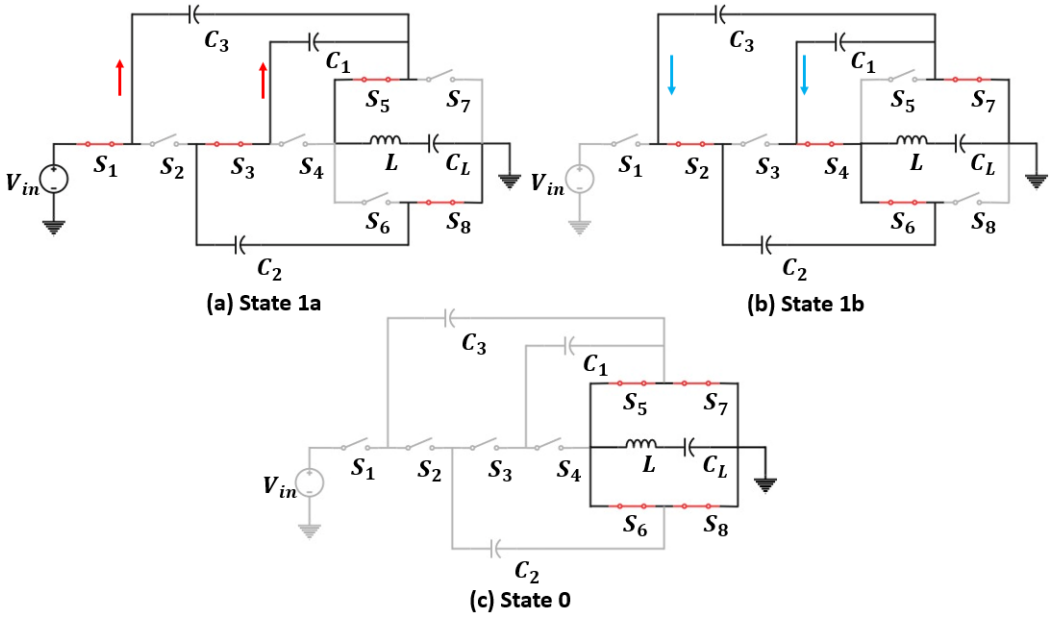

Figure 1.7: Operation states of 4-to-1 Dickson SC converter

A quantitative comparison of hybrid Dickson SC converter against the buck converter is made as follows [20]:

1) Required switch conductance to have same conduction loss:

Different from FCML converter, there are multiple branches conducting currents in each states. For an N-to-1 hybrid Dickson converter, the conduction loss is given as:

$$\begin{aligned} P_{cond} = D(\frac{2}{N}I_{rms})^2 \sum_{i}^{N} R_i + [DI_{rms}^2 + (\frac{1}{2}I_{rms})^2(1-2D)](R_{N+1} + R_{N+3}) \\ + [(\frac{N}{2}-1)\frac{2}{N}I_{rms})^2 D + (\frac{1}{2}I_{rms})^2(1-2D)](R_{N+2} + R_{N+4}) \end{aligned} \tag{1.17}$$

Assuming same on-resistance R for all switches, when N increases, Eq.1.17 approaches:

$$\begin{aligned} P_{cond} &= [1 + (1-\frac{2}{N})^2 2D + \frac{4D}{N}]I_{rms}^2 R \\ &\approx 2I_{rms}^2 R \end{aligned} \tag{1.18}$$

Thus, the switch conductance ratio of the hybrid Dickson converter and buck converter is given as:

$$\frac{G_{Dickson}}{G_{buck}} = 2 \tag{1.19}$$

2) Switching frequency to have equal switching loss:

For hybrid Dickson SC converter, the voltage rating of the switches is either $\frac{2}{N}V_{in}$ ($(N-2)$ switches) or $\frac{1}{N}V_{in}$ (6 switches).

$$\sum(GV^2)_{Dickson} \times f_{Dickson} = \sum(GV^2)_{buck} \times f_{buck} \tag{1.20}$$

$$\frac{f_{Dickson}}{f_{buck}} = \frac{N^2}{4(N-2)+6} \tag{1.21}$$

3) Inductance value:

$$L_{Dickson} = \frac{(1 - \frac{V_{out}N}{V_{in}})V_{out}}{\Delta I_L f_{Dickson} 2} \tag{1.22}$$

Thus,

$$\frac{L_{Dickson}}{L_{buck}} = \frac{(1 - \frac{V_{out}N}{V_{in}})}{1 - \frac{V_{out}}{V_{in}}} \frac{f_{buck}}{2f_{Dickson}} \tag{1.23}$$

The first term on the right side of Eq.1.23 is always smaller than 1 and approaches zero when $\frac{V_{out}}{V_{in}}$ approaches $\frac{1}{N}$ [23]. The second term is also smaller than 1, as the switching frequency of hybrid Dickson converter is usually higher than that of the buck converter.

Energy stored in the inductor can be calculated as:

$$\begin{aligned} E_{L,Dickson} &= \frac{1}{2} L_{Dickson} I_L^2 \\ &= \frac{1}{4}(1 - \frac{V_{out}N}{V_{in}}) \frac{P_{out}}{\alpha_I f_{Dickson}} \end{aligned} \tag{1.24}$$

Since the buck converter and hybrid Dickson converter see equal inductor current, the energy ratio is the same as the inductance ratio, given in Eq.1.25.

$$\frac{E_{L,Dickson}}{E_{L,buck}} = \frac{L_{Dickson}}{L_{buck}} \tag{1.25}$$

4) Flying capacitors:

For hybrid Dickson converter, the voltage rating of the flying capacitors is the same as that of FCML converter, given by:

$$V_{C,i} = \frac{i}{N} V_{in} \tag{1.26}$$

Assuming equal value C for all flying capacitors, thus, the energy stored in all flying capacitors can be obtained as:

$$\begin{aligned} E_{C,Dickson} &= \frac{1}{2}\sum_{i}^{N-1} C_i V_{C,i}^2 \\ &= \frac{(N-1)(2N-1)}{12N} C V_{in}^2 \end{aligned} \tag{1.27}$$

Here, the capacitor ripple is also selected to be a portion of minimum capacitor voltage rating, given as Eq.1.28.

$$\Delta V_C = \alpha_V \frac{V_{in}}{N} \tag{1.28}$$

Thus, the capacitance value can be calculated:

$$\begin{aligned} C &= \frac{\Delta Q_C}{\Delta V_C} \\ &= \frac{N V_{out} I_{out}}{\alpha_V V_{in}^2 f_{Dickson}} \end{aligned} \tag{1.29}$$

Substituting Eq.1.29 into Eq.1.27, flying capacitor energy can be obtained:

$$E_{C,Dickson} = \frac{(N-1)(2N-1)}{12} \frac{P_{out}}{\alpha_V f_{Dickson}} \tag{1.30}$$

5) Volume metric:

Tthe volume ratio between hybrid Dickson converter and buck converter can be obtained as:

$$\begin{aligned} \frac{V_{tot,Dickson}}{V_{tot,buck}} &= \frac{(\frac{E_L}{\rho_{E,L}} + \frac{E_C}{\rho_{E,C}})_{Dickson}}{(\frac{E_L}{\rho_{E,L}})_{buck}} \\ &= \frac{E_{L,Dickson}}{E_{L,buck}} (1 + \frac{E_{C,DicksonL}}{E_{L,Dickson}} \frac{\rho_{E,L}}{\rho_{E,C}}) \end{aligned} \tag{1.31}$$

where,

$$\frac{E_{C,Dickson}}{E_{L,Dickson}} = \frac{(N-1)(2N-1)}{3(1-\frac{V_{out}N}{V_{in}})} \times \frac{\alpha_I}{\alpha_V} \tag{1.32}$$

Observed from Eq.1.31, similar to FCML converter, the passive component volume of the hybrid Dickson converter is also reduced. Besides, due to the parallel-connected branches, the flying capacitors' volume contributes less to the total volume than the FCML converter. Thus, for a larger conversion ratio, the hybrid Dickson converter is a better topology.

To realise complete soft charging in this topology, split-phase control method is proposed [21]. However, this topology also has a major drawback which is that the duty cycle here is reduced by 2, $D = \frac{NV_{out}}{2V_{in}}$.

Based on this, [9] proposed a DIHC. DIHC has fewer switches. Complete soft-charging is achieved by optimizing the size of the flying capacitors. Two naturally interleaved inductors here can support large output current and produce the original duty cycle, $D = \frac{NV_{out}}{V_{in}}$, realizing a larger conversion ratio. Other improvements to the hybrid Dickson SC converter are also shown in [6] and [11]. [6] presented a dual path structure, which can lower the inductor current for a given load current, thus reducing the inductor conduction loss. 92.7% peak efficiency can be obtained for a 48V-to-2V conversion. [11] introduced a symmetrical DIHC. An automatic charge balance can be achieved, reducing design effort and maximizing component utilization.

However, all these converters mentioned above need high voltage-stress transistors. A 12-level hybrid Dickson converter is introduced in [5]. In this architecture, the capacitors take over most of the input voltage, making the circuit to be an equivalent 4V-to-1V converter. This allows the on-chip 5-V transistor in the 48 V design. However, the 5-V transistor here only bears 4-V voltage, leading to a waste of switch voltage stress.

1.3.2 Prior arts for 3∼6-V intermediate bus architecture

Though hybrid SC converters have the potential to reduce the passive components volume compared to the basic buck converter while achieving a large conversion ratio, the power efficiency has just reached about 90%. To improve the efficiency, the two-stage architecture with low intermediate bus voltage comes into people's eyes since the second-stage buck converter performs better with lower input voltage. Thus, high total efficiency can be achieved once the first stage can achieve a decent efficiency.

Resonant SC converter is an attractive candidate for the first stage of the intermediate architecture, as it allows for natural zero current switching and soft charging operations, while maintaining the advantages of traditional SC converter [22]. Since two-phase resonant converter requires a large number of switches and capacitors to achieve a high conversion ratio, resonant converter working in multiple phases becomes increasingly attractive [25].

[36] proposed an 8-to-1 multi-phase resonant doubler SC converter, using the fewest switches and capacitors necessary to convert 48 V to 3 V. 98.0% peak efficiency with a maximum load of 40 A can be achieved. However, the reduction of switches results in a higher output impedance as there is only one conduction path in this converter, negatively impacting the load capability and efficiency. Thus, [2] proposed a multi-resonant cascaded series-parallel SC converter. To achieve the same conversion ratio, though three more switches and one more capacitor are used, the output impedance of the topology is reduced with three parallel current paths. 98.1% peak efficiency with a maximum load of 70 A can be achieved. However, high performance reso-

nant SC converters with larger conversion ratios (e.g. 16-to-1) have not been widely demonstrated.

1.4 THESIS OBJECTIVES

This thesis project's goal is to design high power efficiency, high power density and highly integrated DC-DC converters for 48 V data centers with either standard CMOS or GaN devices:

- Literature review of DC-DC converter topologies for 48 V data centers
- Based on [5], design a 10-level 48V/1V DIHC to fully utilize the voltage stress of 5-V on-chip MOSFET devices. And with two fewer switches this converter should have a higher power efficiency than [5].
- Design a multi-resonant 48V/3V DC-DC converter topology with GaN devices to achieve a high power efficiency.

1.5 THESIS ORGANIZATION

This thesis is divided into 5 chapters.

Chapter 2 presents a 90.6% efficient, 2093 W/in^3 power density direct 48V-to-1V DIHC with delay-line based V2D controller. The overall architecture, operation principle and circuit implementation of the proposed converter are described. The simulation results are presented, where also the comparisons between this work and the previous ones are discussed.

Chapter 3 proposed a 48V/3V multi-resonant DC-DC converter topology. The operation principle and topology analysis are shown, and the design procedures are presented. A simulation result based on the chosen component values is also shown.

Chapter 4 shows the future work of this project.

A final conclusion is presented in **Chapter 5**.

2 A DIRECT 48V-TO-1V DIHC WITH DELAY-LINE BASED V2D CONTROLLER

2.1 ARCHITECTURE

In this section, the architecture of the 10-level DIHC will be introduced. Firstly, the basic half-bridge buck converter will be discussed, and its power loss will be analyzed. From the analyzed power loss, a 10-level Dickson SC based DIHC will be presented. Its advantages and operation principle will be shown. Next, the compensation strategy for this converter will be illustrated. The overall architecture will be shown finally.

2.1.1 Basic Buck converter

The basic buck converter is shown in Fig.2.1a. Switching node voltage is shown in Fig.2.1b. Eq.2.1 shows the relationship between the output voltage and the input voltage, where D is the duty ratio. The power loss of the buck converter can be mainly divided into two categories: conduction loss P_{CON} and switching loss P_{SW} [19].

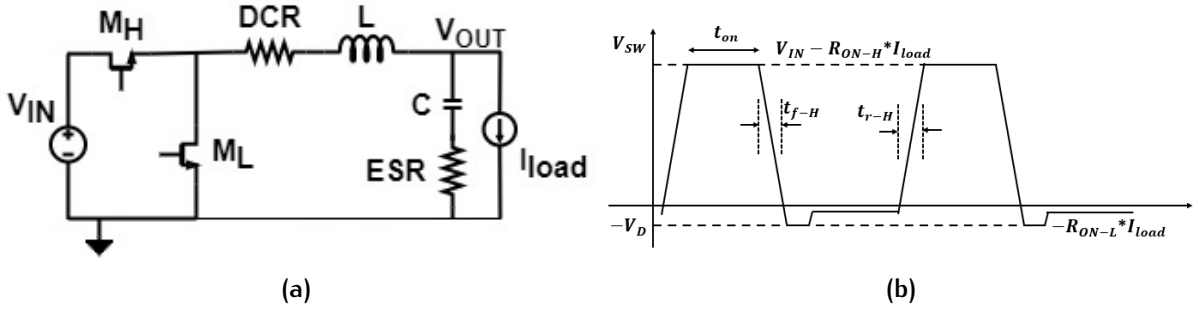

Figure 2.1: (a) Basic buck converter. (b) Switching node voltage of the basic buck

$$V_{out} = DV_{IN} \tag{2.1}$$

Conduction loss P_{CON} mainly includes the losses caused by the high-side transistors and low-side transistors $P_{cond,SW}$, inductor DCR P_{DCR}, and output capacitor equivalent series resistance (ESR) P_{ESR}. The total P_{CON} is given by:

$$P_{CON} = (I_{load}^2 + \frac{(\Delta I)^2}{12}) \times (R_{ON-H}D + (1-D)R_{ON-L} + DCR) + \frac{(\Delta I)^2}{12}) \times ESR \tag{2.2}$$

Here, R_{ON-H} and R_{ON-L} are the on resistance of the high-side switch and low-side switch, respectively. Due to the increase of the output current needed by the data cen-

ters, conduction loss on the inductor DCR and capacitor ESR has become an important factor on the efficiency.

Switching loss P_{SW} mainly includes the I-V overlap loss during turn-on and turn-off of the high-side and low-side transistors $P_{overlap}$, gate driving loss P_G, output capacitance loss P_{COSS}, and reverse recovery loss P_{RR}. P_{COSS} is mainly caused by the charging of parasitic capacitance of the high-side transistor and the low-side transistor due to the change of the switching node. P_{RR} is due to the charge extraction by the low-side parasitic diode when it is changed from the freewheeling state to the off-state. The expressions are given by:

$$P_{overlap} = [\frac{V_{IN}}{2} \times (t_{r-H} + t_{f-H}) + \frac{V_D}{2} \times (t_{r-L} + t_{f-L})] \times f_{SW} I_{load} \tag{2.3}$$

$$P_G = (Q_{G-H} + Q_{G-L}) \times V_{GS} \times f_{SW} \tag{2.4}$$

$$P_{COSS} = \frac{1}{2} \times (C_{oss-L} + C_{oss-H}) \times V_{IN}^2 \times f_{SW} \tag{2.5}$$

$$P_{RR} = Q_{RR} \times V_{IN} \times f_{SW} \tag{2.6}$$

For the 48V/1V converter, most of the conduction loss is due to the low-side transistors, as they are on for most of the time. Besides, when the load is heavy, the DCR loss of the inductor also accounts for a large proportion. Thus, to reduce this kind of loss, low on-resistance low-side transistor and high quality inductor with small DCR are needed. As the switching loss scales with the input voltage and the switching frequency, this part of loss can be reduced by decreasing the frequency or reducing the equivalent input voltage.

Switch quality determined loss P_{FOM} is defined, which includes $P_{cond,SW}$, P_G, P_{COSS} and P_{RR}. To provide a general definition, switching energy E_{SW} is used here to define the power loss associated with switching frequency [5]. Thus, P_{FOM} is given by:

$$P_{FOM} = I_{rms}^2 R_{ON} + f_{SW} E_{SW} \tag{2.7}$$

where, I_{rms} is the root mean square (RMS) current of switch.

$$FOM_E = R_{ON} E_{SW} \tag{2.8}$$

Also, an energy-based switch figure of merit (FoM), FOM_E, shown in Eq.2.8, is introduced to obtain a reasonable relationship between P_{FOM} and switch quality [5]. Substituting Eq.2.8 into Eq.2.7 gives:

$$P_{FOM,min} = 2\sqrt{FOM_E f_{SW}} I_{rms} \tag{2.9}$$

Neglecting charge redistribution loss and assuming $P_{FOM,min}$ is achieved for all switches, the minimum total loss of the basic buck converter is given as:

$$P_{tot,mim,buck} = 2\sqrt{FOM_{E,buck} f_{SW}} I_{o,rms}(\sqrt{D} + \sqrt{1-D}) + [\frac{V_{IN}}{2} \times (t_{r-H} + t_{f-H}) + \frac{V_D}{2} \times (t_{r-L} + t_{f-L})] \times f_{SW} I_{load} + P_{DRC} + P_{ESR} \tag{2.10}$$

2.1.2 The proposed 10-level DIHC

Operation principle

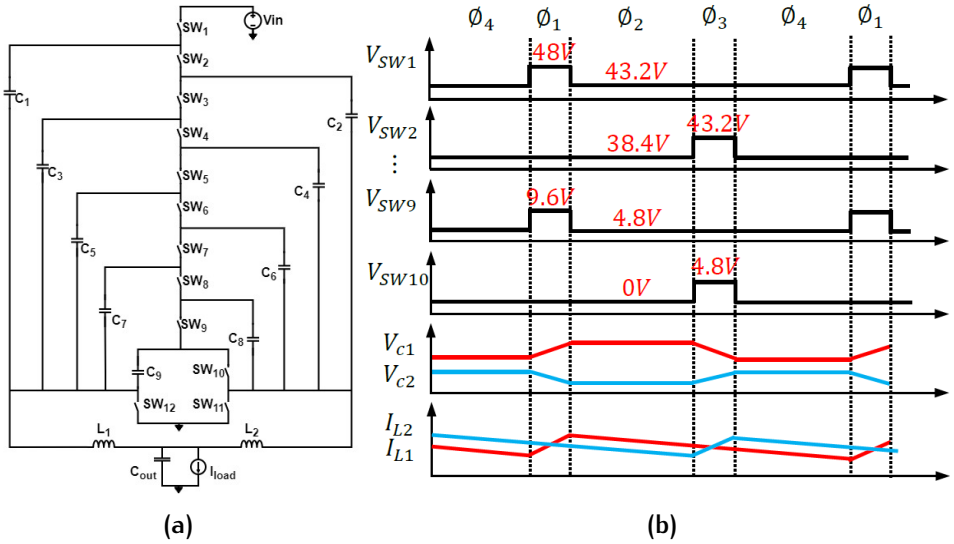

Figure 2.2: (a) The proposed 10-level DIHC. (b) operation waveform

The proposed 10-level DIHC converter is shown in Fig.2.2a. 10 high-side switches SW_1-SW_{10} are connected in series, and two low-side switches SW_{11}-SW_{12} are connected between two inductors L_1, L_2 and ground. The SW_1 is an off-chip e-mode GaN FET (EPC2035) with maximum 60-V continuous V_{DS} to block the full input voltage at the power-on period, and SW_2-SW_{12} are on-chip 5-V NMOS switches. The proposed converter includes 9 capacitors. Fig.2.3 demonstrates the four states of the proposed 10-level DIHC converter. Operation waveforms are shown in Fig.2.2b.

State $\phi 1$ (L_1 storing energy and L_2 releasing energy): The odd-number switches turn on and the odd-number capacitors are charged. The even-number switches and capacitors work just in the opposite way. The inductor L_1 stores the energy and L_2 releases the energy during this time. The power supply is connected to the whole circuit to provide power. The current flow is shown in Fig.2.3a. The necessary equations in state $\phi 1$ are:

$$\begin{cases} V_{in} - V_{C_1} = V_{C_2} - V_{C_3} = V_{C_4} - V_{C_5} = V_{C_6} - V_{C_7} = V_{C_8} - V_{C_9} = V_{X_1} \\ V_{X_1} = V_{L1} + V_{out} \\ 0 = V_{L2} + V_{out} \end{cases} \tag{2.11}$$

State $\phi 3$ (L_1 releasing energy and L_2 storing energy): The even-number switches turn on and the even-number capacitors are charged. The odd-number switches and capacitors work just in the opposite way. The inductor L_1 releases the energy and L_2 stores the energy during this time. The power supply is disconnected to the whole circuit and the output power is provided by the energy storage elements in the circuits. The current flow is shown in Fig.2.3b. The necessary equations in state $\phi 3$ are:

$$\begin{cases} V_{C_1} - V_{C_2} = V_{C_3} - V_{C_4} = V_{C_5} - V_{C_6} = V_{C_7} - V_{C_8} = V_{C_9} = V_{X_2} \\ V_{X_2} = V_{L2} + V_{out} \\ 0 = V_{L1} + V_{out} \end{cases} \tag{2.12}$$

State $\phi 2$ and $\phi 4$ (L_1 and L_2 releasing energy): The low-side switches turn on and all the other switches turn off during this time. The capacitors are idle. The inductors L_1 and L_2 are the power supply for the converter. The current flow is shown in Fig.2.3c where components in grey are in idle state. The necessary equations in state $\phi 2$ and $\phi 4$ are:

$$\begin{cases} 0 = V_{L1} + V_{out} \\ 0 = V_{L2} + V_{out} \end{cases} \tag{2.13}$$

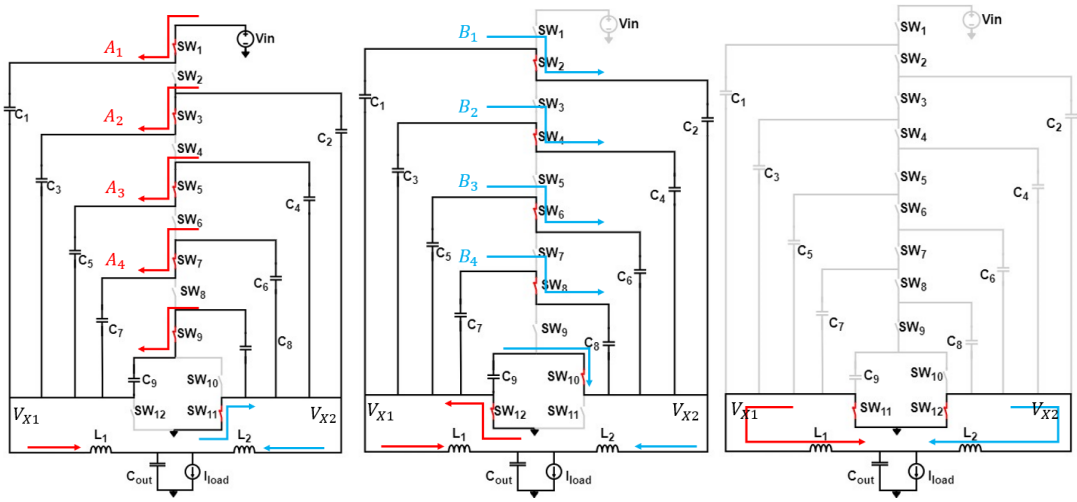

Figure 2.3: Operation states of the proposed structure. (a) State 1. (b) State 3. (c) State 2 and 4

For continuous conduction mode (CCM), according to the inductor voltage-second balance, average inductor voltage can be written as:

$$\langle V_{L_1} \rangle = \langle V_{L_2} \rangle \tag{2.14}$$

If the same duty cycle is applied to state 1 and state 3, expressions for the conversion ratio and flying capacitor voltages during the steady state are given as

$$D = \frac{V_o}{V_{in}/10} \tag{2.15}$$

$$V_{Ck} = \frac{10-k}{10} V_{in}, k = 1, 2, ..., 9 \tag{2.16}$$

where, V_{Ck}, V_{in}, and V_o are the average flying capacitor voltages, the input voltage and output voltage, respectively [8].

To maintain capacitor charge balance, charges shared among all the flying capacitors need to be the same, thus, $I_{Ck} = I_{C(k+1)}$. Inductors L_1 and L_2 see the same number of capacitor branches, which results in the same average current in the two inductors. This indicates that the current balance is automatically achieved [5]. The inductor current ripple in each inductor and the output voltage ripple are given as

$$\Delta i_L \approx \frac{V_o(1 - 10V_o/V_{IN})}{f_{SW}L} \tag{2.17}$$

$$\Delta V_o = \frac{V_o(1 - 10V_o/V_{IN})}{16LC_{OUT}f_{SW}} \tag{2.18}$$

Advantages of the proposed DIHC

The advantages of the proposed DIHC are brought by two parts, the 10-level Dickson SC converter and the interleaved inductors.

Thanks to this 10:1 Dickson step-down converter, most of the voltage stress will be taken over by off-chip capacitors, which reduces the voltage stress of each switch to 4.8 V and takes full advantage of the voltage pressure on the 5-V on-chip transistors.

The two interleaved inductors here enable the soft charging of the flying capacitors and provide the converter with natural current balance [29]. Besides, with these two inductors, the frequency of the output current doubles, which can reduce the output current ripple and the output voltage ripple. Also, as the energy stored in each inductor is reduced, the transient response of the load is improved. Ripple voltage reduction due to current cancellation helps reduce output voltage overshoot and undershoot [4].

Power loss analysis

1) Conduction loss P_{CON}:

Switch conduction loss $P_{CON,SW}$, inductor DCR loss P_{DCR} and capacitor ESR loss P_{ESR} are given in the following equations.

$$\begin{aligned} P_{CON,SW} &= \sum_{i=1}^{N/2} D(\frac{2}{N} I_{L_1,rms})^2 R_H + \sum_{i=1}^{N/2} D(\frac{2}{N} I_{L_2,rms})^2 R_H + 2 \times D I_{o,rms}^2 R_L \\ &+ (1-2D) I_{L_1,rms}^2 R_L + (1-2D) I_{L_2,rms}^2 R_L \\ &= \frac{D}{N} (2I_{L,rms})^2 R_H + 2D I_{o,rms}^2 R_L + 2(1-2D) I_{L,rms}^2 R_L \\ &= \frac{D}{10} I_{o,rms}^2 R_H + (\frac{1}{2} + D) I_{o,rms}^2 R_L \end{aligned} \tag{2.19}$$

$$P_{DCR} = 2I_{L,rms}^2 DCR = 2((\frac{I_o}{2})^2 + \frac{(\Delta i_L)^2}{12}) DCR \tag{2.20}$$

$$P_{ESR} = 9I_{C,rms}^2 ESR = 9 \times 2D(\frac{I_{L,rms}}{5})^2 ESR \tag{2.21}$$

2) Switch quality determined loss:

$$P_{FOM,LS,min} = 2\sqrt{FOM_E f_{SW}} I_{o,rms} \sqrt{2D+1} \tag{2.22}$$

$$P_{FOM,HS,min} = 2\sqrt{FOM_E f_{SW}} I_{o,rms} \sqrt{D} \tag{2.23}$$

3) Overlap loss:

$$\begin{aligned} P_{overlap} &= \frac{1}{2} \times 10 \times \frac{V_{IN}}{10} \times (t_{r-H} + t_{f-H}) \times f_{SW} \frac{I_{load}}{10} + \frac{1}{2} \times 2 \times V_D \times (t_{r-L} + t_{f-L}) \times f_{SW} \frac{I_{load}}{2} \\ &= \frac{1}{2} [\frac{V_{IN}}{10} \times (t_{r-H} + t_{f-H}) + V_D \times (t_{r-L} + t_{f-L})] \times f_{SW} I_o \end{aligned} \tag{2.24}$$

Thus, the minimum total loss of the proposed converter is given as:

$$\begin{aligned} P_{tot,mim,proposed} =& 2\sqrt{FOM_{E,proposed} f_{SW}} I_{o,rms} (\sqrt{D} + \sqrt{2D+1}) \\ &+ \frac{1}{2} [\frac{V_{IN}}{10} \times (t_{r-H} + t_{f-H}) + V_D \times (t_{r-L} + t_{f-L})] \times f_{SW} I_o + P_{DRC} + P_{ESR} \end{aligned} \tag{2.25}$$

As the switches in the proposed are 5-V low-voltage (LV) devices rather than high-voltage (HV) devices in the basic 48/1 V buck converter, the energy-based switch FoM is lower. Besides, the overlap loss is significantly reduced. Thus, a higher switching frequency than the basic buck can be used to reduce the size of passive components. Compared to the 12-level topology in [5], as the conduction loss and switching loss are the two major losses, the first term of Eq.2.25 will be reduced greatly with two less switches. Though the overlap loss will be increased a little due to the reduction in the level number. It can be offset by choosing a slightly lower switching frequency. Therefore, the proposed topology can see a better performance.

2.1.3 Compensation strategy

The equivalent circuit of the proposed 10-level DIHC is shown in Fig.2.4.

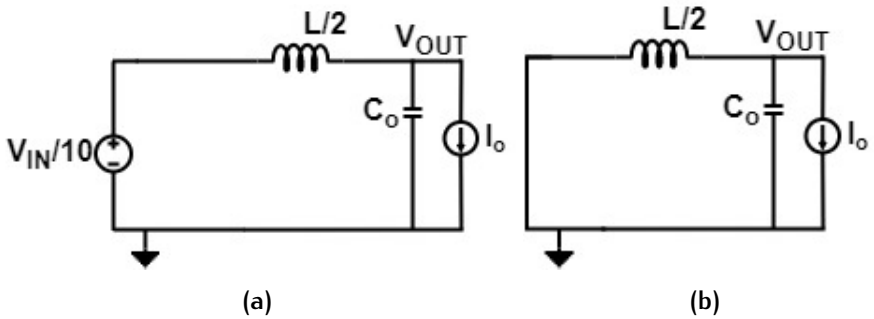

Figure 2.4: Equivalent model of the proposed 10-level DIHC. (a) State 1. (b) State 2.

Considering the ESR of the output capacitor C_o, according to the Kirchhoff laws, the state equations are given by:

State 1: $0 \leq t \leq DT$

$$\begin{cases} \dfrac{L}{2}\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = \dfrac{U_{in}}{10} - U_o, \\ i_L = C_o\dfrac{\mathrm{d}U_C}{\mathrm{d}t} + \dfrac{U_o}{R}, \\ U_o - U_C = R_{ESR}C\dfrac{\mathrm{d}U_C}{\mathrm{d}t}. \end{cases} \tag{2.26}$$

State 2: $DT \leq t \leq T$

$$\begin{cases} \dfrac{L}{2}\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = -U_o, \\ i_L = C_o\dfrac{\mathrm{d}U_C}{\mathrm{d}t} + \dfrac{U_o}{R}, \\ U_o - U_C = R_{ESR}C\dfrac{\mathrm{d}U_C}{\mathrm{d}t}. \end{cases} \tag{2.27}$$

Averaged equations are derived by averaging the resultant state equations with the duty cycle D:

$$\begin{cases} \dfrac{L}{2}\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = D(U_{in} - U_o) + (1-D)(-U_o) = D\dfrac{U_{in}}{10} - U_o, \\ i_L + R_{ESR}C\dfrac{\mathrm{d}i_L}{\mathrm{d}t} = \dfrac{1}{R}(U_o + C_oR\dfrac{\mathrm{d}U_o}{\mathrm{d}t}). \end{cases} \tag{2.28}$$

To linearize the equations, all states and input variables are perturbed with a small signal:

$$\begin{cases} \dfrac{L}{2}\dfrac{\mathrm{d}(i_L + \hat{i_L})}{\mathrm{d}t} = (D + \hat{D})\dfrac{(U_{in} - \hat{U_{in}})}{10} - (U_o + \hat{U_o}), \\ (i_L + \hat{i_L}) + R_{ESR}C\dfrac{\mathrm{d}(i_L + \hat{i_L})}{\mathrm{d}t} = \dfrac{1}{R}[(U_o + \hat{U_o}) + C_oR\dfrac{\mathrm{d}(U_o + \hat{U_o})}{\mathrm{d}t}]. \end{cases} \tag{2.29}$$

From the Eq.2.28 and Eq.2.29, we can get:

$$\begin{cases} \frac{L}{2}\frac{\mathrm{d}\hat{i_L}}{\mathrm{d}t} = D\frac{\hat{U_{in}}}{10} + \hat{D}\frac{U_{in}}{10} + \hat{D}\frac{\hat{U_{in}}}{10} - \hat{U_o} = D\frac{\hat{U_{in}}}{10} + \hat{D}\frac{U_{in}}{10} - \hat{U_o}, \\ \hat{i_L} + R_{ESR}C\frac{\mathrm{d}\hat{i_L}}{\mathrm{d}t} = \frac{1}{R}(\hat{U_o} + C_oR\frac{\mathrm{d}\hat{U_o}}{\mathrm{d}t}). \end{cases} \tag{2.30}$$

After Laplace transformation, the small signal transfer function can be achieved:

$$G(s) = \left.\frac{\hat{U_o}(s)}{\hat{D}(s)}\right|_{\hat{U_{in}}(s)=0} = \frac{U_{in}/10(1+sR_{ESR}C_o)}{s^2\frac{L}{2}C_o + s\frac{L}{2}/R + 1} \tag{2.31}$$

According to Eq.2.31, the simplified loop model is a second-order system, consisting of a pair of conjugate poles and an ESR zero. The bode diagram is depicted in Fig.2.5.

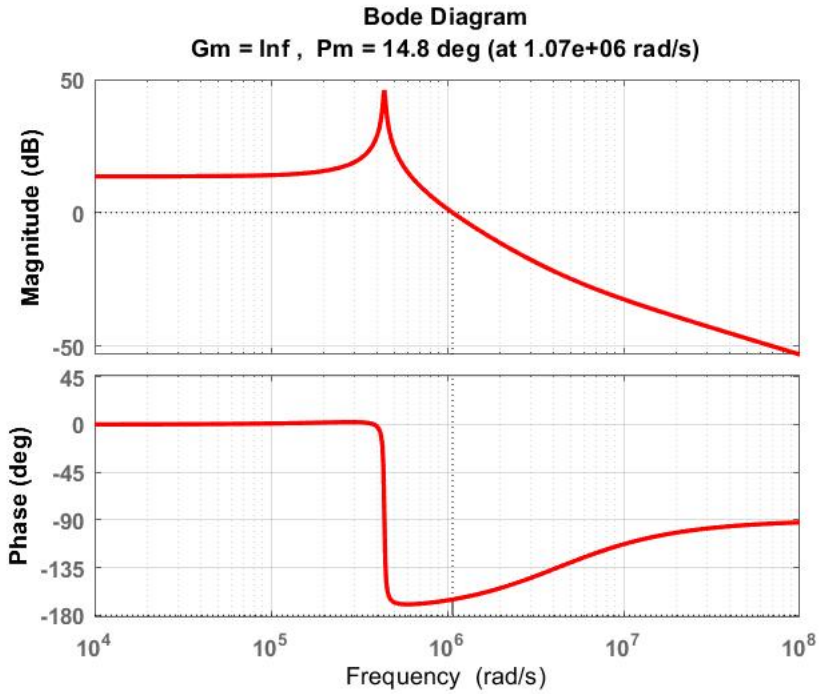

Figure 2.5: Bode diagram of the transfer function

At the gain crossover frequency, the phase is very close to $-180°$. As the Type-II compensator can only provide a maximum phase boost of $90°$, it can not eliminate the phase lag of the proposed buck converter in the CCM [16]. Thus, a Type-III compensator is required. Here, a Type-III A compensator is adopted, shown in Fig.2.6a. Type A has one more capacitor (Capacitor C_2) than the Type B, which can help to filter the high-frequency noise and $C_1 \gg C_2$.

The simplified bode diagram of the Type-III A compensator is shown in Fig.2.6b. The zeros and poles of the Type-III A compensator are listed as follows:

$$f_{p1} = \frac{1}{2\pi R_{o(EA)}C_1} \tag{2.32}$$

$$f_{p2} = \frac{1}{2\pi(R_{f1} \parallel R_{f2})C_{ff}} \tag{2.33}$$

$$f_{p3} = \frac{1}{2\pi R_1 C_2} \tag{2.34}$$

$$f_{z1} = \frac{1}{2\pi R_1 C_1} \tag{2.35}$$

$$f_{z2} = \frac{1}{2\pi R_{f2} C_{ff}} \tag{2.36}$$

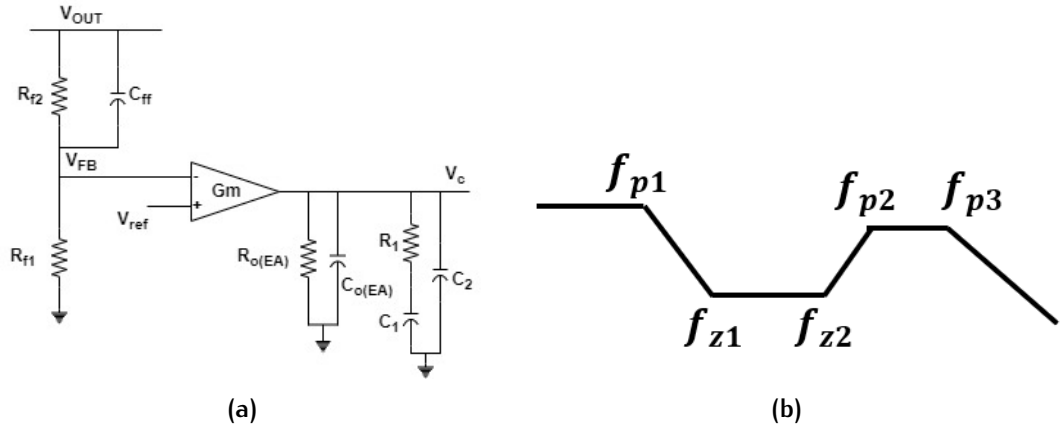

Figure 2.6: (a) Type-III A compensator for OTA. (b) Simplified bode diagram.

Then the transfer function is given by:

$$H(s) \approx \frac{R_{f1}}{R_{f1}+R_{f2}} \times G_m \times R_{o(EA)} \times \frac{1+sR_{f2}C_{ff}}{1+s(R_{f1} \parallel R_{f2})C_{ff}} \times \frac{1+sR_1C_1}{1+sR_{o(EA)}C_1+s^2R_{o(EA)}R_1C_1C_2} \tag{2.37}$$

The compensation principle is shown in Fig.2.7. The first zero of the Type-III A compensator is set below f_{LC}. The pole f_{p2} is set at the ESR zero. And the pole f_{p3} is set at about the switching frequency.

With $L = 110nH$, $C = 47\mu F \times 2$ and $2.5m\Omega$ ESR, the value of the capacitors and resistors in the compensation circuit can be calculated:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_o/2}} \approx 69.996\text{kHz} \tag{2.38}$$

$$C_{ff} = \frac{R_{ESR}C_o}{R_{f1} \parallel R_{f2}} \approx 1.57\text{pF} \tag{2.39}$$

$$f_{z2} = \frac{1}{2\pi R_{f2} C_{ff}} \approx 168.954\text{kHz} \tag{2.40}$$

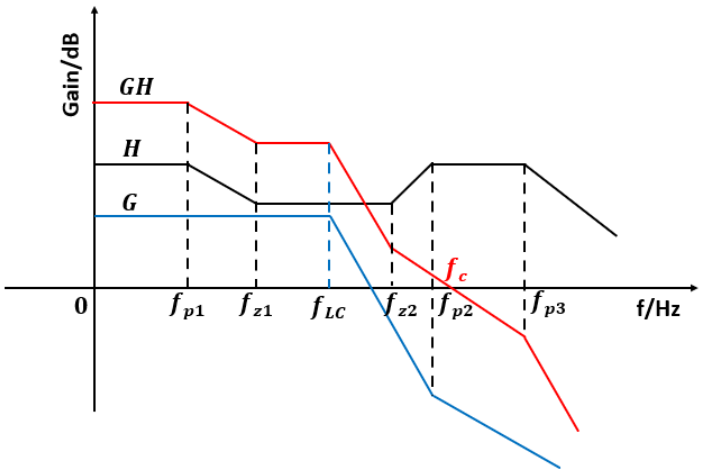

Figure 2.7: Bode diagram compensation principle

$$C_1 = \frac{1}{2\pi f_c} \times \frac{V_{IN}}{10} \times \frac{\Delta D}{V_c} \times \frac{f_{LC}^2}{f_{z2} \times f_{z1}} \times \frac{R_{f1}}{R_{f2} + R_{f1}} \times G_m \approx 10\text{pF} \tag{2.41}$$

$$R_1 = \frac{1}{2\pi C_1 f_{z1}} \approx 880\text{k}\Omega \tag{2.42}$$

$$C_2 = \frac{1}{2\pi \times f_{SW} \times R_1} \approx 180\text{fF} \tag{2.43}$$

The comparison of the bode diagram before and after compensation is shown in Fig.2.8. The red line is the bode diagram before compensation and the blue one is the bode diagram after compensation. From the figure, phase margin increases from 19.4° to 53°.

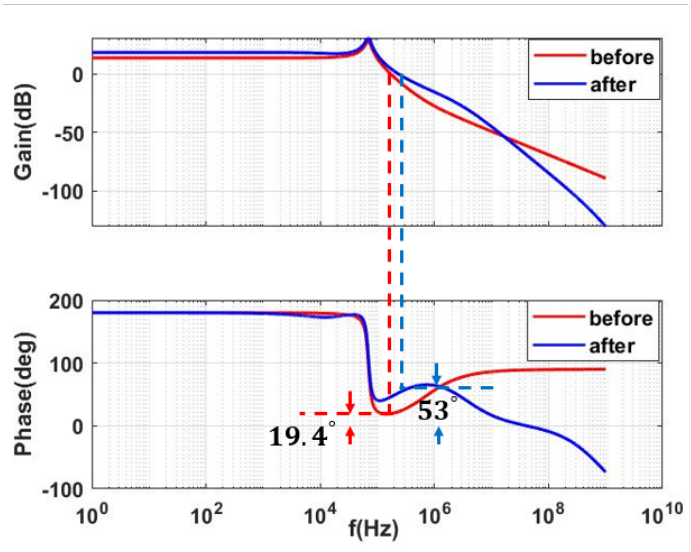

Figure 2.8: The bode diagram before and after compensation

2.1.4 Overall architecture

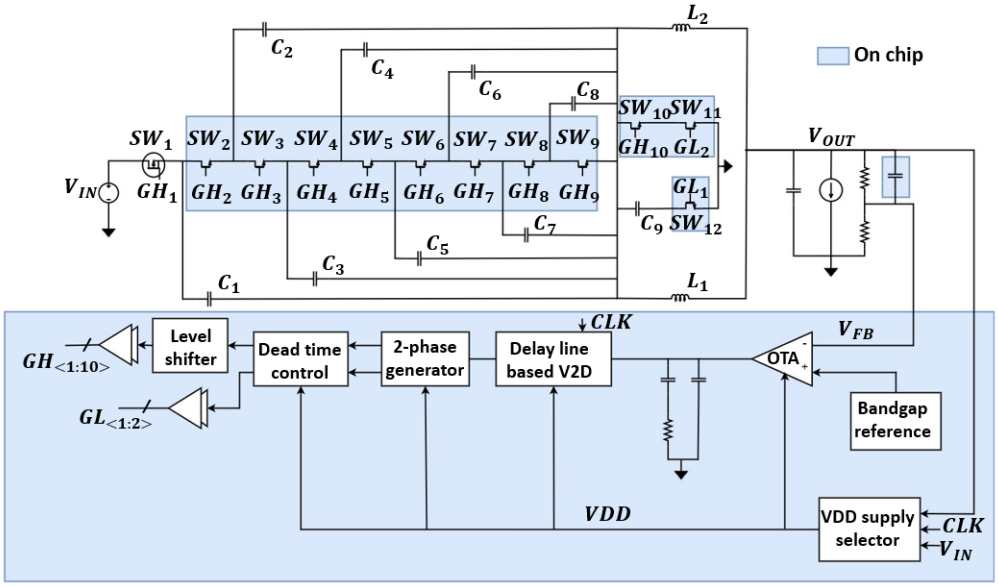

Figure 2.9: Overall architecture of the 10-level DIHC

Fig.2.9 shows the overall architecture of the 10-level Dickson SC based DIHC. The output voltage V_{OUT} is compared with a reference voltage to produce a control voltage to the delay line based V2D controller. The obtained pulse-width modulation (PWM) signal is then divided into two signals with the same frequency (half the input clock frequency) but 180° out of phase. After a dead time control block, two pairs of signals with dead time are generated to control the turn-on and turn-off of the switches SW_1 to SW_{12}. A VDD supply selector here is to provide the internal 5V voltage for the feedback loop.

2.2 CIRCUIT DESIGN

2.2.1 On-chip high-side switch

As the maximum V_{DS} of the high-side switches is 9.6 V, which is higher than 5-V on-chip MOSFET voltage rating, stacking of two 5-V transistors is used in the design, shown in Fig.2.10. Bulk and source of both M_1 and M_2 are connected together. The upper transistor M_2 is biased by 5 V, and the lower switch M_1 is driven by the gate driver. When the control signal Q is high, M_1 and M_2 turn on and are in triode region. When the control signal Q is low, M_1 turns off. The drain voltage of M_1 rises to $5V - V_{th}$ [28], below its voltage rating. The advantage of the stacked switches over high voltage switches can be evaluated by the output capacitance related FoM:

$$FOM = R_{ON}Q_{OSS} \tag{2.44}$$

$$FOM_{stack-10V} \approx N \times R_{ON}\frac{Q_{OSS}}{N} = FOM_{5V} < FOM_{10V} \tag{2.45}$$

where $FOM_{stack-10V}$ is the equivalent FoM of the stacking transistors, while FOM_{5V} and FOM_{10V} are the equivalent FoMs of the 5- and 10-V transistors, respectively [5].

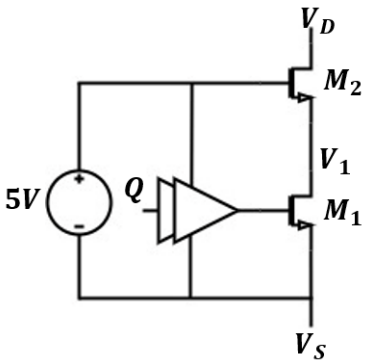

Figure 2.10: Stacking of two 5-V transistors

2.2.2 Bootstrap circuit

The role of the bootstrap circuit is to generate a voltage 5 V higher than the voltage of node SW_i to fully turn on the high-side switches. Directly producing the bootstrap voltage from 48-V input could result in considerable loss, particularly for the lower level switches [5]. Thus, two types of bootstrap circuits are used for the 10 high-side switches.

Bootstrap circuit for SW_1 and SW_2

Since the operation voltage levels of SW_1 and SW_2 are near the 48-V input, the bootstrap circuit of these two switches are directly powered by V_{IN}, shown in Fig.2.11. It mainly consists of a voltage monitor and an active diode. The volatge monitor is a bandgap reference comparator, aiming to detect the bootstrap voltage V_{BST} to make sure V_{BST} will not be larger than the gate breakdown voltage at any time.

The bandgap reference comparator [35] includes subthreshold transistors M_1 and M_2, as well as resistors R_4 and R_5. M_3 - M_8 form the current mirror pairs. The active diode consists of M_P and M_{dp_nmos}. M_{dp_nmos} is a depletion-type NMOS. Resistors R_1 - R_3 are to sample V_{BST}. M_7 is used to control the dividing ratio to achieve hysteretic threshold, and its on-resistance needs to be much smaller than R_3. The width of M_1 is 8 times bigger than that of M_2. The current I_6 is N times larger than I_2 and I_8 is N times larger than I_1. Thus, the voltage level of A is determined by the comparison result of I_1 and I_2. Assuming that V_{BST} rises from a low value to a high one at first, the working procedure can be divided into three stages.

Stage 1: When V_B is low, R_4 has little impact. Thus, due to the width of M_1 is larger than that of M_2, I_1 is larger than I_2. Hence, I_8 is larger than I_6. The voltage of node

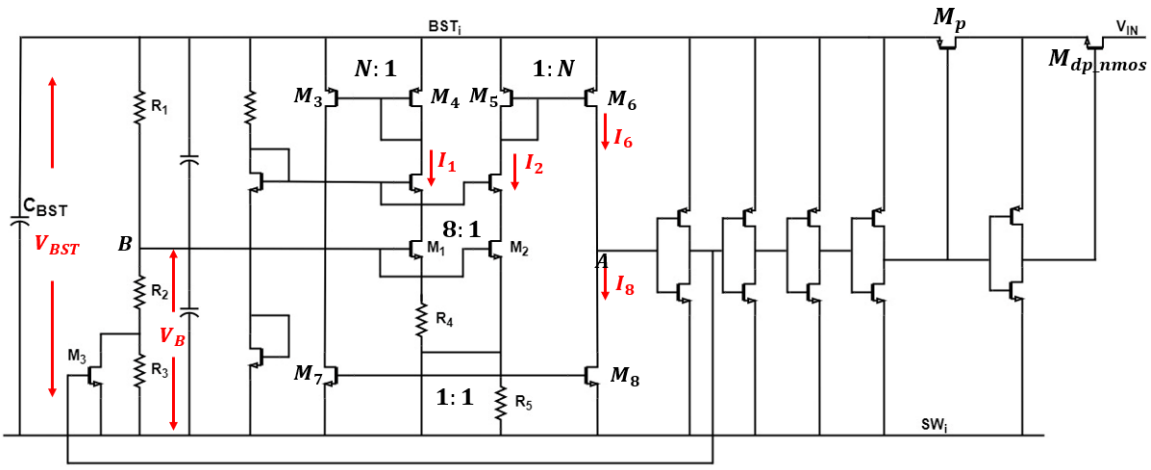

Figure 2.11: Schematic of bootstrap circuit for SW_1 and SW_2

A is pulled down. M_7 turns on, and R_3 is shorted. The active diode is on, and the bootstrap capacitor is charged.

Stage 2: As V_B becomes larger, the voltage drop on R_4 increases. I_2 grows at a quicker rate than I_1. At the time when I_2 is equal to I_1, the corresponding voltage of V_B is the bandgap voltage V_{BG}, given by Eq.2.46. The bootstrap voltage now is shown in Eq.2.47.

$$V_{BG} = V_{GS_2} + 2\frac{R_5}{R_4} n V_T ln8 \tag{2.46}$$

where n is a constant relating to MOSFET process [24].

$$V_{BST} = (1 + \frac{R_1}{R_2}) V_{BG} \tag{2.47}$$

Stage 3: When V_{BST} keeps increasing, I_2 becomes larger than I_1, and thus I_6 is larger than I_8. The voltage of node A is pulled up. M_7 turns off. R_3 is added to the resistive divider. The active diode is off, and the bootstrap capacitor is discharged. At this time, the bootstrap voltage is given by Eq.2.48.

$$V_{BST} = (1 + \frac{R_1}{R_2 + R_3}) V_{BG} \tag{2.48}$$

The operation results of bootstrap circuit are shown in Fig.2.12.

Bootstrap circuit for SW_3 to SW_{10}

The Bootstrap circuit depicted in Fig.2.13 is used for SW_3 - SW_{10}, which operate at lower voltage levels. The i-th high-side bootstrap is powered by the switching node SW_{i-2}, rather than V_{IN}. The voltage difference between SW_{i-2} and SW_i is a constant 9.6 V. From the 9.6-V floating sources, the 5-V floating supply is provided for each switch. The operation results are shown in Fig.2.14.

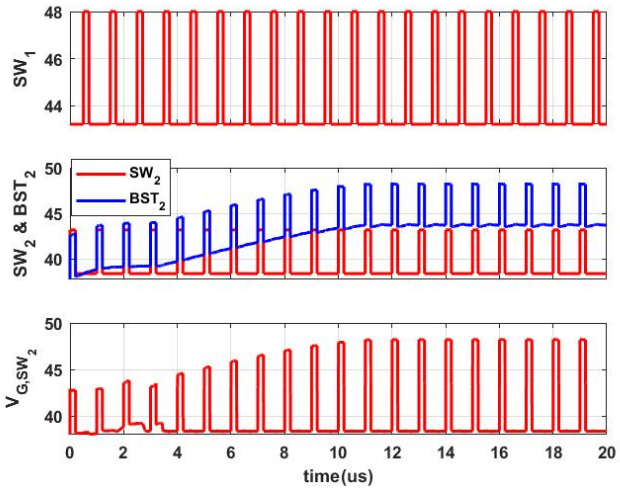

Figure 2.12: Operation results of bootstrap circuit for SW_2

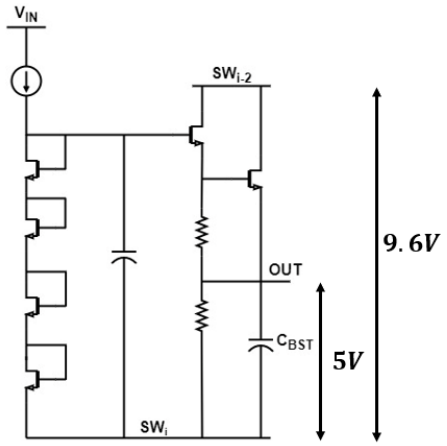

Figure 2.13: Schematic of bootstrap circuit for SW_3 and SW_{10}

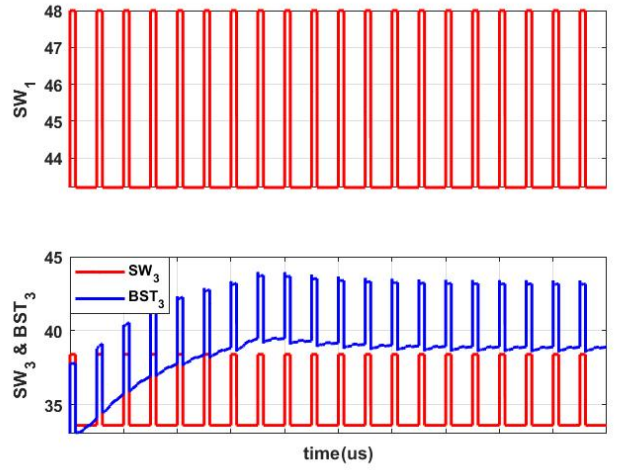

Figure 2.14: Operation results of bootstrap circuit for SW_3

2.2.3 Level shifter

Conventional high-voltage drivers typically have a propagation delay of several tens of nanoseconds in the level shifter, resulting in a poor performance as the switching frequency approaches high [30]. To address this issue, a DLS with both pulse-triggered (PT) and level-triggered (LT) level shifter is adopted, shown in Fig.2.15. The PT level shifter establishes the signal at the rising and falling edges of the input control signal, with short propagation delay and relatively large instantaneous power consumption. The LT level shifter is to maintain the signal, after the brief pulse has vanished. The propagation delay is relatively long, but the average power consumption is low. The two collaborate to ensure fast and accurate delivery of the low-side control signal to the high-side. Timing waveforms of this DLS are shown in Fig.2.16.

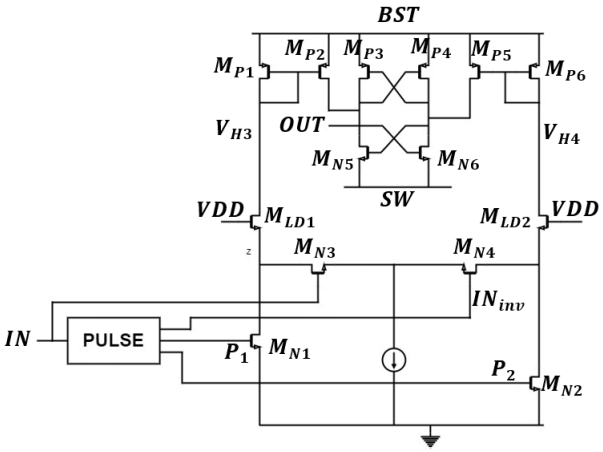

Figure 2.15: Schematic of a DLS

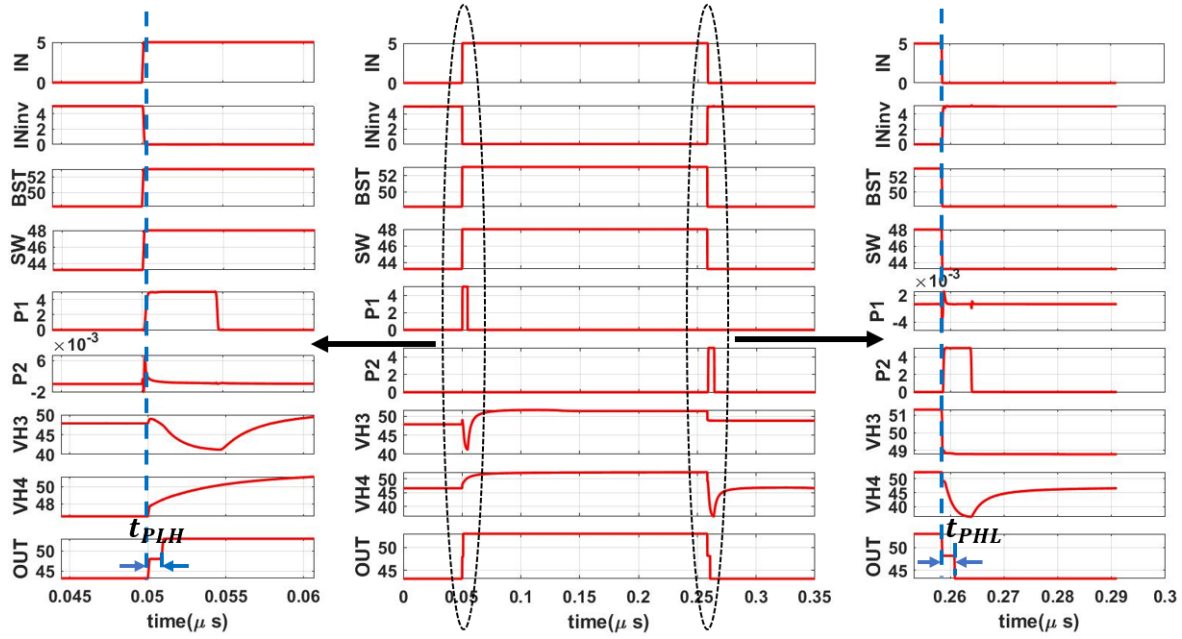

Figure 2.16: Timing waeforms of DLS

The input control signal IN generates narrow pulses on its rising and falling edges through the pulse generator, namely P_1 and P_2 in the figure, to control on and off of M_{N1} and M_{N2} respectively. M_{N3} and M_{N4} are controlled by the IN and the voltage

signal inverse to the input control signal IN_{inv}, respectively. M_{LD1} and M_{LD2} are HV MOS to isolate the high-side driving path and low-side driving path. Their gates are biased by VDD to protect the LV MOS. Fig.2.17 shows $\frac{dV_{SW}}{dt}$ issues when the voltage of SW_i changes rapidly [38]. When the voltage of SW_i rises rapidly, the voltage of BST_i will follow V_{SW_i}. However, due to C_D, the voltage of node A and node B are unable to respond instantly. Thus, the parasitic capacitor C_D will be charged. Both current mirrors copy large currents. The differential-mode current is close to 0. The output signal has a brief transient from 1 to 0, disturbing the normal turn-on of the high-side switches. When the voltage of SW_i drops rapidly, the voltage of BST_i will also drops quickly. Thus, the parasitic capacitor C_D will be discharged. Currents on both sides reduce. The differential-mode current is also close to 0. The output signal has a brief transient from 0 to 1, interfering high-side switches' normal turn-off. This problem can be solved by using the transient current generated by the pulse generator. The transient current needs to be larger than the common-mode current. Its expression is given by:

$$I > C_D \frac{dV_{SW}}{dt} \tag{2.49}$$

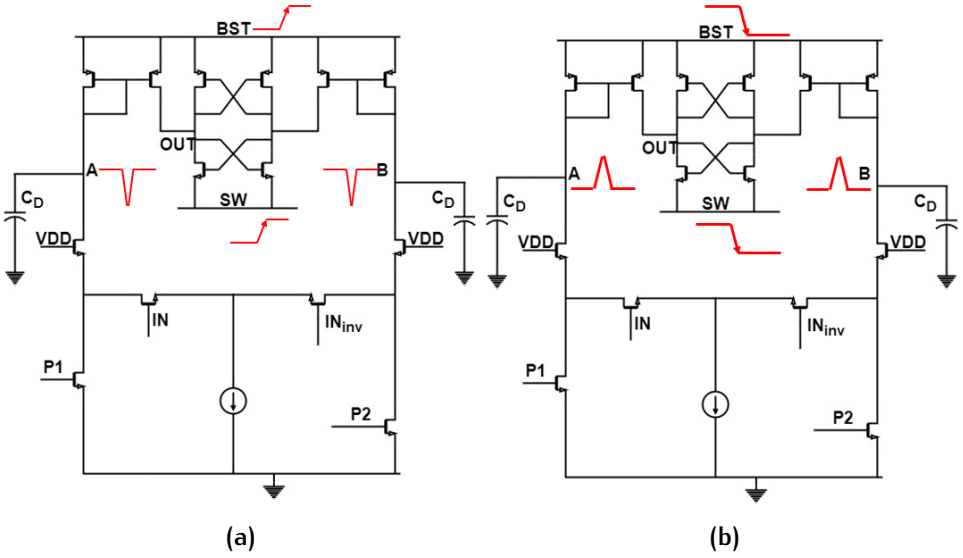

Figure 2.17: (a) Positive slewing. (b) Negative slewing.

During the narrow pulse at the rising edge of IN, the gate voltages of M_{N1} and M_{N3} are high. The current flowing through M_{LD1} is given by:

$$I_{M_{LD1}} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_{M_{LD1}}(V_{GS,M_{LD1}} - V_{th,M_{LD1}})^2 \tag{2.50}$$

The drain voltage of diode connected M_{P1} (V_{H3}) is pulled down, followed by the drain voltage of M_{P2} to pull up. During the narrow pulse at the falling edge of IN, the gate voltages of M_{N2} and M_{N4} are high. The drain voltage of diode connected M_{P6} (V_{H4}) is pulled down, followed by the drain voltage of M_{P5} to pull up. M_{N5} turns on, pulling down the voltage of output node. t_{PLH} and t_{PHL} in Fig.2.16 are the total propagation delay for the high-side driving path when the input control signal changes from low to high and high to low, respectively. The values are $900ps$ and $2.3ns$.

2.2.4 Feedback loop controller

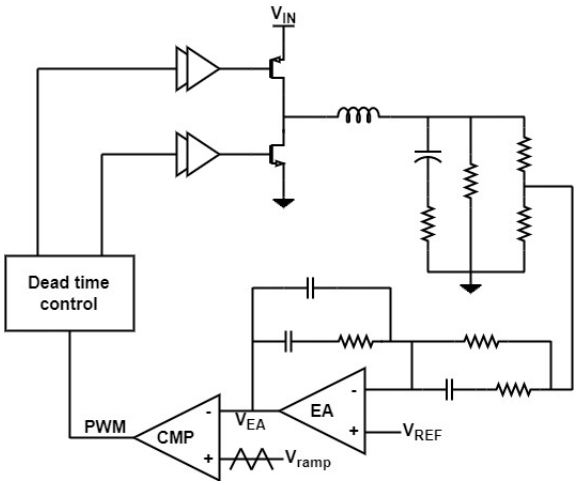

Figure 2.18: Buck converter with ramp-comparator based V2D controller

Voltage control mode (VCM) is widely used because of its easy design and good immunity to disturbances at the reference input [14]. Fig.2.18 shows the structure of a buck converter with ramp-comparator based V2D controller and Type-III compensation. The output of the error amplifier V_{EA} is compared to a fixed frequency ramp signal V_{ramp} through a comparator to generate the PWM signal. If $V_{ramp} > V_{EA}$, $PWM = 1$. If $V_{ramp} < V_{EA}$, $PWM = 0$. However, in this controller, the delay time of the comparator limits the maximum duty cycle of the converter [7]. Thus, a high-speed comparator is required.

A delay line based PWM controller is adopted, which can simplify the complexity of circuit design, fit the high switching frequency used and ease the delay-related limitations. The block diagram of the main part delay line based V2D controller is shown in Fig.2.19. It consists of two parts, a fixed small duty cycle generator and a V2D controller. The duty cycle of the fixed small duty cycle generator is set to be 20%, corresponding to minimum $D = 10\%$ for P_1 and P_2 in Fig.2.9. In each part, there are two V2D cell, calibrating the bias current of the delay cell, which determines the maximum duty cycle.

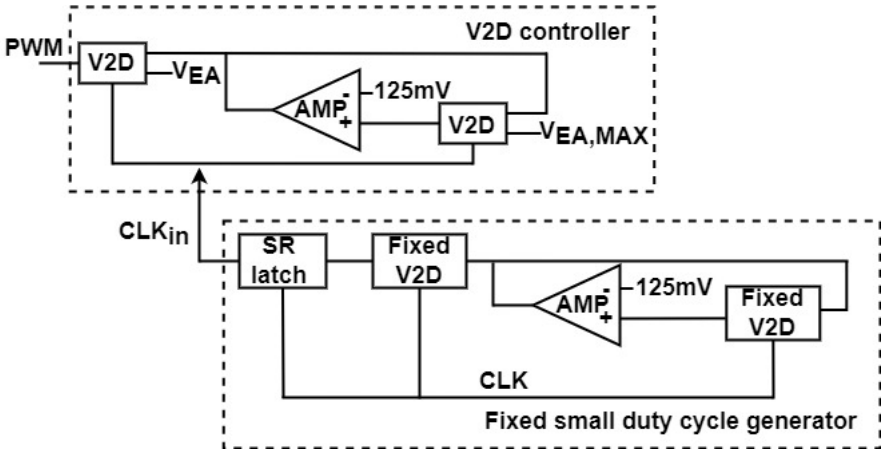

Figure 2.19: Delay line based V2D controller

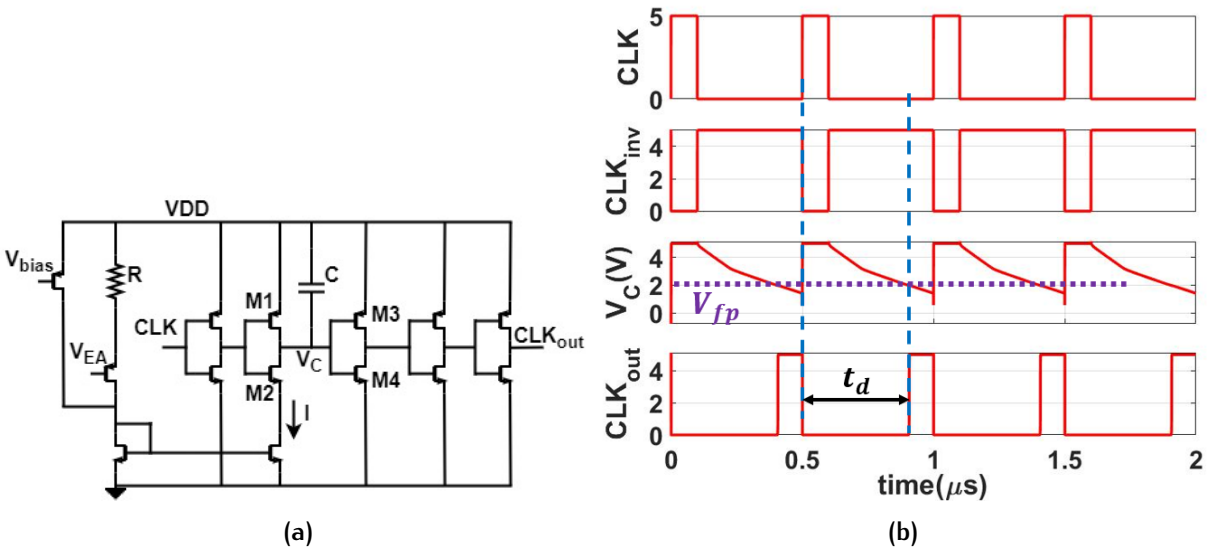

Figure 2.20: (a)Schematic and (b) timing diagram of the V2D cell

Fig. 2.20a shows the V2D cell in the V2D controller. It generates a duty cycle signal by changing the delay of the falling edge of the clock based on the control voltage V_{EA} from the previous error amplifier stage. It first converters V_{EA} into current and then converts the current to output PWM signal. The timing diagram of the V2D circuit is shown in Fig. 2.20b. When CLK is high, V_C equals to VDD and CLK_{out} is low. When CLK is low, M2 turns on. V_C begins to decrease. When its value is lower than the flip voltage of the following inverter (V_{fp}), CLK_{out} changes to high. The changed time t_d can be expressed as:

$$t_d = \frac{C(VDD - V_{fp})}{I} \tag{2.51}$$

where I is controlled by both the bias voltage V_{bias} and control voltage of the error amplifier V_{EA} in the previous stage.

Since the V_{bias} determines the bias current and thus the maximum duty ratio, it needs to be constant. A small change of the bias voltage will cause problems in the feedback circuit. The bias calibration is realised by using a second V2D cell [15]. Fig.2.21a shows the characteristics of the V2D controller. The error voltage range is corresponded to the output range $V_{out} = 1V \pm 5\%$. The output PWM waveforms matching the data points in Fig.2.21a is shown in Fig.2.21b.

The schematic of two-phase generator is shown in Fig.2.22a. The function of it is to generate two control signals with the same duty cycle and a phase difference of 180°. It consists of an inverter, a D flip-flop and two AND gate. Q_2 lags Q_1 by half a cycle. The timing diagram is shown in Fig.2.22b.

In order to avoid the loss produced by the simultaneous conduction of the high-side and low-side switches, a dead control circuit is designed. It includes an inverter, two NOR gates, two buffers and two inverter chains. Fig.2.23a shows its schematic. The width of the inverter chains is set to the minimum value, and the length is selected according to the required dead time. When V_{PWM} is high, D and thus G_L go low first. After a delay, C goes low. A and C pass the NOR gate and E is set to high, and thus

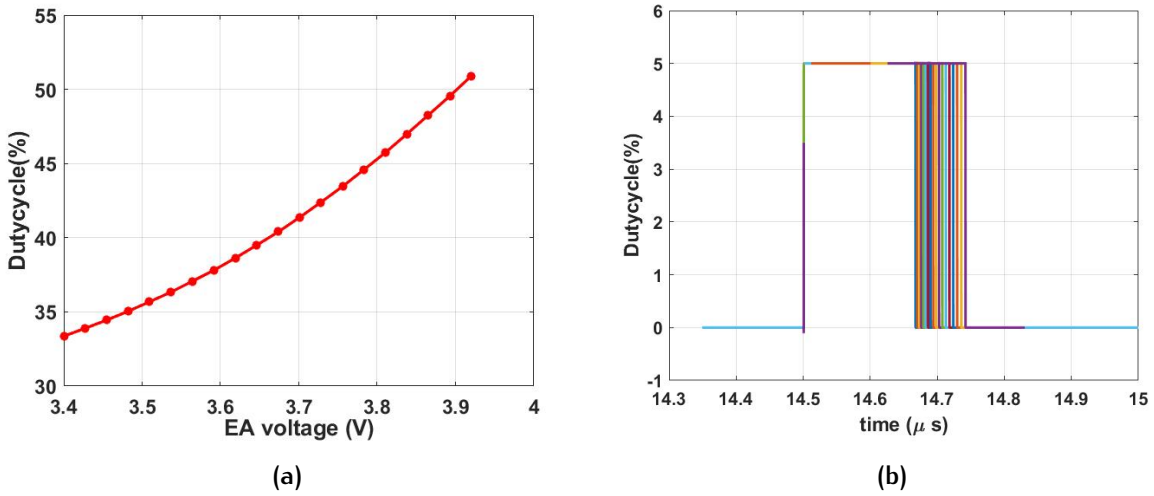

Figure 2.21: (a) Characteristics of the V2D controller. and (b) output PWM waveforms.

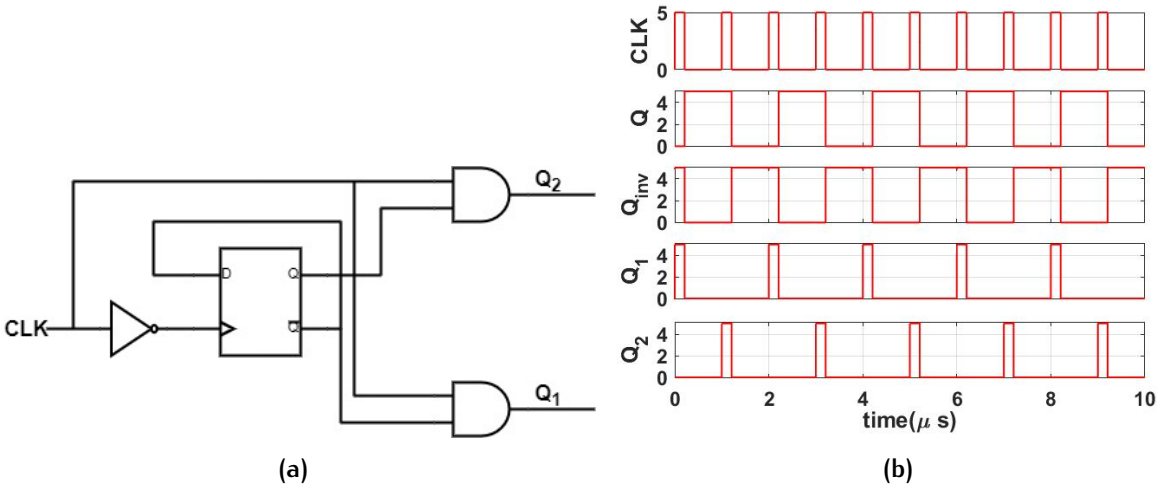

Figure 2.22: (a) Schematic and (b) Timing diagram of the two-phase generator.

G_H. When V_{PWM} is low, E goes low first, and thus G_H. After a delay, B goes low. B and V_{PWM} pass a NOR gate and then D goes high, and thus G_L. The timimg diagram of the dead time control circuit is shown in Fig.2.23b.

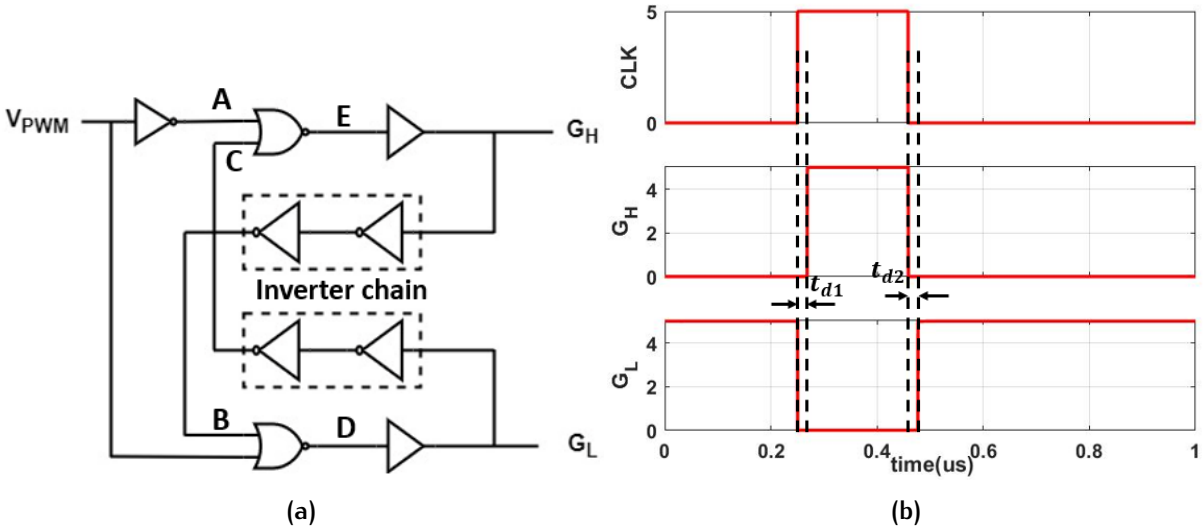

Figure 2.23: (a) Schematic and (b) Timing diagram of the dead time control circuit.

2.2.5 VDD supply selector

As the power supply in the feedback controller is about 5V, different from the input voltage of the system. Thus, an internal power supply generator is required to produce a low voltage. As there is a big difference between the needed voltage and the input voltage, the low-dropout linear regulator (LDO) is not applicable due to its low frequency. However, it has fast transient response, which can produce the needed voltage quickly. Thus, a VDD supply selector is proposed, shown in Fig.2.24. It consists of high-voltage pre-regulator, LDO, bandgap reference, comparator, 1:5 SC DC-DC converter and switches.

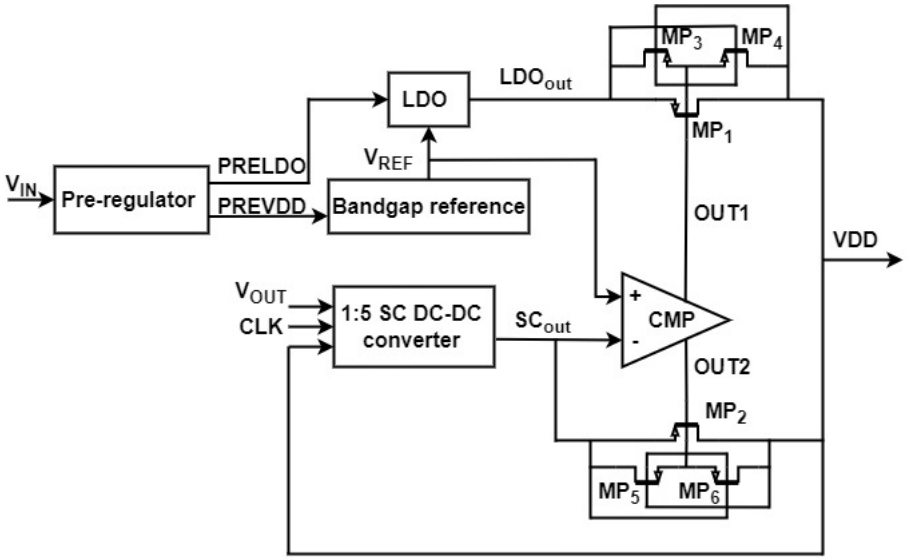

Figure 2.24: Block diagram of the proposed VDD supply selecting circuit

For the two switches MP_1 and MP_2, two additional PMOS are added to each switch to connect the bulk of the two switches to the higher voltage level to eliminate the effect of parasitic bipolar[12]. When the source voltage of MP_2 is lower than the drain voltage, MP_6 is on and MP_5 is off. Thus, the bulk voltage of MP_2 is connected to the drain side.

Since the input voltage of the system is high, when it is directly supply to the bandgap reference and LDO circuit, if LV transistors are used, they will break down due to insufficient voltage withstand capability, and if HV transistors are used, the chip area will be greatly increased [17]. Thus, a pre-regulator is used at first.

The overall operation of this proposed supply selecting circuit is shown in Fig.2.25. At the beginning, the VDD supply is provided by the LDO. As long as the output voltage of SC converter builds up, the output of the comparator changes and SC converter will replace the less efficient LDO to provide the VDD supply. Fig.2.26 shows that there is an increase in feedback controller duty cycle when the VDD supply decreases. This can help increase the load capability of the converter, as when it carries heavy loads, the output voltage may go below 1 V and thus the VDD supply also decreases, which can further increase the duty cycle to help the voltage go back to 1 V.

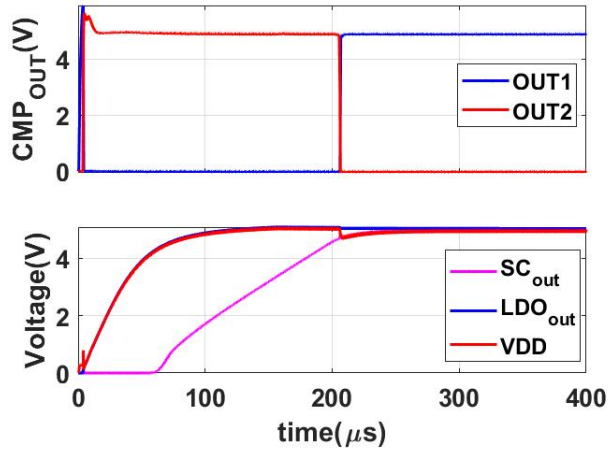

Figure 2.25: Overall operation of the proposed VDD supply selecting circuit

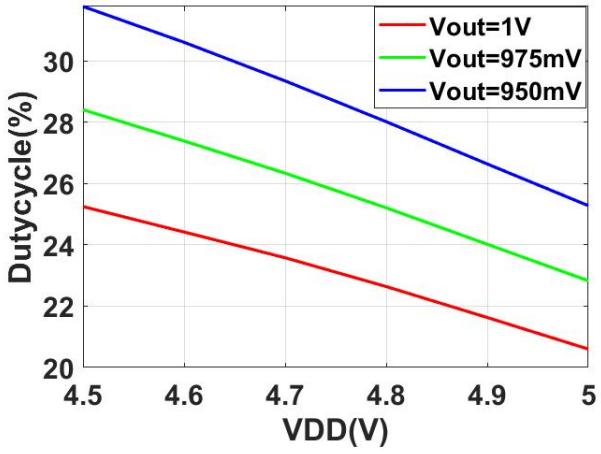

Figure 2.26: Duty cycle with VDD

2.3 SIMULATION RESULTS

The proposed 10-level DIHC converter was designed in a 0.18-μm BCD process and the results are based on post-layout simulations of the whole chip. Fig.2.27 shows the layout of the proposed converter. The active size is 3.8mm $\times$ 5.9mm, with an area of around 22 mm^2. The converter was simulated under the following conditions: input voltage $V_{in} = 48$ V, output voltage is regulated at $V_{out} = 1$ V, and the switching frequency $f_{SW} = 1$ MHz. The GaN Spectre model provided by EPC is used for the SW_1 switch.

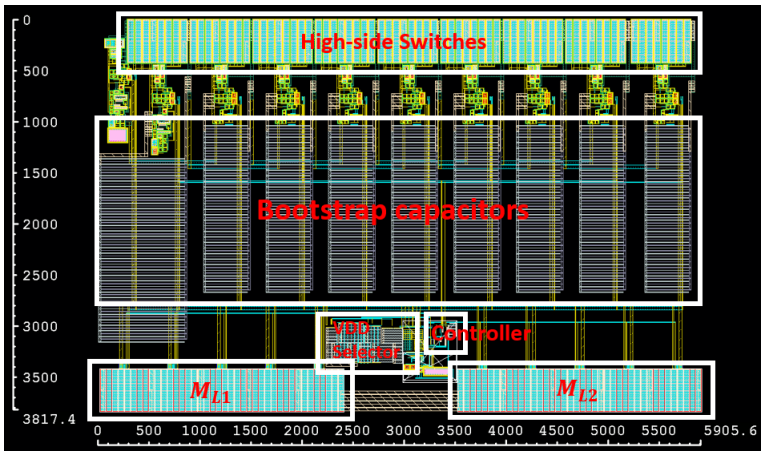

Figure 2.27: Layout of the proposed converter with an area of 3.8mm $\times$ 5.9mm

Fig.2.28 shows the simulated waveforms of the switching nodes. During the power-on period, only SW_1 (GaN) takes the up to 48-V voltage stress and all NMOS switches take up to 4.8-V voltage stress to secure a safe power-on stage for these 5-V devices. During the steady state, as shown in Fig.2.28b, the voltage swing of all switching nodes is 4.8 V, which is $V_{in}/10$, i.e., the voltage of SW1 is between 48 V and 43.2 V, the voltage of SW2 is between 43.2 V and 38.4 V, and so on.

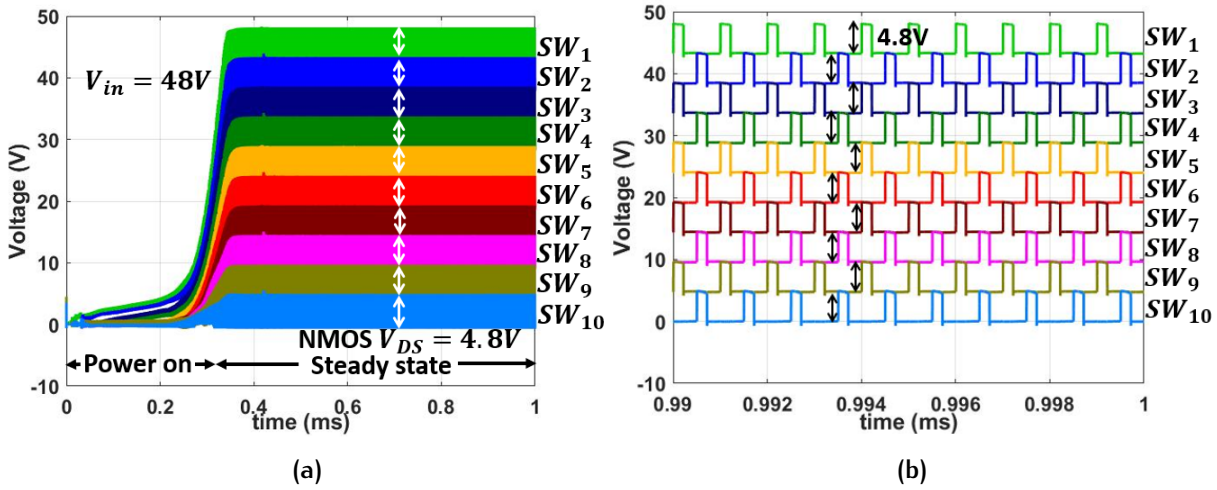

Figure 2.28: Simulated waveform of switching nodes of NMOS switches during (a) power ON and (b) steady-stage operations.

The simulated efficiency values in a range of load current are shown in Fig.2.29. The converter achieves a peak efficiency of 90.6% at 5.2-A load. For a large range of load

current from 2 A to maximum 18 A, the efficiency is above 80%. The inductor current and output voltage at the optimum load (I_{load} = 5.2 A) are illustrated in Fig.2.30. The output voltage is maintained at 1 V with a small ripple of 12.4 mV. The inductor current waveform shows that there is uniform current distribution between the two inductors.

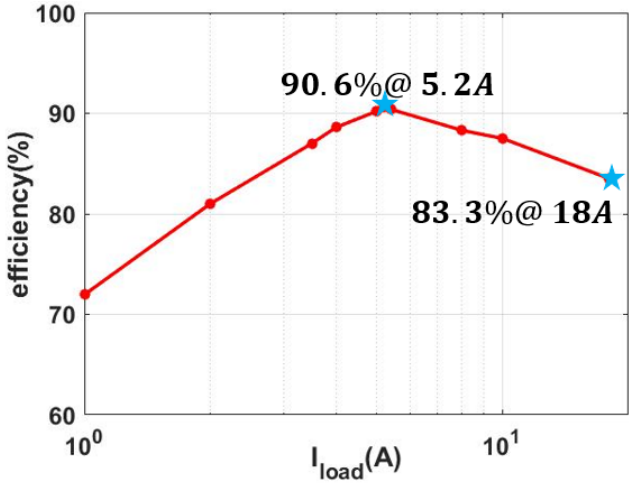

Figure 2.29: Simulated power efficiency

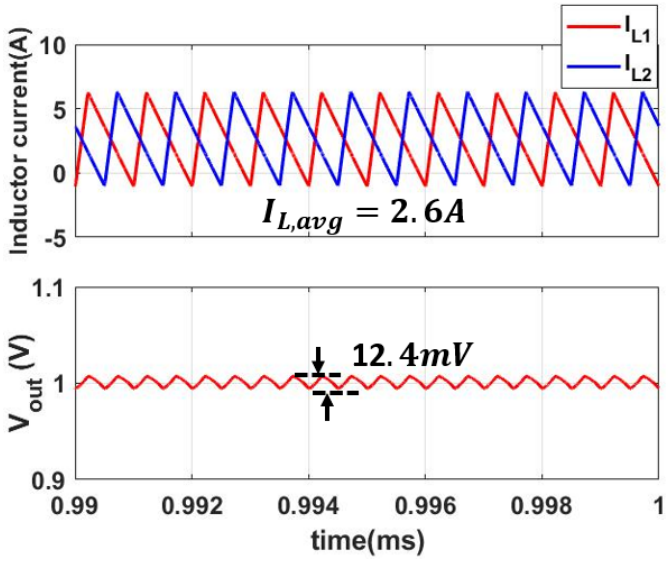

Figure 2.30: Inductor current and output voltage at the optimum load

Fig.2.31 shows the simulated load transient responses of the proposed converter. When load current steps up from 0 A to the optimal load current 5.2 A, the undershoot voltage is 46.4 mV and the recovery time is about 4 μs. When load current steps down, the recovery time is 3.7 μs, and the overshoot voltage is 50 mV. The proposed converter performs a quite fast transient response.

Fig. 2.32 gives an estimated loss breakdown based on post-layout simulation results. The proposed design adopts 1 μF capacitor with 5-mΩ ESR for all flying capacitors, and 110 nH inductor with 3-mΩ DCR for the two inductors. The conduction and overlap loss, the gate and switching loss, the DCR and ESR loss, and the layout loss account for 42.8%, 23.9%, 23.1% and 8.6%, respectively.

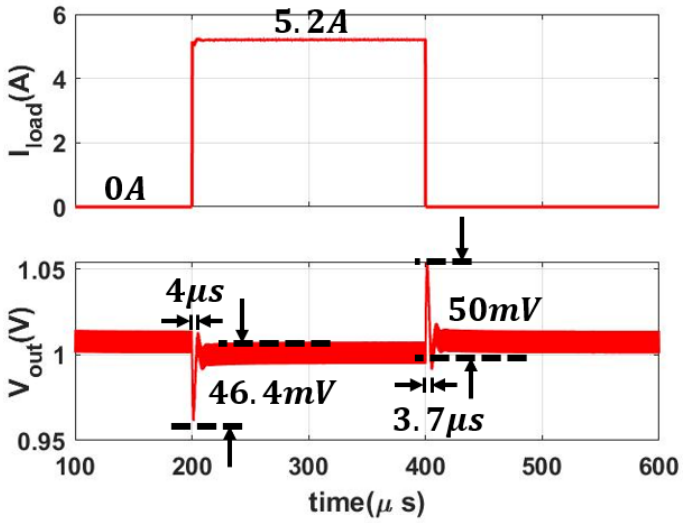

Figure 2.31: Simulated load transient responses between o and optimum load with $C_{out} = 47\mu\text{F}\times 2$

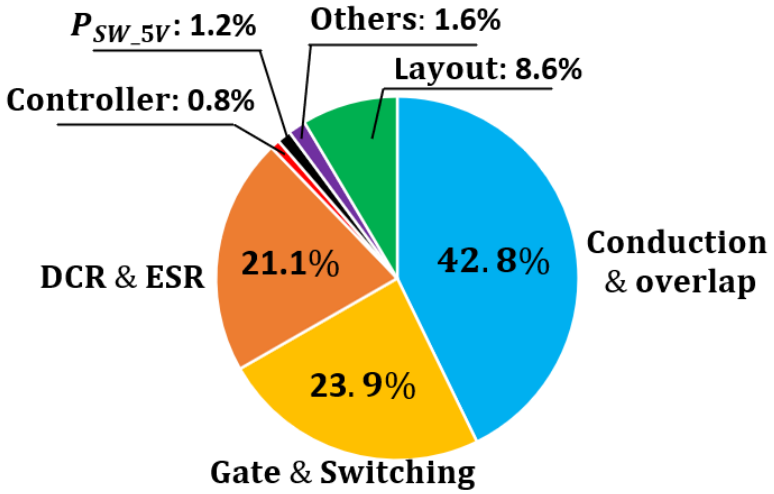

Figure 2.32: Estimated loss breakdown at the optimum load

The comparison between this proposed 10-level DIHC and state-of-the-art designs is shown in Table 2.1. Compared with the 12-level converter in [5], this converter uses two less on-chip switches and two less flying capacitors to achieve 48-V to 1-V conversion. It is able to carry maximum 18-A load, and achieves higher peak efficiency at 90.6% and more than two times higher power density. Compared with two other works, the proposed design only employs one single off-chip GaN switch, which significantly reduces the system FoM factor and improves the power density.

Table 2.1: Comparison with the previous work

Structure	**Dual-phase dual inductor [29]**	**Dual-phase multi-inductor [8]**	**12-level Dickson [5]**	**This work**
V_{in}**[V]**	48-54	48	36-60	48
V_{out}**[V]**	1-2	1-5	0.5-1	1
Switching frequency [KHz]	300	330	2500	1000
Inductors	2	4	2	2
Capacitors	5 C_{fly} + 1 C_{out}	3 C_{fly} +1 C_{out}	11 C_{fly} + 1 C_{out}	9 C_{fly} + 1 C_{out}
Power transistor	8 GaN	8 GaN	13 On-chip 5V MOSFET + 1 GaN	11 On-chip 5V MOSFET + 1 GaN
I_{omax}**[A]**	10	100	8	18
Peak efficiency when $V_{in} = 48$**V**	93%	90.9%	90.2%	90.6%
Power density $[W/in^3]$	225	440	998	2093*

* Calculated from 18 A maximum load current and power stage volume (around 0.0086 in^3) estimated from [5].

3 TOPOLOGY OF A 48V/3V MULTI-RESONANT DC-DC CONVERTER

In this chapter, a topology design of a 16-to-1 resonant DC-DC converter with multi-phase operation for the 48-V data centers is proposed at first. Then the design procedure of the parameters in the topology are described. Simulation results in cadence based on the calculated parameter values are shown in the end, and the results are also compared to some prior arts.

3.1 ARCHITECTURE

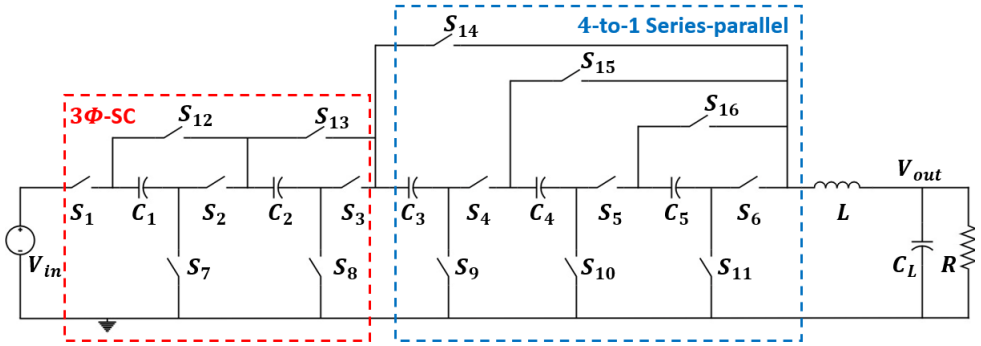

Figure 3.1: Topology of the proposed 48V/3V multi-resonant DC-DC converter

Fig.3.1 shows the schematic of the proposed 16-to-1 topology. It consists of a 3Φ-SC stage and a 4-to-1 series-parallel stage. 16 switches and 5 flying capacitors are used in the topology. Current waveforms of the inductor and flying capacitors, and gate control signal of the switches are shown in Fig.3.2. It has four phases. Phase 1 is the charging phase, while the other three phases are discharging phases.

During phase 1, the flying capacitors C_1 - C_5 are connected in series between the input voltage V_{in} and the inductor L. All the flying capacitors are resonantly charged. The necessary equation in Φ_1 is:

$$\Phi_1 : V_{in} = V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_{C5} + V_L + V_{out} \tag{3.1}$$

During phase 2, C_1 is discharged, and C_2 - C_5 are connected in series between the positive terminal of C_1 and the inductor L. The necessary equation in Φ_2 is:

$$\Phi_2 : V_{C1} = V_{C2} + V_{C3} + V_{C4} + V_{C5} + V_L + V_{out} \tag{3.2}$$

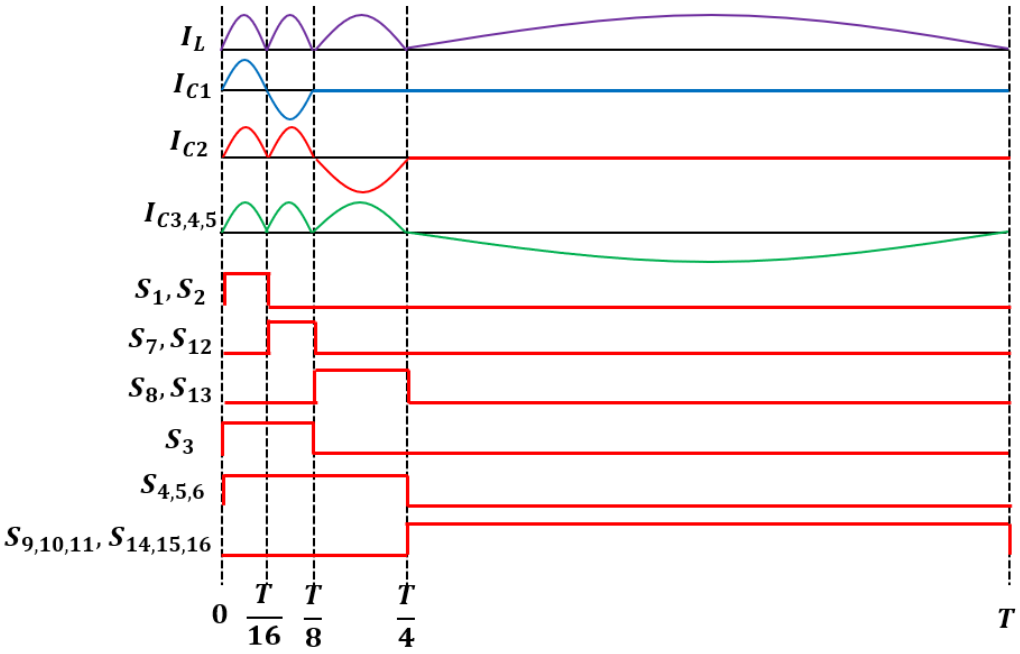

Figure 3.2: Current waveforms and control signals of the proposed converter

During phase 3, C_1 is disconnected. C_2 discharges into the series connection of C_3-C_5. The necessary equation in Φ_3 is:

$$\Phi_3 : V_{C2} = V_{C3} + V_{C4} + V_{C5} + V_L + V_{out} \tag{3.3}$$

During phase 4, both C_1 and C_2 are disconnected. C_3 - C_5 are connected in parallel. The necessary equation in Φ_4 is:

$$\Phi_4 : V_{C3} = V_{C4} = V_{C5} = V_L + V_{out} \tag{3.4}$$

By solving Eq.3.1 - Eq.3.4, flying capacitor voltages and output voltages can be achieved:

$$V_{c1} = \frac{1}{2} V_{in} \tag{3.5}$$

$$V_{c2} = \frac{1}{4} V_{in} \tag{3.6}$$

$$V_{c3} = V_{c4} = V_{c5} = \frac{1}{16} V_{in} \tag{3.7}$$

$$V_{out} = \frac{1}{16} V_{in} - V_L \tag{3.8}$$

During a whole period, due to the inductor voltage-second balance, V_L is zero. Thus, the ideal output voltage is:

$$V_{out} = \frac{1}{16} V_{in} \tag{3.9}$$

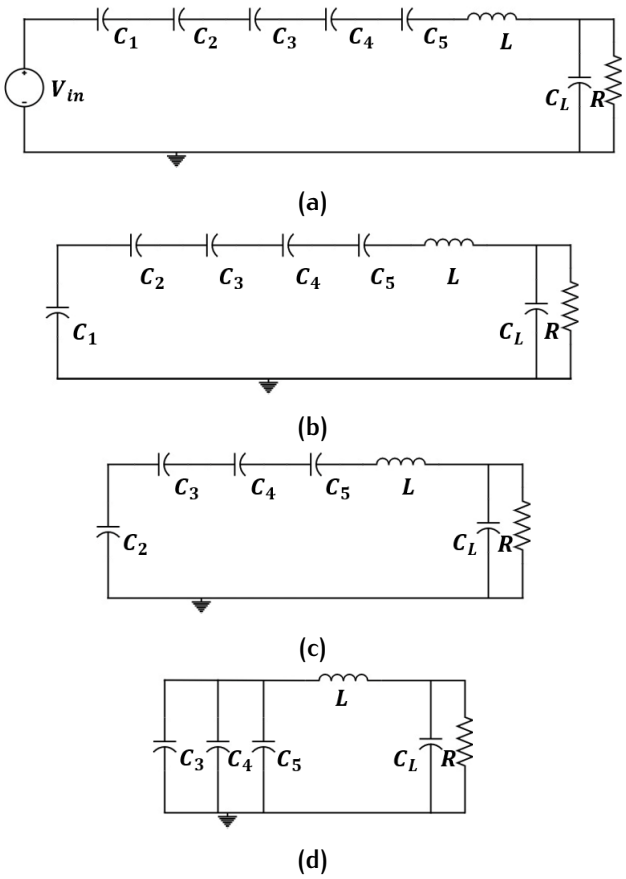

Figure 3.3: Operation phases of the proposed 16-to-1 SC DC-DC converter (a) Phases 1. (b) Phase 2. (c) Phase 3. (d) Phase 4.

The advantages of this topology are attributed to two parts.

- Multiple phases: For two-phase SC converter, for a given capacitor number k, the maximum step-up or step-down ratio is limited by the kth Fibonacci number F_k [25]:

$$M[k] = \frac{V_{out}}{V_{in}} = \frac{1 \leq P[k] \leq F_k}{1 \leq Q[k] \leq F_k} \tag{3.10}$$

  where, $F_1 = 1$, $F_2 = 2$, $F_n = F_{n-1} + F_{n-2}$. However, when multi-phase is applied, with the same number of capacitors k, the maximum conversion ratio is:

$$M[k]_{max} = 2^{k-1} \tag{3.11}$$

  which is greater than the conversion ratio calculated by Eq.3.10. Thus, with multiple phases, to achieve the same step-down ratio, fewer capacitors are needed. As shown in Fig.3.1, 5 flying capacitors are needed to achieve 16-to-1, while for two-phase SC converters, 5 flying capacitors can only obtain a step down ratio of 8.

- Resonance: For conventional SC converters, there is mismatch between capacitor initial voltages, which will cause charge redistribution loss and a large instantaneous current through the switches. Fig.3.4 shows the redistribution loss of connecting a voltage source to a capacitor and connecting two capacitors

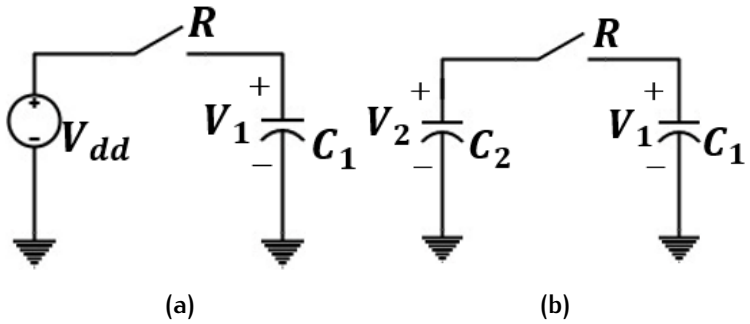

Figure 3.4: Redistribution loss of (a) connecting a voltage source to a capacitor and (b) connecting two capacitors.

Fig.3.4a shows a capacitor charged by a voltage source through a switch conduction resistance R with the initial voltage of V_1. The energy dissipated by R is given by:

$$E_{loss} = \frac{1}{2}C_1(V_{dd} - V_1)^2 \tag{3.12}$$

$$P_{loss} = \frac{1}{2}C_1(V_{dd} - V_1)^2 f_{sw} \tag{3.13}$$

Fig.3.4b shows two capacitors connected together, with initial voltage V_1 and V_2, respectively. The energy dissipated by R is given by:

$$E_{loss} = \frac{1}{2}(C_1 \parallel C_2)(V_1 - V_2)^2 \tag{3.14}$$

$$P_{loss} = \frac{1}{2}(C_1 \parallel C_2)(V_1 - V_2)^2 f_{sw} \tag{3.15}$$

From Eq.3.13 and Eq.3.15, power loss is related to the initial voltage difference between the voltage source and capacitor or between capacitors, but independent of the series resistance. Besides, initial voltage difference is inversely proportional to the capacitor value and switching frequency [22]. Thus, we have,

$$P_{loss} \propto \frac{1}{f_{sw}}, \frac{1}{C_{fly}} \tag{3.16}$$

To reduce the redistribution loss, either increase the switching frequency or increase the value of flying capacitors. However, higher switching frequency will lead to higher switching loss and bottom plate loss, while larger flying capacitor will increase the circuit size. However, with resonance, soft charging can

be achieved. With the additional inductor, minimum resistance of the converter can be reached at a lower switching frequency, and thus, the same efficiency can be achieved with lower switching frequency [22].

3.2 DESIGN

3.2.1 Resonant inductor current

Ignoring the parasitic resistance and assuming an infinite resonance quality factor, the instant resonant inductor current can be deduced.

During Φ_1, according to Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL), time-doman equations are as follows:

$$V_{in} = v_{C11} + v_{C21} + v_{C31} + v_{C41} + v_{C51} + L\frac{di_{L1}}{dt} + V_{out}, \tag{3.17}$$

$$i_{C11} = C_1\frac{dv_{C11}}{dt} = i_{L1}, \tag{3.18}$$

$$i_{C21} = C_2\frac{dv_{C21}}{dt} = i_{L1}, \tag{3.19}$$

$$i_{C31} = C_3\frac{dv_{C31}}{dt} = i_{L1}, \tag{3.20}$$

$$i_{C41} = C_4\frac{dv_{C41}}{dt} = i_{L1}, \tag{3.21}$$

$$i_{C51} = C_5\frac{dv_{C51}}{dt} = i_{L1}, \tag{3.22}$$

where, v_{Ci1} and i_{Ci1} are the instant voltages and currents of C_i, respectively; i_{L1} is the instant inductor current during Φ_1. Combining Eq.3.17 - Eq.3.22, we can get:

$$\frac{i_{L1}}{C_1} + \frac{i_{L1}}{C_2} + \frac{i_{L1}}{C_3} + \frac{i_{L1}}{C_4} + \frac{i_{L1}}{C_5} + L\frac{d^2i_{L1}}{dt^2} = 0. \tag{3.23}$$

By solving Eq.3.23, a solution can be obtained:

$$i_{L1} = A_1 \cdot \sin\left(\frac{1}{\sqrt{L\left(C_1 \parallel C_2 \parallel C_3 \parallel C_4 \parallel C_5\right)}}t\right), \tag{3.24}$$

Similar deduction can be used for other three phases. The instant inductor current equations are as follows:

$$i_{L2} = A_2 \cdot \sin\left(\frac{1}{\sqrt{L\left(C_1 \parallel C_2 \parallel C_3 \parallel C_4 \parallel C_5\right)}}t\right), \tag{3.25}$$

$$i_{L3} = A_3 \cdot \sin\left(\frac{1}{\sqrt{L\left(C_2 \parallel C_3 \parallel C_4 \parallel C_5\right)}}t\right), \tag{3.26}$$

$$i_{L4} = A_4 \cdot \sin\left(\frac{1}{\sqrt{L\left(C_3 + C_4 + C_5\right)}}t\right), \tag{3.27}$$

3.2.2 Capacitor values

According to the capacitor charge balance, the net charge flowing into a capacitor is zero during a whole period. Thus, the duration of each phase can be obtained:

$$T_1 = T_2 = \pi\sqrt{L\left(C_1 \parallel C_2 \parallel C_3 \parallel C_4 \parallel C_5\right)} = \frac{1}{16}T \tag{3.28}$$

$$T_3 = \pi\sqrt{L\left(C_2 \parallel C_3 \parallel C_4 \parallel C_5\right)} = \frac{1}{8}T \tag{3.29}$$

$$T_4 = \pi\sqrt{L\left(C_3 + C_4 + C_5\right)} = \frac{3}{4}T \tag{3.30}$$

Thus, the required relationship among capacitor values for a perfect resonant operation is:

$$C_3 = C_4 = C_5 = C \tag{3.31}$$

$$C_2 = \frac{1}{9}C \tag{3.32}$$

$$C_1 = \frac{1}{36}C \tag{3.33}$$

3.2.3 Output impedance

The equivalent model of each phase of a resonant SC converter can be assumed as Fig.3.5 [26]. As the resonant converter system needs to be designed in underdamped $(\frac{R_i}{2}\sqrt{\frac{C_i}{L}} < 1)$ to achieve soft-charging [22], the current in Fig.3.5 is given as:

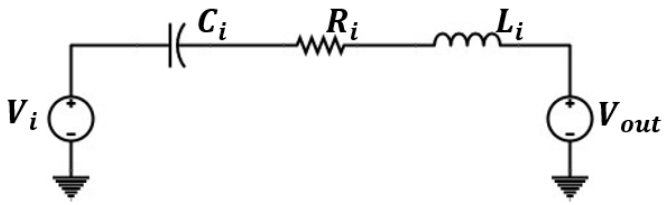

Figure 3.5: Equivalent model for any phase of a resonant converter

$$I_i(t) = k_i e^{-tR_i/(2L)} \sin(\omega_i t + \phi_i) \tag{3.34}$$

where, ω_i is the damped resonance frequency and equals to $\sqrt{\frac{1}{LC_i} - (\frac{R_i}{2L})^2}$.

For a resonant converter, for each phase, $t_i = \frac{\pi}{\omega_i}$ and $\phi_i = 0$. Charge flowing into the output during phase i is defined as:

$$q_i = \int_0^{t_i} I_i(t)dt = k_i L_i C_i \omega_i \left(1 + e^{-R_i \pi/(2L_i\omega_i)}\right) \tag{3.35}$$

The energy dissipated in phase i due to conduction loss is given as:

$$E_i = \int_0^{t_i} R_i I_i^2(t)dt = \frac{k_i^2 L_i^2 C_i \omega_i^2}{2} \left(1 - e^{-R_1 \pi/(L_i\omega_i)}\right) \tag{3.36}$$

The effective resistance R_{eff} is defined as Eq.3.37. $\alpha_i = q_i/q_{out}$ is defined to simplify the calculations, where q_i is the charge delivered to the output in phase i.

$$R_{eff} = \frac{\sum E_i}{f_{sw} (\sum q_i)^2} \tag{3.37}$$

Combining Eq.3.37 and Eq.3.36 gives:

$$R_{eff} = \frac{\sum \frac{\alpha_i^2}{C_i} \tanh\left(\frac{R_i \pi}{4L\omega_i}\right)}{2 f_{sw} (\sum \alpha_i)^2} \tag{3.38}$$

For a high quality factor resonant converter, Eq.3.38 reduces to:

$$R_{eff} \approx \frac{\sum \frac{\pi \alpha_i^2}{4\sqrt{C_i L}} R_i}{2 f_{sw} (\sum \alpha_i)^2} \tag{3.39}$$

For the proposed 16-to-1 converter,

$$\alpha = [\frac{1}{16}, \frac{1}{16}, \frac{1}{8}, \frac{3}{4}] \tag{3.40}$$

Considering $T_i = \pi\sqrt{C_i L} = \alpha_i / f_{sw}$, Eq.3.39 can be simplified to:

$$R_{eff} = \frac{\pi^2}{8} \sum (\alpha_i R_i) \tag{3.41}$$

For the proposed 16-to-1 converter,

$$R_1 = R_{on1} + R_{on2} + R_{on3} + R_{on4} + R_{on5} + R_{on6} + ESR_{C1} + ESR_{C2} + ESR_{C3} + ESR_{C4} + ESR_{C5} + DCR_L \tag{3.42}$$

$$R_2 = R_{on7} + R_{on12} + R_{on3} + R_{on4} + R_{on5} + R_{on6} + ESR_{C1} + ESR_{C2} + ESR_{C3} + ESR_{C4} + ESR_{C5} + DCR_L \tag{3.43}$$

$$R_3 = R_{on8} + R_{on13} + R_{on4} + R_{on5} + R_{on6} + ESR_{C2} + ESR_{C3} + ESR_{C4} + ESR_{C5} + DCR_L \tag{3.44}$$

$$R_4 = (R_{on9} + R_{on14} + ESR_{C3}) \parallel (R_{on10} + R_{on15} + ESR_{C4}) \parallel (R_{on11} + R_{on16} + ESR_{C5}) + DCR_L \tag{3.45}$$

where R_i is the equivalent resistance in the ith phase; R_{oni} is the on-resistance of the ith switch; ESR_{Ci} and DCR_L are the series resistance of C_i and L in Fig.3.1, respectively.

3.2.4 Parameters design

Step 1: switches choosing

The ideal voltage stress of each switch is listed in Table 3.1.

Table 3.1: Ideal voltage stress of the switches in the proposed converter

Switch	Ideal voltage stress
S_1, S_2, S_7, S_{12}	$\frac{1}{2}V_{in}$
S_3, S_8, S_{13}	$\frac{1}{4}V_{in}$
S_9, S_{14}	$\frac{3}{16}V_{in}$
S_{10}, S_{15}	$\frac{1}{8}V_{in}$
S_4, S_5, S_6, S_{11}, S_{16}	$\frac{1}{16}V_{in}$

Step 2: switching frequency design

Switching loss for each power switch is given as:

$$P_{SW,i} = (Q_{G,i}V_{GS,i} + Q_{OSS,i}V_{B,i})\, f_{SW} \tag{3.46}$$

where $Q_{G,i}$ and $Q_{OSS,i}$ are the total gate charge and output charge of switch, respectively; $V_{GS,i}$ and $V_{B,i}$ are the gate-to-source voltage and voltage swing of the i-th power switch, respectively; f_{SW} is the switching frequency. The total switching loss is:

$$P_{SW} = \sum_{i=1}^{16} \left(Q_{G,i} V_{GS,i} + Q_{OSS,i} V_{B,i} \right) f_{SW} \tag{3.47}$$

The total conduction loss is given as:

$$P_{Cond} = I_{out}^2 R'_{eff} \tag{3.48}$$

where R'_{eff} is similar to R_{eff} in Eq.3.41 but excluding the parasitic resistances of capacitors and inductor. To optimize the efficiency of the proposed converter, Eq.3.47 and Eq.3.48 needs to be equal at the optimal load. Thus, a nearly optimum switching frequency 15kHz can be obtained. In practical, to offset the impacts of component tolerance variations and to lower the RMS current of switches, capacitors and inductor, the converter is run at a slightly higher frequency [2].

Step 3: capacitors values design

The voltage ripple of each flying capacitors are shown in Eq.3.49 - Eq.3.51.

$$\Delta V_{C1} = \frac{I_{out,max} \times T_{\phi_1}}{C_1} = \frac{I_{out,max} \times \frac{1}{16}}{f_{SW} \frac{1}{36} C} \tag{3.49}$$

$$\Delta V_{C2} = \frac{I_{out,max} \times T_{\phi_3}}{C_2} = \frac{I_{out,max} \times \frac{1}{8}}{f_{SW} \frac{1}{9} C} \tag{3.50}$$

$$\Delta V_{C3,4,5} = \frac{I_{out,max} \times T_{\phi_4}}{C_{3,4,5}} = \frac{I_{out,max}/3 \times \frac{3}{4}}{f_{SW} C} \tag{3.51}$$

Thus, the biggest voltage ripple occurs at capacitor C_1. Ideally, in resonant mode, ripple voltage can be as large as the DC voltage of the capacitor [33]. But the choosing of voltage ripple is also limited by the voltage stress of the connected switches.

Step 4: inductor value design

Combining Eq.3.28 -Eq.3.33, the inductor value can be deduced as:

$$L = \frac{1}{\pi^2 f_{SW}^2 \frac{16}{3} C} \tag{3.52}$$

3.3 SIMULATION RESULTS

The converter was designed and simulated in cadence. Table 3.2 lists the component parameters and operating parameters. The GaN Spectre model of EPC2024 and

Table 3.2: Component parameters

Parameter Name	Parameter Symbol	Parameter Value
Input voltage	V_{in}	48 V
Output voltage	V_{out}	3 V
Switching frequency	f_{SW}	30 kHz
Flying capacitors	C_3, C_4, C_5 C_2 C_1	375 μF 41.7 μF 10.42 μF
Output capacitor	C_L	220 μF
Inductor	L	225 nH, 0.63 mΩ
Power switches	S_1, S_2, S_7, S_{12} others	EPC2024 EPC2023

EPC2023 provided by EPC are used. The dead-time between each phase is set to 10 ns.

Fig.3.6 illustrates the output voltage, inductor current and flying capacitor voltages waveforms with an 8-A load. The converter exhibits an output voltage of 2.96 V with a voltage ripple of 72 mV. The converter is also able to handle large load transient, shown in Fig.3.7. When load current steps up from 0 A to the maximum load current 30 A, the undershoot voltage is 0.8 V and the recovery time is about 40 μs. When load current steps down, the recovery time is 100 μs, and the overshoot voltage is 0.82 V.

The simulated efficiency values and output voltage in a range of load current are shown in Fig.3.8 and Fig.3.9, respectively. The converter achieves a peak efficiency of 96.94% at 8.4-A load. For a large range of load current from 2.5 A to maximum 30 A, the efficiency is above 95%. For the output voltage, the average value drops to about 2.863 V at the maximum load of 30 A.

Table 3.3 compares this proposed resonant converter with other state-of-the-art designs. Compared with [2], [36] and [33], the proposed converter achieves a higher voltage conversion ratio, 16-to-1. For a 48 V input voltage, 3 V output voltage can be obtained. Compared with [11] and [10], with same conversion ratio, the proposed converter achieves much higher efficiency, more than 6% and 3%, respectively.

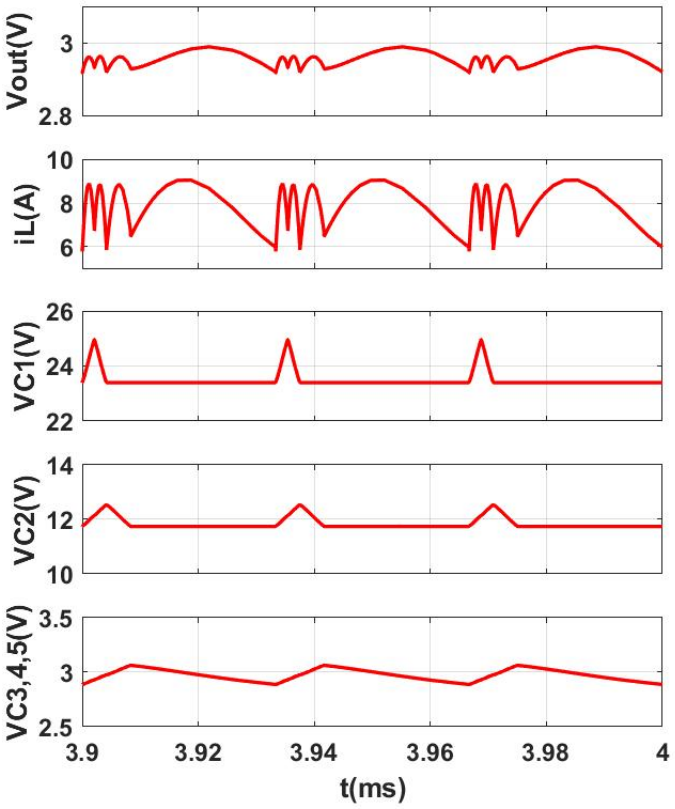

Figure 3.6: Simulated key voltages and currents of the proposed converter

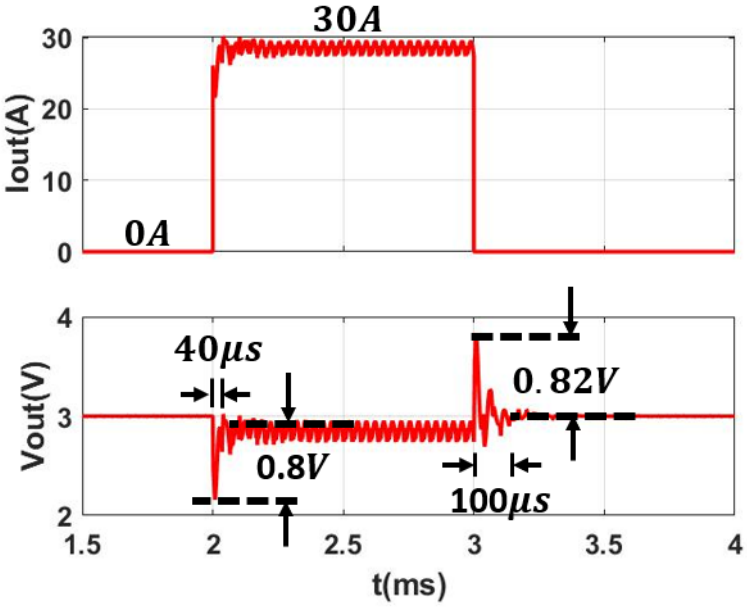

Figure 3.7: Simulated load transient responses between o and maximum load

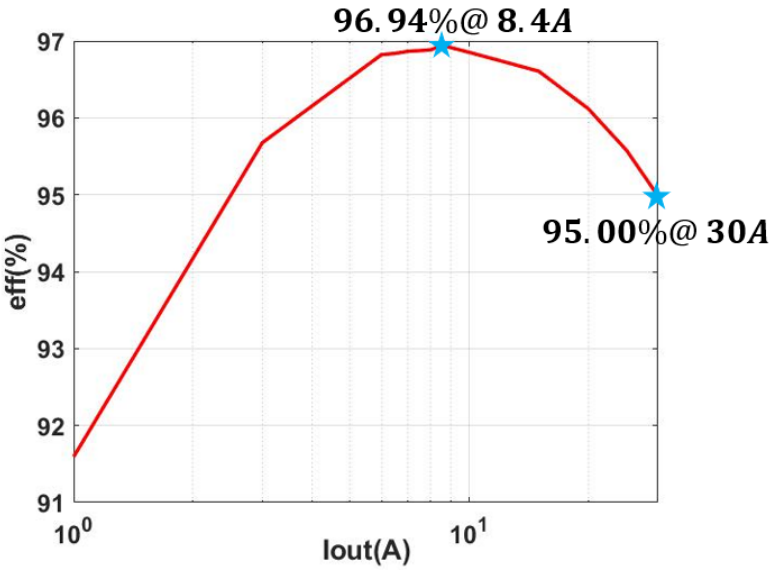

Figure 3.8: Simulated power efficiency

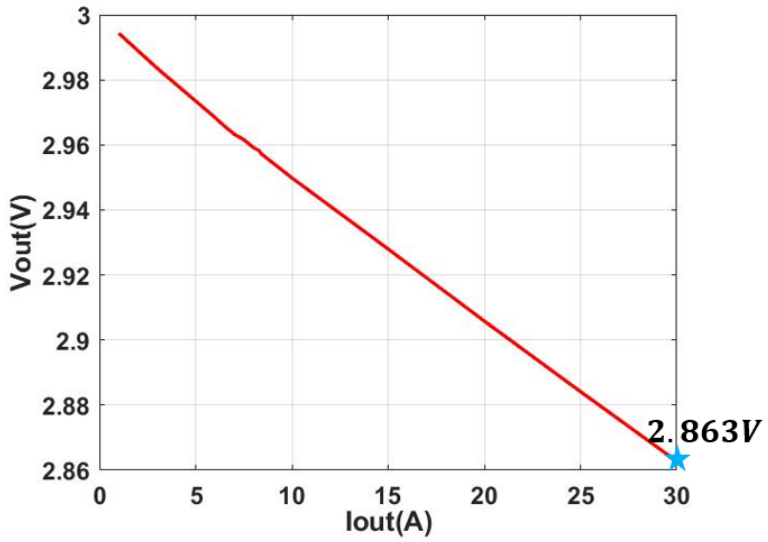

Figure 3.9: Simultaed output voltage versus the load current

Table 3.3: Comparison of this work and the previous work

Topology	Voltage ratio	Output current	Power efficiency (without gate driving loss)
This work (3Φ-SC series-parallel)	48-to-3V	30 A	full load: 95.0%, peak: 96.94%
Cascaded series-parallel [2]	48-to-6V	70 A	full load: 95.3%, peak: 98.6%
Multi-resonant doubler [36]	48-to-6V	40 A	full load: 96.0%, peak: 98.6%
Re3Φ-SC [33]	48-to-12V	10 A	full load: <90%, peak: ~98%
SDIH Dickson[11]	48-to-3V	45 A	full load:<90%, peak: 89.8%
DIH Dickson[10]	48-to-3V	50 A	full load:~ 91%, peak: 93.8%

4 FUTURE WORK

4.1 FUTURE WORK FOR THE 10-LEVEL DIHC CONVERTER

Potential further improvements to this design are listed below:

- Split phase control to properly regulate the turn-on time of the high-side switches can be done to eliminate the charge redistribution loss.
- Switch's sizing and switching frequency can be chosen carefully to achieve a better efficiency.

4.2 FUTURE WORK FOR THE 48V/3V MULTI-RESONANT DC-DC CONVERTER

In the current design, only the topology is proposed and the calculation method of each parameter is given. Potential further work to this design are listed below:

- The type of switches can be selected carefully to reach a better efficiency for this converter. Five switches in the topology have an ideal voltage stress of only 3 V. GaN switch may not be a best choice for them.
- PCB test is expected to be done to verify the performance of the proposed converter.
- Although there is no necessity for regulation of the output voltage in the first stage of the 48-V architecture, feedback control is important when this converter is used in other applications. A potential feedback strategy for a resonant-mode converter is to use the off-time modulation [33].

5 CONCLUSIONS

In this thesis, a 10-level DIHC is presented, which converts 48 V directly to 1 V at 1-MHz switching frequency for data center applications. The proposed converter takes full advantage of the voltage pressure on the 5-V transistors. This converter exhibits higher efficiency and improved power density compared with the state-of-the-art works, achieving 90.6% peak power efficiency with loads up to 18 A and about 2093 W/in^3 power density. Besides, the efficiency can stay above 80% in a large range of load current from 2 A to 18 A. The performance of the proposed design has been well verified with post-layout simulations designed in a 0.18-μm BCD technology.

Also, this thesis proposes a novel 16-to-1 multi-resonant DC-DC converter to convert 48 V to 3 V. With multi-phase operation, the proposed converter uses fewer components than the traditional two-phase SC converter. Besides, the resonant operation mode further improves the efficiency. GaN devices with small on-resistance are used to reduce the power loss of switches. Simulation results show that a peak efficiency of 96.94% can be obtained. The maximum load is up to 30 A, with a full load efficiency of 95%. And for a large range of load current from 2.5 A to maximum load, the efficiency can be above 95%.

6 LIST OF PUBLICATIONS

Y Hua, Q Lu, S Li, S Du, "A 90.6% Efficient, 0.333 W/mm^2 Power Density Direct 48V-to-1V DIHC with Delay-line Based V2D Controller," IEEE Transactions on Circuits and Systems II: Express Briefs, 2022. (Under review)

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