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REVIEW

Challenges and Strategic Drivers in 3D IC Failure Analysis: Closing the Critical Gaps using Designs for Analysis

Lesly Zaren Endrinal · Willem D. van Driel · Guo Qi Zhang

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Abstract The relentless pursuit of high-performance computing driven by 5G/6G, artificial intelligence, autonomous driving, Internet of things (IoT), quantum computing, and data centers has pushed traditional integrated circuit scaling to its limits [1]. As lithography challenges and escalating manufacturing costs slow Moore's law, the industry has pivoted toward design technology co-optimization (DTCO) and system technology co-optimization (STCO). These methodologies extend device performance through process and package scaling, introducing complex transistor architectures like gate-all-around (GAA), forksheets, and complementary FETs (CFET), alongside system-level innovations like backside power deliver networks (BPDN), 3D IC, and heterogeneous integration. While these advancements optimize power, performance, area, and cost (PPAC), they inadvertently create a significant bottleneck in failure analysis (FA). Advanced package technologies such as co-packaged optics, heterogeneous integration, and chiplets have fundamentally disrupted electrical fault isolation (EFI) flows. Complex package routing and dense 3D stacking of multiple components now pose severe challenges to fault isolation. Historically, the industry relied on design for test (DFT) to screen defects and design for diagnosis (DFD) to predict failure locations. However, in advanced nodes, diagnostic quality is often insufficient to characterize underlying failure mechanisms, and design complexity restricts accessibility and controllability of internal signals needed for EFI. This paper reviews the impact of DTCO and STCO on failure analysis, identifying key challenges and drivers. FA has traditionally been treated as a post-silicon afterthought; chip and hardware designs rarely consider its workflows. Yet, as new technologies evolve, FA becomes a critical bottleneck to yield learning, slowing down yield ramp-up and time-to-market. This paper calls for a strategic "left-shift" of FA requirements early into the design cycle through design for analysis (DFA). By integrating dedicated DFA features, manufacturers can bridge the gap between silicon design and post-silicon debug, transforming FA into a proactive driver of yield.

Keywords Failure analysis · 3D IC · Heterogeneous integration · Electrical fault isolation · Photon emission microscopy · Laser stimulation · Laser probing

Introduction

Failure analysis (FA) plays a key role throughout the entire silicon product lifecycle: from initial development and yield ramp-up, to long-term performance and reliability, helping identify critical test, design marginality and process issues in a timely and efficient manner to ensure the development of high-quality, cost-effective, and reliable chips. Failure analysis has 2 main phases: electrical fault isolation (EFI) and physical failure analysis (PFA). The goal of EFI is to electrically isolate the failure to a significantly smaller area (usually block or component level) using various fault isolation techniques, as shown in Fig. 1. EFI is typically a nondestructive approach that preserves the defect or failure mechanisms to correlate with the

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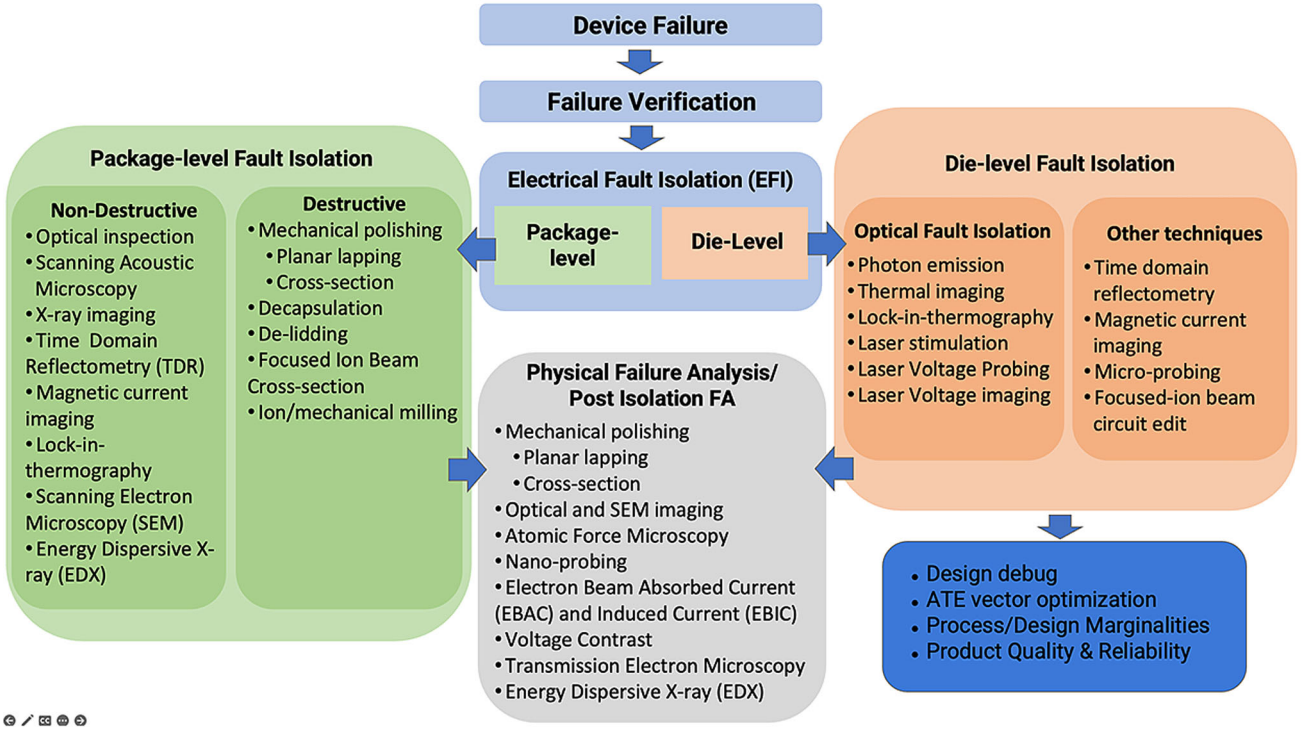


Fig. 1 Typical failure analysis flow

failures originally observed [2]. Advanced fault isolation methodologies utilize emission microscopy or laser-based optical tools, which can be nonintrusive or intrusive, respectively [3].

Most advanced designs incorporate design for test (DFT) architectures that enable comprehensive fault detection and diagnosis for both logic (using automated test pattern generation or ATPG) and memory (using memory built in self-test or MBIST). The diagnostic results provide a prediction of the failure sites, facilitating a more efficient and directed physical failure analysis (PFA).

However, diagnostic results are sometimes insufficient to support a direct PFA approach due to two primary factors:

- *Diagnosstic Resolution and Accuracy* While a single callout with a 100% confidence score is ideal, complexity of certain failures often leads to dozens of potential candidates or low-confidence scores, making direct PFA infeasible. An example of a diagnostic result with 100% score and two callouts is shown in Fig. 2A. Ideally, a good quality diagnosis should have fewer than 3 suspects with confidence level scores above 75% [4].
- *Physical Area of Interest (AOI)* When a diagnostic suspect area spans more than 100 µm (potentially reaching into the millimeter range), delayering techniques become extremely challenging, if not impossible. An example of a diagnostic AOI with dozens of callouts spanning over a millimeter is shown in Fig. 2B.

Consequently, electrical fault isolation (EFI) has become a critical step in the FA workflow, isolating the failure AOI into a smaller region to facilitate a more successful and feasible PFA. Furthermore, EFI is not only used for defect identification, but is increasingly utilized for test vector optimization and silicon characterization to identify process-to-design marginalities.

Key Drivers of Failure Analysis Challenges

The increasing design complexity of devices, coupled with DTCO and STCO, is introducing new challenges to electrical fault isolation (EFI) and physical failure analysis (PFA). The main drivers of these FA challenges include:

(a) Transistor Scaling (Gate-All-Around, Forksheet, Complementary Field Effect Transistors)
Electrical fault isolation involves optical fault isolation (OFI) techniques that utilize visible, near-infrared (NIR), and mid-wave IR (MWIR) wavelengths (from 577 nm 5 µm) to characterize and diagnose logic cells from inside the chip. These

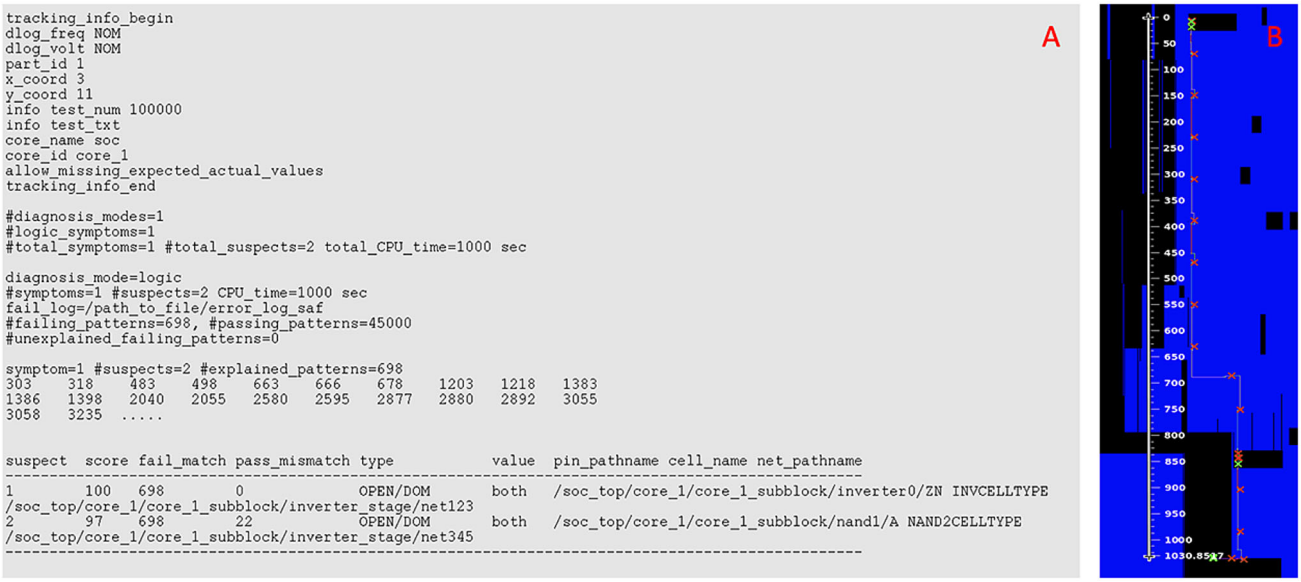


Fig. 2 (**A**) Example of a diagnostic callout, (**B**) multiple diagnostic callouts mapped on FA CAD

Table 1 Overview of optical fault isolation techniques

Photon emission (Pem) (1-2 um)	Thermal imaging (> 3 um)	Laser voltage imaging/probing (577 nm N 1340 um)	Dynamic laser stimulation (~ 1-1.3 um)
Optical response (photon emission) resulting from electrical stimuli (aka electroluminescence). Localization of resistive shorts/opens and leakage failures, ESD damages	Lock-in thermography: for the detection of low-level leakages	E-field variations in a switching transistor modulated the incident laser to provide timing information. Laser voltage imaging (LVI)	Laser is used to alter the electrical performance of a transistor or component.
Defect isolation of hard failures (stuck-at ATPG fails and MBIST)	Hot spot analysis for identifying location of shorts/leakages in the package or die	Provides a visualization (frequency map) of transistors that switch at a specific frequency (scan clock, data, and periodic signals)	Photocurrent laser stimulation (PLS)
IDDQ vector debug	Thermal mapping provides an accurate temperature mapping of the package/die at the surface	Laser voltage probing (LVP)	Speeds up transistors (reduce Vt): 1064 nm wavelength
		Provides accurate timing information of signals (such as propagation delay, duty cycle, frequency, period, etc.)	Speed path sensitivity
			Thermal laser stimulation (TLS)
			Introduces localized heating (1320 nm)
			Resistive defect localization, thermal sensitivity

techniques include photon and thermal emissions, dynamic laser stimulation (DLS), and laser voltage imaging/probing (LVX). The key features of each OFI technique are summarized in Table 1.

The theoretical limit of optical resolution for these OFI tools rely on Abbe's criterion which dictates that the resolution of any conventional optical system is limited by the wavelength (λ) of light used and the numerical aperture (NA) of the objective lens:

$$\text{Resolution} = \frac{\lambda}{2\text{NA}}$$

Table 2 shows the theoretical optical resolution as a factor of wavelength and numerical aperture (NA). The most commonly used wavelengths for EFI range from 1 to 1.8 µm, resulting in ~ 200–300 nm resolution. Laser-based tools utilize 1340 and 1064 nm wavelengths. What this translates to is that **the resolution of our current optical FI tools cannot catch up with the scaling of transistors**, as shown in Fig. 3. Since the typical spot size of an OFI tool is about ~ 200–300 nm, this means that

there are about at least 10 transistors covered with the laser spot in the latest technologies (2, 3 nm), as shown in Fig. 4. Tool vendors explore intermediate wavelengths such as 1122 nm, mitigating the invasiveness from shorter 1064 nm wavelength, while offering better optical resolution than conventional 1340 nm lasers [5]. The development of visible light prober (VLP), which utilizes shorter laser wavelengths such as 785 and 577 nm, provides improved optical resolution of 130 and 90 nm, respectively. Silicon transmission rate is better on the infrared region, improving with longer laser wavelength [3]. However, as the wavelength shortens, the laser absorption increases, which requires the silicon to be much thinner, in the order of 1–5 µm [6–8]. This requirement raises sample preparation complexity and consistency issues, especially as dies become increasingly larger. Furthermore, the shorter wavelength laser induces more photocarriers in the substrate, resulting in slow edges during laser probing and in some cases, can be even destructive. Thermal mitigation is also a concern for VLP applications, as the remaining silicon thickness (RST) is very minimal, causing thermal runaway and device damage even before the analysis starts.

In addition, as part of design for manufacturability (DFM), DTCO introduces design rules that eliminate layout nonuniformity, thereby creating **issues with CAD-to-image tool alignment**, as optical FI tools reach the resolution limits. CAD navigation and alignment are crucial to every EFI step to accurately identify the failure location. Figure 5A shows a dense logic area within a 4 nm test chip with barely any recognizable feature, alongside the corresponding CAD layout for that area (Fig. 5B). The accuracy of fault isolation heavily depends on how well the analyst could align the CAD layout with the actual image of the transistors. While shorter laser wavelengths (577 to 785 nm) can be utilized for better resolution, such optical systems require the silicon to be thinned to about 1 to 5 µm, making sample preparation very challenging.

Furthermore, **as the transistor VDD continuously reduces to meet low power needs, the photon emission spectrum moves to the higher wavelength** (closer to 1800 nm). This phenomenon is called "red shift" and

Table 2 Optical resolution limit based on Abbe's criterion

Wavelength (µm)	Numerical aperture	Spatial resolution (µm)	Application	Required remaining silicon thickness (RST) for EFI
5	2.2	1.14	Thermal	≥ 50 µm
3	2.2	0.68	Thermal	≥ 50 µm
2	2.9	0.34	PEM	≥ 50 µm
1.9	2.9	0.33	PEM	≥ 50 µm
1.8	2.9	0.31	PEM	≥ 50 µm
1.55	2.9	0.27	PEM	≥ 50 µm
1.34	3	0.22	DLS/LVX	≥ 50 µm
1.154	3	0.19	DLS/LVX	≥ 50 µm
1.064	3.1	0.17	DLS/LVX	≥ 50 µm
0.785	3.1	0.13	DLS/LVX	~ 5 µm
0.577	3.1	0.09	DLS/LVX	~ 1-2 µm

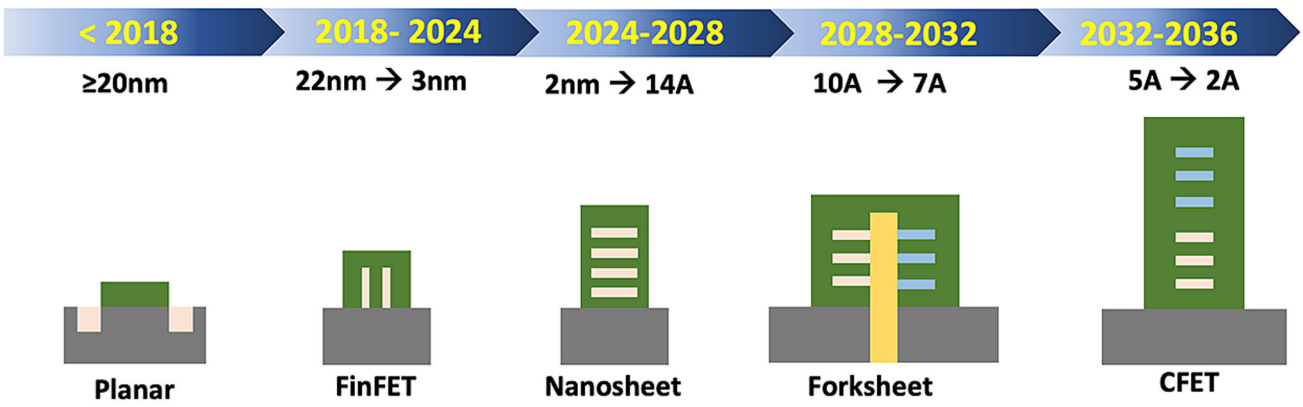


Fig. 3 Transistor scaling and roadmap from IMEC [8, 76]

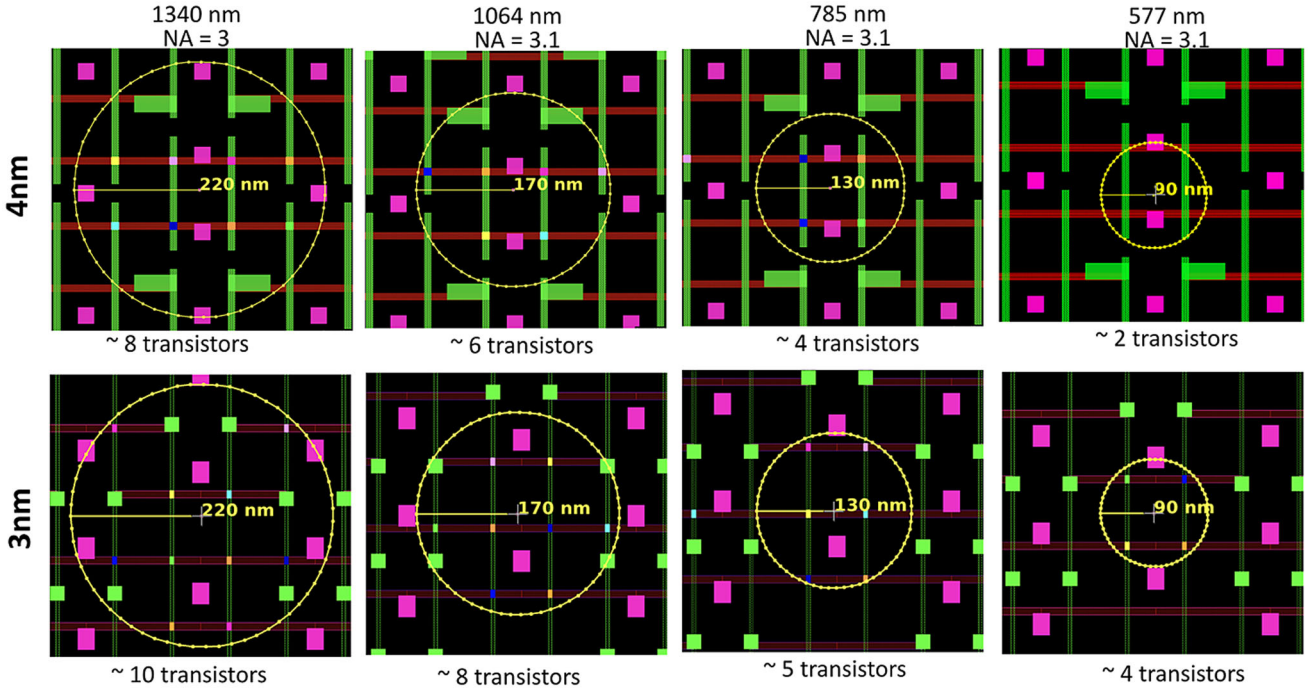


Fig. 4 Number of transistors covered by laser spot size, 3 vs 4 nm

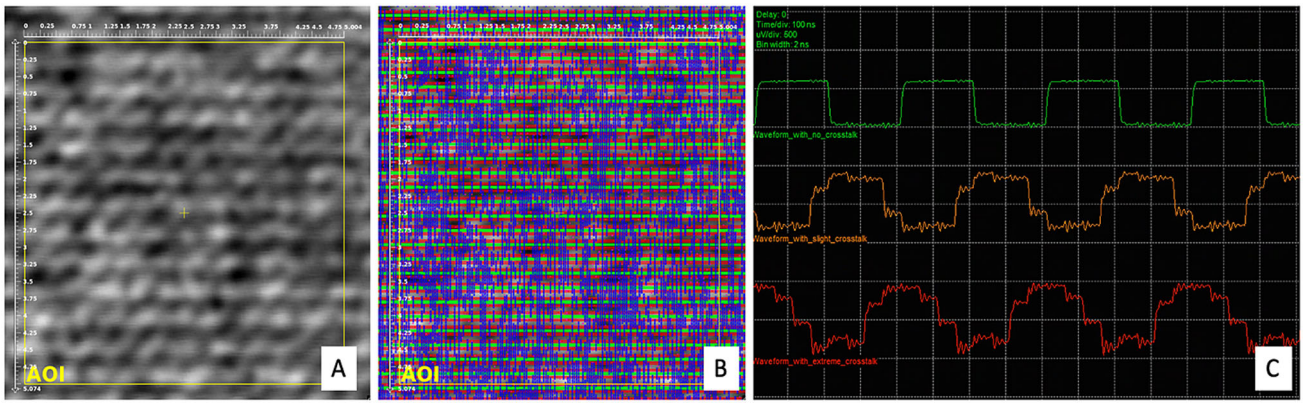


Fig. 5 (**A**) 1340 nm laser image of a 4 nm test chip, (**B**) corresponding CAD layout, (**C**) laser probing without (green), with slight (orange) and with significant (red) cross talk

results in photon emission spots that become bigger and less resolved (Abbe's criterion). Hence, **electrical fault isolation becomes ambiguous and uncertain, leading to lower physical FA success rates.**

(b) Backside Power Delivery Network

To optimize PPAC and enable Moore's law beyond 3 nm, the backside power delivery network (BPDN) scheme had become part of the technology roadmap for major foundries like Intel, TSMC, and Samsung. The BPDN will become a significant technology driver in the future due to its promise of optimized PPAC. BPDN comes in two flavors: FinFET and nanosheet (to maximize scaling). Figure 6 shows an example of a conventional frontside power distribution network which often experiences congestion because both power and signal routing share the same space on the top side of the die. This often leads to longer signal and power paths, causing IR drops and efficiency issues. This concern for congestion was finally addressed by BPDN, separating the routing of power (at the bottom of transistors) and signals (on top of the transistors), freeing up space on the top side for signal routing.

Figure 6 demonstrates that **BPDN will block any**

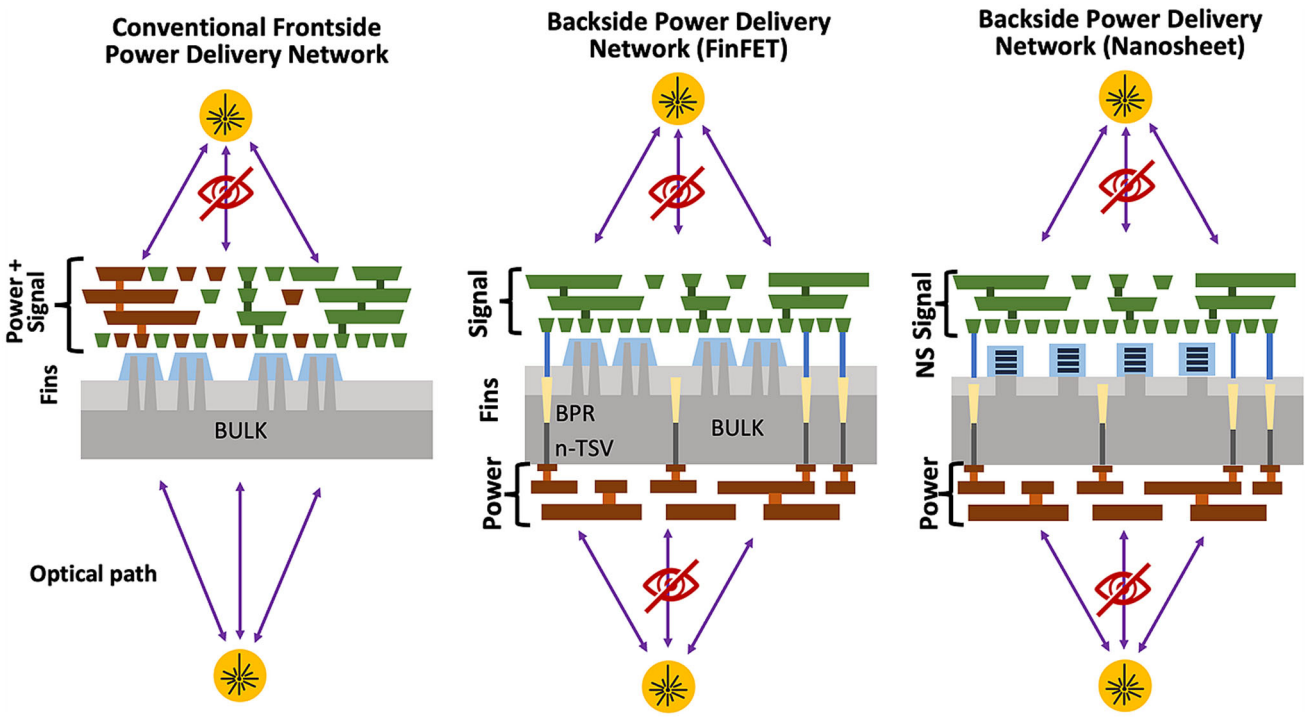


Fig. 6 Conventional frontside PDN versus backside PDN

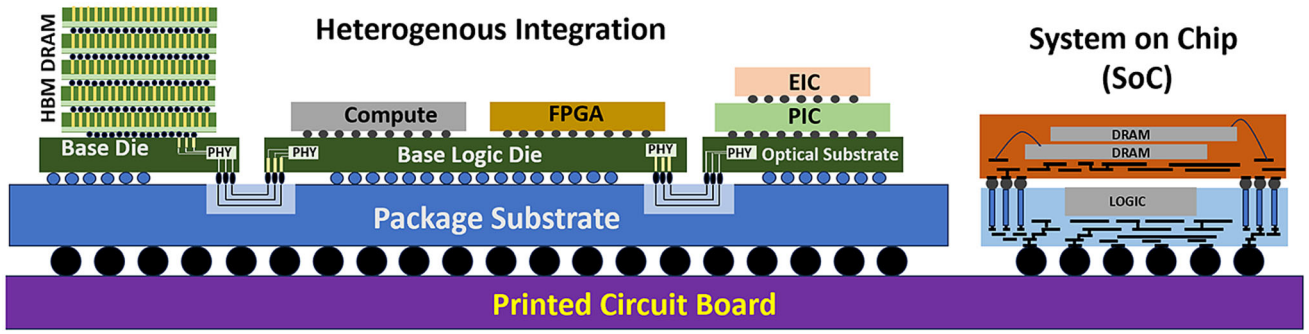


Fig. 7 Example of STCO (heterogeneous integration)

optical path from either the top or bottom side of the transistor, because of the presence of opaque metal routing. This enabling technology will render conventional OFI techniques ineffective, and therefore, **it is very critical to develop designs for test and FA that will help promote yield learning despite these challenges.**

(c) Advanced Packaging (3D IC/Heterogeneous Integration/ Chiplets)

System-technology co-optimization (STCO) is a methodology that optimizes the entire system design, including the process and package technology, and normally goes hand-in-hand with DTCO to extend the capability beyond Moore's law [9]. STCO improves the performance of a product by introducing advanced packaging techniques such as heterogeneous integration, chiplets and 3D IC, as shown in Fig. 7.

The increasing complexity of packages is also posing significant hurdles to performing failure analysis. These challenges include:

- *Obstruction of Line-of-Sight* Most OFI tools require direct line-of-sight access to the transistor. The stacking of multiple dies obstructs optical access to the transistor channels. Removal of overlying components may not always be possible due to the interdependency between different stacked dies in the package.

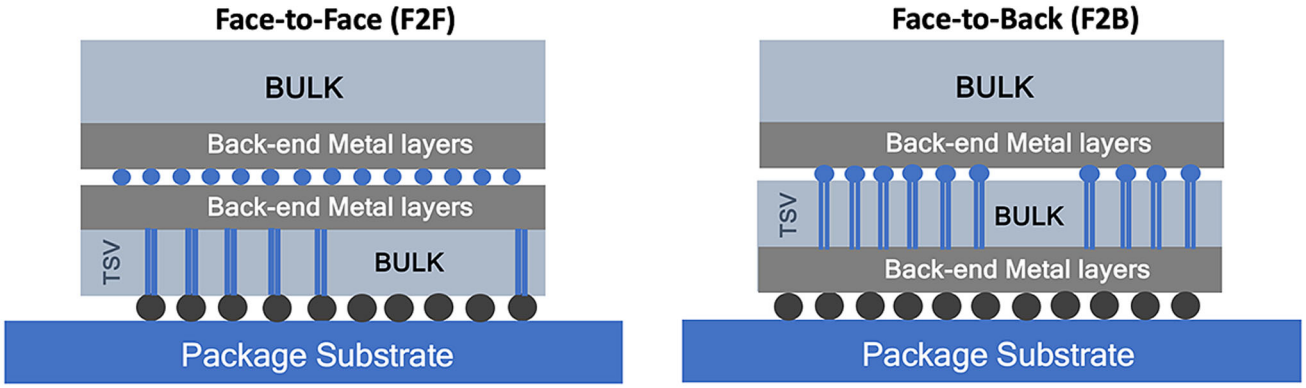


Fig. 8 Face-to-face versus face-to-back 3D IC configuration

Furthermore, depending on the 3D IC configuration (face-to-back or face-to-face), as shown in Fig. 8, direct optical access to the transistor channel may not be possible.

- *Die vs Package Failure* As more and more chips are integrated into one package, it becomes more challenging to isolate the failure: Is it in the die or the package? How to detect and diagnose marginal failures and identify new 3D IC package failure mechanisms? Pinpointing the actual location of the defect in a complex package will become difficult due to the lack of accessibility to the chip [10]. This is where the importance of design for test and diagnosis becomes crucial in predicting the location of a defect and understanding the failures.
- *Very Small Interconnects, Limited Tool Resolution* As the interconnects approach submicron pitch, similar to the OFI tools, current existing imaging tools such as the x-ray microscope (XRM) and scanning acoustic microscopes (SAM) are approaching tool resolution limits as well. EFI tools such as time domain reflectometer (TDR) and magnetic current image (MCI) microscope have resolution in the tens of microns, making it difficult to isolate and localize hairline cracks and very small defects within the package, especially for hybrid bonding and bump pitch below 10 µm. Furthermore, conventional TDR suffers from resolution challenges due to the distance of the defect to the probe requiring very high speed time resolution. Electro optical terahertz pulse reflectometry was developed to address this challenge [11–13]. By generating a terahertz pulse using an ultrafast laser and a pair of photoconductive switches, EOTPR is able to improve the detectability of defects compared to a conventional TDR, as a result of a faster rise time, greater SNR, and reduced jitter [14].
- *Observability and Accessibility of Interfaces Connecting Different Chip Pins* One of the challenges for adopting complex package technologies is the insufficient understanding of 3D testing issues and the lack of DFT solutions. Testing of 3D packages has been limited due to lack of probe and test access for stacked wafers and dies, thermal concerns, design testability, test economics, and new defects mechanisms [15]. With 3D IC and heterogeneous integration, many of chip pins are obscured from the outside world, making direct curve tracing of chip pins practically impossible. Furthermore, observability, control, and accessibility of the individual IC signal pins become challenging, which poses challenges to EFI, as all EFI techniques require direct stimulation of the signal of interest (through test patterns). This requires special designs for FA and debug that would allow access to certain logical blocks of the chip/chiplet from the outside world.
- *Advanced Process Technology Node Scaling and Optical Resolution Challenges* To maximize the advantages of 3D IC and heterogeneous package configurations, it is imperative for ICs to employ the most advanced process technology nodes, hence subjecting 3D IC OFI to the same challenges for transistor scaling.
- *FA Workflow* FA workflow includes everything from the CAD infrastructure to device handling, and sample preparation. As HI introduces more chips into one package, it becomes a significant bottleneck to integrate all the design files (layout, schematic, technology) into one CAD database. Accessing a complex package database may result in long access times and latencies. Furthermore, as

die and package interconnects continue to scale down, repackaging techniques become almost impossible, as some of the package assemblies are done at the wafer foundry sites. Sample preparation techniques such as localized die milling, silicon thinning, and die extraction require extensive planning and development, as most HI packages include multiple components that are densely packed and could be at risk of getting damaged during the process.

(d) Complex Designs and Architectures

As system-on-chip (SoC) designs grow in complexity and integrate more functions onto a single IC, the need for more efficient testing becomes imperative, resulting in design for test (DFT) strategies that pivot toward test pattern compression. This results in complex DFT architectures that prevent direct stimulation of logic cells of interest, preventing conventional OFI techniques. Furthermore, the complexity of digital logic and introduction of compression hardware in DFT designs can result in less accurate and resolved diagnostics, making fault isolation more challenging.

Nowadays, it is no longer enough to know that a device fails through DFT. It is imperative that accurate diagnostics is required for an effective fault isolation. However, even diagnostic results at times fail to provide accurate fault isolation (due to equivalence and other factors). Hence, the need to develop better and more effective design for diagnostics (DFTD). Lastly, while it is good to be able to localize and isolate the failure, the next question that follows is "Why?". Hence, there is a need to enable designs for debug and FA. Collectively, this initiative is called DFTDD (design for test, diagnosis, and debug). Design for debug is also known as design for analysis (DFA).

Table 3 Spot size versus wavelength versus number of transistors

				# transistors (approximate)		
Wavelength	NA	Spot size	Application	4 nm	3 nm	2 nm
3000 nm	2.2	680 nm	Thermal	96	100	> 100
1800 nm	2.9	310 nm	PEM	20	21	22
1340 nm	3	220 nm	DLS/LVX	8	10	11
1065 nm	3.1	170 nm	DLS/LVX	6	8	9
785 nm	3.1	130 nm	DLS/LVX	4	5	4.5
577 nm	3.1	90 nm	DLS/LVX	2	4	4

Current State of the Art in Failure Analysis

Optical Fault Isolation Tools

Current optical fault isolation (OFI) techniques such as emission (PEM/Thermal) and laser-based (DLS/LVX) are not able to catch up with the continuous scaling of the transistors. To summarize, Table 3 shows the number of transistors that are covered by the wavelength of light used for each OFI technique.

Thermal imaging has the worst resolution due to the wavelength of light that it uses (3 to 5 μm) and the lower lens NA (approx. 2.2). This yields to about 680 nm spot size, based on Abbe's criterion. The region of influence covers about 100 + transistors in today's process technology node (2–3 nm). This means that thermal analysis will not be as effective in narrowing down to a specific transistor. Furthermore, as heat tends to spread, this often makes resolution of thermal imaging less accurate than laser or photon emission techniques.

Photon emission imaging at 1550 nm with an NA = 2.9 can yield as much as 267 μm spatial resolution. However, as the transsistor supply voltage continuously decreases to meet the low power needs, this results in a phenomenon called "red shift," where the wavelength of photon emissions is pushed to the higher IR range. Studies from [16] showed that the most optimal PEM signal-to-noise (SNR) ratio can be achieved by using shortpass (SP) filters at 1800 nm. Results using a 2000 nm filter showed higher PEM intensity but also elevated noise due to blackbody radiation, as the wavelength gets close to MWIR. This results in a lower SNR than that of an 1800 nm SP filter. Using 1800 nm wavelength as baseline, PEM spots may cover about 20 transistors in today's process nodes and hence, becomes a challenge in isolating the failure to a specific transistor. Furthermore, as the optical resolution depends on the wavelength and NA, this also means that it becomes difficult to resolve features when imaging. The same is true using laser-based techniques (DLS and LVX). However, recent developments have allowed for better resolution using visible light probing at 785 and 577 nm. While shorter wavelengths effectively improve spatial resolution, it also comes with its own set of challenges. As the wavelength shortens, the absorption of light increases, making it difficult to get laser signals back to the detector. To resolve this problem, the remaining backside silicon must be further thinned to ~ 1–5 μm, necessitating aggressive sample preparation techniques which sometimes result in device damage, especially if the die is big. Furthermore, the shorter laser wavelength has more energy and can inject more photocarriers that could eventually disrupt or alter the measurement due to the invasiveness of the laser. Hence, while VLP is currently available, most

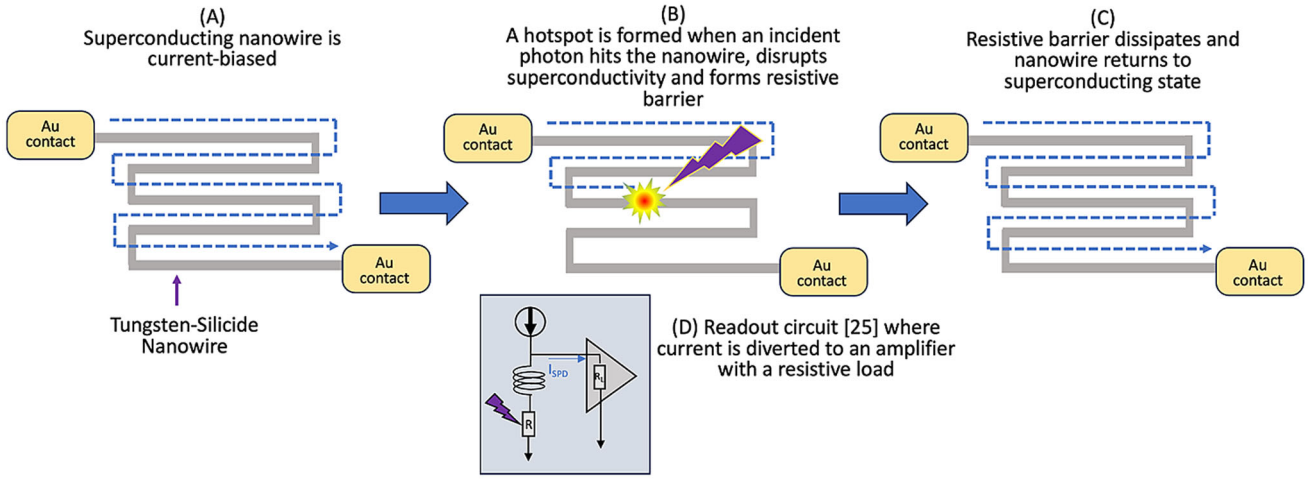


Fig. 9 Concept of superconducting nanowire single-photon detector

companies still defer back to 1064 nm probing which allows for 30–50 µm silicon RST.

Aside from optical resolution improvements, there were also recent tool developments aimed at improving OFI efficiency and effectiveness:

- *Superconducting Nanowire Single-Photon Detector (SNSPD)* [17–21]: Also known as superconducting single-photon detector, this new technology utilizes the highest-performing photon counting devices in the near-infrared spectrum (1.4–2.2 µm) with a high detection efficiency of 98% [17]. Figure 9 shows an illustration of an SNSPD. The SNSPD uses a 100 nm nanowire that is cooled below superconducting critical temperature. At this point, this wire will have zero resistance. Current drives this nanowire (Fig. 9A), which is in parallel with a detection circuit (Fig. 9D). When an incident photon is absorbed by the nanowire (Fig. 9B), some of the current is diverted toward the amplifier with a resistive load and creates a region of high resistance (hotspot). This resistance eventually dissipates and the nanowire is back to its superconducting state (Fig. 9C). This technology improves both spatial and temporal resolution of photon emissions (also known as time-resolved emissions, or TREM).
- *Digitizers in Laser Probing hardware* As transistors become densely packed, one of the biggest challenges of LVP is optical cross talk from neighboring transistors [22]. Furthermore, with the complexity of designs and the way devices are tested, functional test patterns become significantly long (> 10 ms), making LVP measurements challenging, if not impossible. The introduction of high speed digitizers, in addition to already existing oscilloscopes for LVP waveform measurement, allows for faster acquisition times. These digitizers offer improved trigger efficiency of 99.8% trigger capture, vs 77% trigger efficiency of existing oscilloscopes [23]. Furthermore, the introduction of digitizers eliminated the restrictions on the number of bins per waveform, which used to be limited to 1000 bins using an oscilloscope, therefore enabling high-resolution waveform capture for a longer period of time. This allows glitches to be detected even when using very long test patterns. Because of the fast acquisition rate, digitizers are utilized for optimization of laser probing, as it can provide real-time waveforms. As the bandwidth of the digitizer is lower than that of an oscilloscope, the best workflow to date is something that utilizes both digitizer and oscilloscope. First, the digitizer is used to scan long patterns for glitches or anomalies in the waveform. Once the anomaly is localized to a certain time stamp, the oscilloscope is used to capture the precise timing waveform at the specific period.
- *Lock-in Amplifiers for Improved LVI* One requirement of laser voltage imaging (LVI) is that for the LVI signal to be detected, the duty cycle should be completely periodic and close to 50%. The LVI signal at the fundamental frequency significantly drops once the duty cycle goes out of 50%. Hence, LVI is quite challenging to perform on pulse trains. This challenge is solved using laser voltage tracing (LVT). LVT utilizes lock-in amplifiers together with boxcar averaging to extend the capabilities of LVI beyond the limitations of spectrum analyzers and allow frequency mapping of aperiodic signals or pulse trains [24]. Lock-in amplifiers are known to extract weak signals from noisy backgrounds using phase-sensitive detection and low pass filtering. A diagram of a lock-in amplifier is shown in Fig. 10.

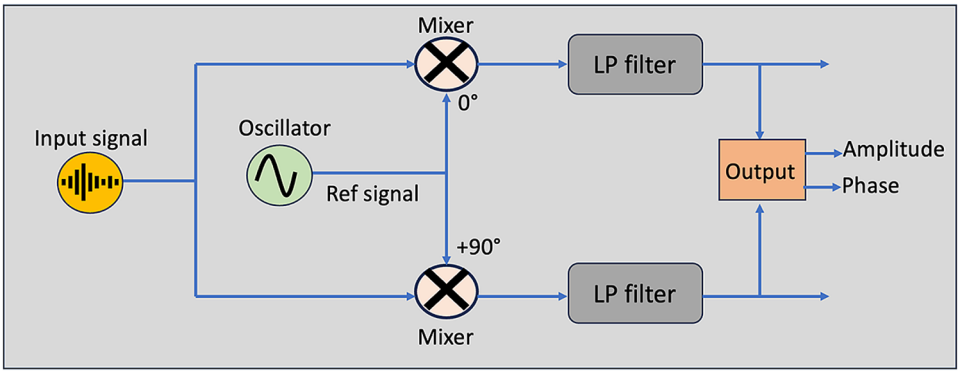


Fig. 10 Block diagram of a lock-in amplifier

- *Electron-Beam Probing (EBP) and Electron-Beam-Assisted Device Alteration (EADA)* The backside power delivery network (BPDN) is a new process technology scheme that aims to optimize power, performance, area, and cost (PPAC) by routing the power network below the transistors and the signals above the transistors, essentially blocking the optical path on both sides and rendering the OFI techniques obsolete, since light cannot penetrate opaque materials such as metals. To address this impending challenge, the electron-beam probe, which used to be a debug tool during the 90's, is being re-developed for BPDN applications. The EBP is based on the voltage contrast phenomenon. When an electron beam interacts with the sample, it produces secondary electrons that are detected by a through lens detector (TLD). Depending on the bias, the surface will turn dark or bright according to the potential of the surface [25–27]. Using a continuous electron-beam current, the maximum bandwidth of the system is only 5 MHz. To extend this further at higher frequencies, the e-beam is chopped using an electrostatic beam blanker to create a high speed e-beam pulse that synchronizes with the test pattern to achieve at least 2 GHz bandwidth at 500 eV [28]. Electron voltage probing (EVP) serves as the electron-beam equivalent of the LVP technique, while electron voltage imaging (EVI) is similar to LVI. The advantage of e-beam probing is that it provides superior spatial resolution compared to optical techniques (2 nm SEM resolution vs 150 nm VLP). It also allows detection of signals from metal lines, whereas LVP and VLP only allow measurements directly from the transistors. EADA is another electron-beam-based technique which is analogous to the DLS, except that it uses electron beams to stimulate a device [27]. The effectiveness of the EADA is illustrated in [27], where location of a failure on a high VMIN device was found on a PowerVia device. Furthermore, this study explored the e-beam interactions with NMOS and PMOS devices. It was found that the frequency tends to decrease during NMOS e-beam stimulation, while increasing during PMOS e-beam stimulation. While the results for e-beam-based analysis proves to be promising, this comes with significant challenges. This includes extensive efforts in developing a complex ATE and bench setup, self-heating issues (as the device is in vacuum), the time it takes to put the part in vacuum (since it uses the SEM), limited signal access (as most signals are buried in the layers), bandwidth limitation, and potential cross talk. The cost to develop such infrastructure is also high, costing more than $6 M. Sample preparation also needs meticulous planning and development efforts.
- *X-ray-Assisted Device Alteration* To address the OFI challenge on BPDN, the perturbation effects of x-rays have been explored in [29]. Research showed that while LADA creates a temporary stimulation through electron-hole pairs, XADA operates through total ionizing dose (TID) effects, which cause charging effects that shift the Vt of transistors.
- *Thermo-Reflectance*:Thermo-reflectance is a noncontact thermal analysis technique that measures the temperature fluctuations in a material by detecting changes in the reflectivity of the surface. This phenomenon was explored in the 2000 s and is now having a resurgence [30–34] due to the FA challenges of BPDN.

Package-Level Analysis

With the introduction of complex packages such as 3D IC and heterogeneous integration (HI), the conventional package inspection tools are also reaching the limit of their resolution. Table 4 shows the current state of the art for the most common FA tools and techniques used for 3D IC debug.

Table 4 Current state of the art for FA tools

Tool/technique	Current state of the art and developments		Limitations
Optical microscopy	Improved magnification (up to 6000X in digital microscopes) 0.9 to 0.95 NA, 0.5 um resolution		Limited spatial resolution
X-ray microscopy	~ 500 nm (40 nm voxel) [5, 59, 60] Use of AI for improved imaging and increased TPT [5, 59]		-Limited resolution (~500 nm, 40 nm voxel) -Form factor versus resolution (bigger boards, less resolution) -Throughput time (long scans over 5 h) -Volumetric inspection and automation
Confocal scanning acousting microscopy (CSAM)	-Axis precision (x, y, z) = .5 um [61, 62] − 300 MHz transducer: Detection limit = 1.67 umaxial resolution = 5.02 um [63] − 2 GHz transducer: Detection limit = 0.63 umaxial resolution = 0.6 um [63] -High speed gantry-Image processing software [5, 6] -High speed gantry-Image processing software [5, 6]		Imaging multiple stacked dies is difficult because signals often overlap (convolution), resulting to a tradeoff between scan depth reach and clarity of resulting image. [6]
Time domain reflectometry	Sub 5 um resolution, rise time < 6 ps [64] EOTPR workflow and CAD enhancements		-Complex package branching and interconnections-Modeling, simulation, and fault isolation of multiple nested-traces-Z-resolution challenged (locating the defect in a via stack, etc.)
Magnetic field imaging (MFI)	**Superconducting Quantum Interference Device (SQUID):** Sensitivity: 100 nA [65] WD: 100 um–10 mm [65–67] Resolution: 3 um [6, 67] Kept at vacuum and cryogenic tempPackage-level analysis	**Giant Magneto Resistor (GMR):** Sensitivity: 20 uA [65] WD: < 100 um (best at 5 um) [67, 68] Resolution: 250 nm [67, 68] Room temp, no vacuumWafer and die-level analysis	-SQUID has poor resolution. -GMR has better resolution but may not be enough for < 250 nm interconnects or features.
	Development of quantum diamond microscope which allows for wide FOV, high spatial resolution.		-Resolution is affected by the sensor size and standoff distance to the field source [6] -Sample prep may be needed (metal lines may need to be removed for better resolution), which results to semidestructive process.

Artificial Intelligence and Machine Learning for FA

Artificial intelligence (AI) is a general term used to describe a technology that uses computers and machines to make human-like decisions, predictions, and reasoning using a set of information (input data and target outcomes), sometimes called learning models. Machine learning is a subset of AI that utilizes algorithms that can identify patterns in the data to make accurate inferences about new data. Its ability to recognize patterns enables machine learning models to make decisions without explicit instructions [35]. A more focused subsection of ML is deep learning (DL), which is driven by neural networks, which are algorithms that mimic the brain structure, extracting complex patterns from huge datasets to enable advanced operations such as image recognition and natural language processing.

Since failure analysis involves a significant amount of data gathering through measurements and images, machine learning provides endless opportunities for advanced capabilities such as automatic defect detection, enhanced signal and image processing, shorter throughput times, optimized workflows, visualization [36], and organization of FA data for predictive analysis.

Below are some of the recent developments in failure analysis through machine learning:

- *FA Workflow Improvements, Data Mining, FA Classification, and Prediction* Ref [37] used natural language processing (NLP) algorithms such as k-nearest neighbors (kNN), support vector machines (SVM), and deep neural networks (DNN) to extract physical failures and electrical fault information and identify underlying patterns within different FA jobs to predict the root cause. Ref [38] utilized web ontology language (OWL) in standardizing machine-readable definitions for faults, which are methods and tools that can be later used for data processing. Having a standard terminology usage enables automated text classification, data mining, and workflow verification, essentially improving documentation consistency. One of the main challenges of performing data mining on FA reports is the lack of proper annotations and standardized data labels that could allow for machine learning. To build the FA software infrastructure, Ref [39] developed annotation services in the existing software. By integrating machine learning and ontologies, it creates machine-readable training data from heterogeneous data (such as images, labels, and texts). Lastly, various AI algorithms have been utilized to improve yield by optimizing the test program [40–42].
- *Image Resolution, Enhancement, and Image Capture TPT Improvements* Deep learning has been heavily utilized to reconstruct high-resolution images from low-resolution or low-dose scans, significantly improving data acquisition times.

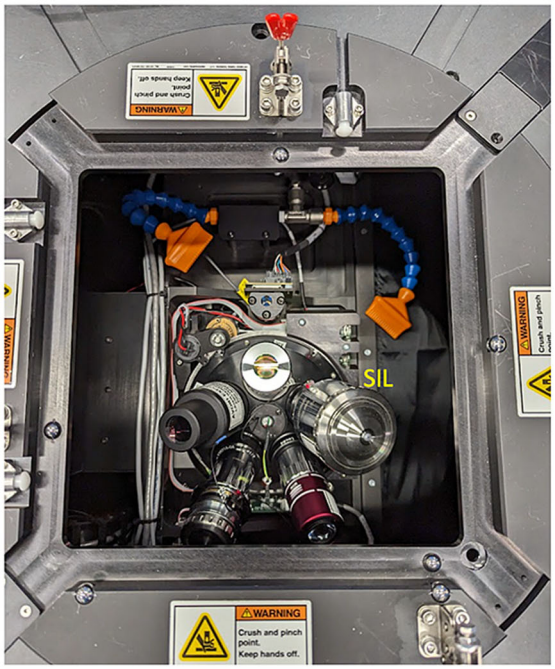
  3D x-ray Microscopy (XRM): Deep learning high-resolution reconstruction (DLHRR) algorithms are used to improve the resolution of 3D x-ray scans whsile reducing noise and cutting down scan times. This allows for more effective defect detection due to improved image quality and resolution, which is critical in the analysis of heterogeneous packages [43–46].

  Scanning Acoustic Microscopy (SAM): Ref [47] presented an AI-based image enhancement workflow to improve scanning acoustic microscopy (SAM) images using deep convolutional neural network (CNN) with skip connections and network in network (DCSCN) models on low-resolution images to improve the detectability of defects and optimize the scan times.

- *Defect Detectability Improvement and Automation* Several papers have utilized machine learning and CNN models such as random forest, U-Net, Mask R-CNN, and "You Only Look Once" (YOLO) for automated defect detection. These models are effective in image segmentation, tracing shapes, and boundaries for edge detection and image recognition. Such methodologies are useful for automated labeling [39], automated interconnect inspection of printer boards [48], automatic classification of pad defects [49], FIB-SEM 3D Tomography [50–52], nanoprobing tip-detection and automation [53], and STEM grain size analysis [54].

Design For Analysis (DFA)

One of the main challenges of failure analysis is that it has always been an afterthought when it comes to product design and development. ICs are increasingly becoming complex, preventing straightforward diagnosis and accessibility of critical internal signals for FA. The introduction of advanced process nodes and packaging technologies has pushed the current FA tools to the limit of resolution. Furthermore, with more functionalities integrated within a single IC, the test hardware becomes complex and populated with various electrical components which limit the accessibility of the solid immersion lenses (SIL) for higher resolution imaging. Since yield learning and ramp-up are highly dependent on resolving yield issues, finding the root cause of failures is paramount. Hence, it becomes imperative to consider the impact of designs to FA and



(A) Lens setup in EFI tool

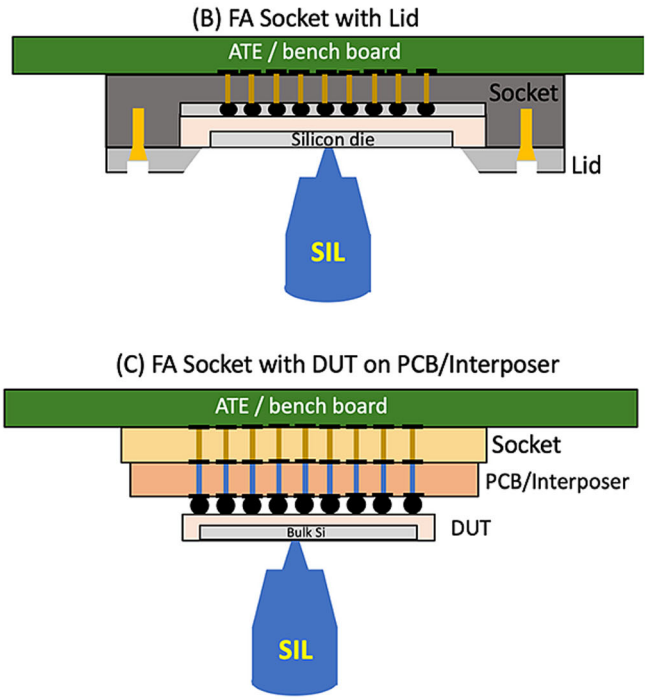


Fig. 11 (**A**) An image of a lens configuration within an OFI tool, (**B**) FA socket with open lid for SIL contact, (**C**) FA socket with PCB/interposer (also known as carrier or coupon board)

consciously develop features that would help improve FA workflows.

Design for Test, Diagnosis, and Debug

The adoption of 3D IC and heterogeneous integration has introduced technical and commercial testability challenges, where EDA tools and methodologies are challenged to support the latest package configurations into their design flows [14]. Advanced package designs require multi-physics, thermo-mechanical simulations to understand the interaction between different components. Sensors are becoming a utility, not only on the board, but on the package and the die, to allow for real-time measurements and a way to monitor different components from a complex package scheme.

Furthermore, as transistors continue to scale, conventional OFI tools are reaching the limit of optical resolution. Backside imaging of transistors becomes challenging and CAD-to-silicon alignment becomes a problem. Various solutions have been implemented on the IC to aid with CAD navigation. Prior work [55–57]. To improve the quality of chain diagnosis, a special hardware is added on the DFT infrastructure to enable shifting of data in both directions [58, 59].

Test Hardware Development

Test hardware design for bench application board and ATE load boards often overlook the FA requirements. Oftentimes, the FA engineers find themselves limited in EFI because of the keep out requirements for the lenses. Hence, it is very important to take into consideration certain FA requirements. The solid immersion lens (SIL) is an objective lens with a high refractive index used to increase the numerical aperture (NA) of the optical system to improve optical resolution. The SIL is typically placed in direct contact with the backside silicon to minimize the refractive index mismatch between the sample and surrounding medium (air), as a result improving the efficiency of light collection [4]. The contact area of the SIL tip ranges from $\sim$ .5 to $\sim$ 3 mm in diameter and is customizable. An image of a lens turret configuration with multiple air gap and SIL lenses is shown in Fig. 11A. To access the backside silicon using the SIL, specialized socketing hardware needs to be developed, as shown in Fig. 11B and C.

Electronic Design Automation (EDA) and Computer-Aided Design (CAD) Tool Developments

CAD tools are an essential part of EFI, as it integrates the chip design (layout and schematics) to enable precise

navigation during EFI and circuit analysis, after gathering EFI data. EDA tools, on the other hand, help integrate certain hardware designs that are essential for debugging and provide the capability to diagnose failures through automated ATPG diagnostics, memory bitmapping, and fault simulations.

Complex package technologies such as heterogeneous integration may involve multiple different components, and failure analysis of such systems-in-package (SIP) requires cross-collaboration between different suppliers, laboratories, assembly, and test factories. In such cases, sharing of sensitive IP information becomes a major concern, especially when it involves an external company. Failure analysis, specifically EFI, involves usage of design data such as layouts and schematic. Ref [60] illustrates an initiative by a CAD vendor, Synopsys, to enhance FA efficiency by integrating full heterogeneous systems into a single CAD navigation (CADNav) database that enables secure, industry-wide collaboration without exposing sensitive information. Ref [60] and [62] illustrate the versatile use of cross mapping and layout CAD functions of Avalon to visualize the different mask layers and perform a deep dive circuit analysis to find the root cause of failures. Furthermore, additional debug features of Synopsys Avalon CAD tool include an automated cone of logic tracing feature to find a relationship between two or more cells (also known as PathFinder). This feature allows the FA engineer to correlate different PEM spot locations and interpret the results. This is a more extensive version of the "hotspot analyzer," which checks for common signals between two or more hot spot locations [61]. The CAD tool can be also used to load FA data, such as image files from OFI tools and diagnostic data from yield and EDA tools. Lastly, Ref [63] and [64] discuss solutions using the Synopsys CAD tool, Avalon, for CAD alignment and navigation.

Lastly, the emergence of advanced DFT architectures has introduced challenges in observing and controlling internal signals, which is critical during EFI. To address this, EDA tool vendors such as Siemens have, for the first time, integrated dedicated hardware features into the DFT fabric to enable laser voltage probing and imaging (LVX) within the streaming scan network (SSN) architecture, a capability otherwise unavailable in its native mode [65]. Furthermore, by collaborating with the FA community to understand specific test stimulus requirements for EFA, Siemens has incorporated features that streamline FA test pattern generation workflows.

Conclusion

Today's advancements in design, process, and package technologies have been accelerating to a point where failure analysis (FA) could not catch up. As DTCO and STCO aim to address the growing challenges of power, performance, area, and cost (PPAC), it creates bottlenecks for performing FA, which slows down yield learning and ramp-up needed to meet the time-to-market. This paper presented the key drivers of FA challenges, namely transistor scaling, backside power delivery network, advanced packaging (3D IC and heterogeneous integration), and complex design architectures. The current state of the art in failure analysis was also presented, along with the gaps in each failure analysis discipline (microscopy, sample preparation, metrology, inspections, optical fault isolation, and physical FA). Design for test (DFT) is no longer sufficient; it is not enough to just screen failures. It is very important to identify the location of the failures through design for diagnosis (DFD). As the failure mechanisms become more complex, blurring the lines between process and design-related issues, design for diagnosis and debug (DFDD) becomes a necessity.

The key takeaway here is that we can no longer treat failure analysis as an afterthought and approach problem solving in a reactive manner. To keep up with the pace of more than Moore's law, the industry needs to adopt a "left-shift" in strategy. By integrating design for analysis (DFA) into the early stages of chip design and hardware development, we can develop "hooks" directly into the silicon, the hardware or even the EDA and CAD tools. Moving forward, achieving accelerated yield ramp-up is not just about design and hardware. It is about optimizing FA workflows and techniques using AI and machine learning. This paper has presented several developments in failure analysis using AI, which includes image enhancements, TPT improvements, and FA workflow optimizations. Predictive FA and digital twins will be key in addressing the growing challenges of FA and in transforming it from a reactive approach to a proactive discipline.

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References

1. L. Endrinal, S. Goh, "2D/2.5D/3D heterogeneous integration". Electronic device failure analysis technology roadmsap. ISBN electronic: 978-1-62708-462-8. November (2023)
2. H. -H. S. Lee, K. Chakrabarty, "Test challenges for 3D integrated circuits," in *IEEE Design & Test of Computers*, 26(5), 26-35, 2009, https://doi.org/10.1109/MDT.2009.125.
3. V. K. Ravikumar, "Understanding testing for dynamic fault isolation of microprocessors," *2016 IEEE 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Singapore, 2016, pp. 17-21, https://doi.org/10.1109/IPFA.2016.7564238
4. J D'Souza, "Reversible chain diagnosis", siemens EDA white paper
5. G. Ranganathan, V. -K. Ravikumar, A. Phoa and C. -W. Teo, "Timing analysis case studies using 1064 nm continuous wave laser for fault isolation on scan failures," *2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits*, Hsinchu, Taiwan, 2015, pp. 13-16, https://doi.org/10.1109/IPFA.2015.7224320
6. Die-level roadmap council–isolation committee technical summary. EDFAS FA technology roadmap. November (2022)
7. Electron device failure analysis roadmap: https://dl.asminternational.org/handbooks/monograph/193/Electronic-Device-Failure-Analysis-Technology
8. V.K. Ravikumar et al., "Short wavelength probing for fault isolation applications". in 108–115 (2020). https://doi.org/10.31399/asm.cp
9. V. Somasundaram, S. Y. Xuan, A. Phoa, W. Lua, C. C. Meng and V. Krishnan Ravikumar, "Characterization of 1122 nm Laser for Laser Based Fault Isolation Applications," *2019 IEEE 26th International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA)*, Hangzhou, China, 2019
10. A. Chigurupati, N. Lassar, "Root cause analysis using artificial intelligence," *2017 Annual Reliability and Maintainability Symposium (RAMS)*, Orlando, FL, USA, 2017, pp. 1-5, https://doi.org/10.1109/RAM.2017.7889651
11. Li, Y., Goyal, D. (2021). Fault isolation and failure analysis of 3D packaging. 3D microelectronic packaging
12. Y. Cai, Z. Wang, R. Dias and D. Goyal, "Electro optical terahertz pulse reflectometry—an innovative fault isolation tool," *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2010, pp. 1309-1315, https://doi.org/10.1109/ECTC.2010.5490646
13. https://teraview.com/semiconductor/
14. J. Alton, M. Igarashi, "Non-destructive fault localization in advanced IC packages using electro optical terahertz pulse reflectometry," *2013 Eurpoean Microelectronics Packaging Conference (EMPC)*, Grenoble, France, 2013, pp. 1-4
15. L. Endrinal et al., Solving complex electrical fault isolation challenges with innovative DFT strategies. J. Fail. Anal. Prev. **25**, 1986–2007 (2025). https://doi.org/10.1007/s11668-025-02276-7
16. A.B. Shehata, F. Stellari, A. Weger, P. Song, H. Deslandes, T. Lundquist, E. Ramsay, " Novel NIR camera with extended sensitivity and low noise for photon emission microscopy of VLSI circuits", 2014 International Symposium for Testing and Failure Analysis, Houston, Texas
17. R. Chowdhury, et al. "CMOS integrated circuit analysis using superconducting nanowire single-photon detectors". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference* October 28–November 1, 2024, San Diego, California, USA
18. https://www.nist.gov/noac/technology/quantum-optics-and-radiometry/superconductive-nanowire-single-photon-detectors
19. C. Boit, "Photonic localization techniques", international symposium for testing and failure analysis tutorial (2022)
20. C.M. Natarajan et al., "Superconducting nanowire single-photon detectors: physics and applications." Supercond. Sci. Technol. **25**, 063001 (2012)
21. L. You, Superconducting nanowire single-photon detectors for quantum information. Nanophotonics. **9**(9), 2673–2692 (2020). https://doi.org/10.1515/nanoph-2020-0186
22. L. Endrinal, R. Kinger, L. Ranganathan, A. Sheth, "Solving critical issues in 10 nm technology using innovative laser-based fault isolation and DFT diagnosis techniques," 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 2018, pp. 6B.1-1-6B.1-5, https://doi.org/10.1109/IRPS.2018.8353622
23. W. Lua, V.K. Ravikumar, A. Phoa. "Fast laser probing using gigahertz digitizer". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference* October 28–November 1, 2024, San Diego, California, USA
24. S. Lee, K. Dickson. "Lock-in amplifier applications for fault isolation". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference* October 28–November 1, 2024, San Diego, California, USA
25. N. Leslie, J. Vickers, B. Freeman, S. Samani, P. Sabbineni, P. Vedagarbha, "2GHz Contactless Electron Beam Probing", 2022 International Symposium for Testing and Failure Analysis, Pasadena, California
26. N. Leslie, J. Vickers. "Electrical event capture with an electron beam probing system". In *ISTFA 2023: Proceedings of the 49th International Symposium for Testing and Failure Analysis Conference* November 12—16, 2023, Phoenix, Arizona, USA
27. J. Huening, et al. "E-beam probing and E-beam-assisted device alteration (EADA) for fault isolation in powervia and advanced technology nodes". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference* October 28–November 1, 2024, San Diego, California, USA
28. J. Vickers, S. Somani, B. Freeman, P. Carleson, L. Tuma, M. Uncovsky, P. Hlavenka, "Failure analysis of FinFET circuitry at GHz speeds using voltage-contrast and stroboscopic techniques on a scanning electron microscope", 2019 International Symposium for Testing and Failure Analysis, Portland, Oregon
29. L. Endrinal, "A practical tutorial on ATE-based electrical fault isolation of digital SoCs using photon emission and laser voltage imaging/probing". International Symposium for Testing and Failure Analysis Tutorial 2023
30. W. Lo, et. al. "Device alteration using a scanning x-ray microscope". In *ISTFA 2022: Conference Proceedings from the 48th International Symposium for Testing and Failure Analysis*. Pasedena, California, USA
31. S. Tominaga, et. al. "Application to a failure analysis of Visible ThermoDynamic ® Imaging". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference*
32. M. Senger, et. al "Comprehensive fault isolation technologies for the gate-all-around transistor and backside power delivery paradigm shifts". In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference*. Pasadena, California.
33. M.G. Jeong, et. al. "High-spatial-resolution thermoreflectance microscope using shear force microscopy". In 2025 International Symposium for Testing and Failure Analysis Conference. Pasadena, California
34. C.B. Jeong, et. al. "Thermoreflectance microscopy for the steady-state and transient thermal analysis of semiconductor devices".

2025 International Symposium for Testing and Failure Analysis.Pasadena, California
35. D. Bergmann. "What is machine learning?". https://www.ibm.com/think/topics/machine-learning
36. S. Suthar, L. Goh. "AI application in yield and failure analysis to reduce overall time-to-defect and failure root-cause isolation". In *ISTFA™ 2022: Conference Proceedings from the 48th International Symposium for Testing and Failure Analysis* October 30–November 3, 2022 Pasadena Convention Center, Pasadena, California, USA
37. F. Platter, et al. "Report classification for semiconductor failure analysis". In *ISTFA 2021: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference*. Phoenix, Arizona
38. A. Safont-Andreu, et. al "Using Ontologies in Failure Analysis", In *ISTFA 2021: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference*. Phoenix, Arizona.
39. N. Matha, et al. "Automated labeling infrastructure for failure analysis". In *ISTFA 2022: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference*. Pasadena, California.
40. D. Valet, J. Gaudestad, C. Richardson "High-resolution backside GMR magnetic current imaging on a contour-milled globally ultrathin die". International Symposium for Testing and Failure Analysis Tutorial 2014.
41. J. Kim, et. al. "Machine learning-based optimization technique for high-capacity V-NAND flash memory". *In ISTFA 2021: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference* October 31— November 4, 2021 Phoenix Convention Center, Phoenix, Arizona, USA
42. Y. Chan, S. Goh. "Genetic algorithm-based digital test optimization method and its application to yield improvement". In *ISTFA 2021: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference* October 31—November 4, 2021 Phoenix Convention Center, Phoenix, Arizona, USA.
43. A. Gu, M. Terada, H. Stegmann, T. Rodgers, C. Fu, Y. Yang, "From system to package to interconnect: an artificial intelligence powered 3D x-ray imaging solution for semiconductor package structural analysis and correlative microscopic failure analysis," *2022 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Singapore.
44. A. Gu, et al. "Accelerate your 3D x-ray failure analysis by deep learning high resolution reconstruction". In *ISTFA 2021: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference*. Phoenix, Arizona.
45. S. Mohammad-Zulkifli, et. al. "An artificial intelligence powered resolution recovery technique and workflow to accelerate package level failure analysis with 3D x-ray microscopy". In *ISTFA 2023: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference*. Phoenix, Arizona.
46. H. Villarraga-Gómez, et. al. "Assessing electronics with advanced 3D x-ray microscopy techniques and electron microscopy". In *ISTFA 2023: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference*. Phoenix, Arizona.
47. R. Wilhelmer, et. al. "AI-based image enhancement improves detection of white bump defects". In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference*. Pasadena, California.
48. P. Craig, et. al "Optical automated interconnect inspection of printed circuit boards". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference* October 28–November 1, San Diego, 2024, California,
49. D. Utess, et. al. "AI-based image segmentation for the characterization of bond pads after SLAT".In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference* November 16–20, 2025, Pasadena, California, USA
50. H. Stegmann, F. Cognini. "Few-shot AI segmentation of semiconductor device FIB-SEM tomography data".In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference*, October 28–November 1, 2024, San Diego, California
51. P. Limbecker, et. al. "A step towards automation in failure analysis by FIB-SEM 3D tomography and AI segmentation." In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference November*, 16–20, 2025, Pasadena, California,
52. D. Mello. "Advanced method for 3D FIB tomography AI supported on SRAM I/O circuit block with missing data bits problems". In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference*, November 16–20, 2025, Pasadena, California, USA
53. D. Kleindiek, et. al. "Enhancing semiconductor nanoprobing procedures with AI-Driven Tip Detection". In *ISTFA 2024: Proceedings from the 50th International Symposium for Testing and Failure Analysis Conference*, October 28–November 1, 2024, San Diego, California, USA
54. C. Li, et. al. "Grain size analysis by differential phase contrast (DPC)- scanning transmission electron microscopy (STEM) and artificial intelligence (AI) segmentation". In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference* November 16–20, 2025, Pasadena, California, USA
55. R. Schlangen. "CAD alignment methodologies for accurate and reliable optical fault isolation at sub-5 nm process technologies". In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference* November 16–20, 2025, Pasadena, California
56. R. Salem, L. Endrinal, H. Bunnalim, H. Lim, L. Ranganathan, M. Malabry. "Visible alignment markers/landmarks for CAD-to-silicon backside image alignment". US Patent 10,605,859. Mar 2020
57. M. Alston, L. Endrinal, H. Bunnalim, M. Malabry, L. Ranganathan, R. Salem. "Visible alignment markers/landmarks for CAD-to-silicon backside image alignment". US Patent 10,262,950. Apr 2019
58. L. Endrinal, R. Kinger, J. Fang, S. Patil, L. Ranganathan. "Laser-based Integrated Circuit Testing Techniques". US Patent 10,324,131. June 2019
59. W. Tung Cheng, Y. Huang. "Bidirectional scan cells for single-path reversible scan chains". US Patent 11,408,938. Aug 2022
60. R. Gopinath, et. al."Enhanced CAD alignment techniques for FinFET devices". In *ISTFA™ 2022: Conference Proceedings from the 48th International Symposium for Testing and Failure Analysis* October 30–November 3, 2022 Pasadena Convention Center, Pasadena, California,
61. J.M. De Jesus, et. al. "Failure localization technique for metal and transistor defects through avalon CAD navigation and focused ion beam circuit edit". In *ISTFA 2023: Proceedings of the 49th International Symposium for Testing and Failure Analysis Conference* November 12—16, 2023, Phoenix, Arizona
62. A. Evangelista, et. al. "Avalon-aided mapping of fault-localized area of ADI's RADAR receive path analog front-end (AFE) amplifier with 0.18 μm 6-Metal CMOS Fab Process". In *ISTFA 2023: Proceedings of the 49th International Symposium for Testing and Failure Analysis Conference* November 12—16, 2023, Phoenix, Arizona

63. A. Bhattacherjee, et. al. “Heterogeneous industry collaboration and system CAD navigation for advanced package failure analysis”. In *ISTFA 2021: Proceedings from the 47th International Symposium for Testing and Failure Analysis Conference* October 31— November 4, 2021 Phoenix Convention Center, Phoenix, Arizona,
64. A. Bhattacherjee, J. Liao.”Hyper-integrated CAD database for one-shot EOTPR fault localization in heterogeneous SiP-on-board assemblies”. In *ISTFA 2025: Proceedings from the 51st International Symposium for Testing and Failure Analysis Conference* November 16–20, 2025, Pasadena, California
65. N. Chinone, et. al. “High resolution thermal imaging of Si device by near-infrared thermoreflectance and separation of thermal/electro-optical mixed signals by means of bias dependency”. 2025 International Symposium for Testing and Failure Analysis.Pasadena, California
66. MAPT 2.0 Roadmap. “Manufacturing and process development metrology”. https://srcmapt.org/chapter10/
67. E.P. DeBenedictis, M. Badaroglu, A. Chen, T.M. Conte, P. Gargini, Sustaining Moore’s law with 3D chips. Computer. **50**(8), 69–73 (2017). https://doi.org/10.1109/MC.2017.3001236
68. https://www.tecreps.com/images/pdfs/Specification-Sheet-Gen7-G7001.pdf
69. Sonoscan D9600 specification. https://www.cohpros.com/Total%20file/561-D9600.pdf
70. PVA TePla analytical systems https://www.pvatepla-sam.com/en/products/transducer/#:~:text=High%2DResolution%20Transducers%20up%20to,be%20achieved%20on%20suitable%20samples.
71. EOTPR 4500 https://www.acesolution.com.tw/en/products/product_TeraView_EOTPR4500.html#:~:text=The%20EOTPR%204500%20system%20couples,generation%20in%20automated%20probe%20stations
72. A, Orozco, Y. Kaneko “Current imaging using SQUID and GMR sensors for failure analysis”.https://neoceramagma.com/wp-content/uploads/2017-nanots_kaneko-orozco.pdf
73. Neocera magma https://neoceramagma.com/semiconductor-failure-analysis-tools/semiconductor-failure-analysis-capabilities/
74. S. H. Lau *et al*., “Decoupling Sub-micron Resolution and Speed from Sample Size in 3D X-ray Imaging,” *2022 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Singapore, Singapore, 2022, pp. 1-6, https://doi.org/10.1109/IPFA55383.2022.9915760.
75. N. Gaudestad, V. V. Gagliolo, R. H. Talanov, Yeh, C. J. Ma, “High resolution magnetic current imaging for die level short localization,” *Proceedings of the 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Suzhou, China, 2013, pp. 347-350, https://doi.org/10.1109/IPFA.2013.6599179.
76. ”Scaling CMOS beyond FinFETs: from nanosheets and forksheets to CFETs,” https://www.imec-int.com/en/imec-magazine/imec-magazine-december-2019/scaling-cmos-beyond-finfets-from-nanosheets-and-forksheets-to-cfets.
77. J. Gaudestad. “Magnetic field imaging for non-destructive 3D package fault isolation”. In *IMAPS 2014 Proceedings*. Oct 13-16, 2015. ISBN: 978-0-9909028-0-5

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