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DOI
10.1109/TED.2022.3233816

Publication date
2023

Document Version
Final published version

Published in
IEEE Transactions on Electron Devices

Investigation of Unclamped Inductive Switch Characteristics in 4H-SiC MOSFETs With Different Cell Topologies

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***Abstract*— To investigate the unclamped inductive switch (UIS) characteristics, 1200 V silicon carbide (SiC) planar MOSFETs with four cell topologies of linear, current sharing linear, square, and hexagon are designed and manufactured. The experimental platform was built and tested. The results show that the single pulse avalanche energy density of the linear cell topology is 1.69 times higher than that of the square and 1.49 times that of the hexagon. Further, the UIS process is simulated by using physical simulation, which shows that the avalanche energy was concentrated near the corner of the P-base region in the UIS mode. From this, the avalanche energy distribution differences of the four cell topologies were analyzed and compared. A theoretical model of avalanche heating per unit area is proposed, which shows that the avalanche energy density is inversely proportional to the proportion of avalanche energy concentration region. This study may contribute to the cell topology design of SiC MOSFETs under the application scenario with high avalanche reliability requirements.**

***Index Terms*— Avalanche, cell topologies, failure analysis, silicon carbide (SiC) planar MOSFET, unclamped inductive switch (UIS) test.**

I. Introduction

SILICON carbide (SiC) MOSFETs are gradually replacing silicon-based insulated gate bipolar transistors (IGBTs) in medium and high voltage applications due to their fast switching speed, low power dissipation, and high operating temperature [1], [2]. With the expansion of the application field of SiC power devices, the complex and changeable application scenarios have put forward more requirements on the stability and reliability of SiC MOSFETs.

In the fields of uninterruptible power supply, hybrid electric vehicles, photovoltaic inverters, etc., inductive loads are widely used in the system. During the switching process, in the absence of clamping diodes, the energy stored in the inductors is released through the power devices, which will cause the devices to operate under high-voltage and high-current conditions, resulting in avalanche breakdown, which greatly increases the probability of device failure [3]. Therefore, the avalanche capability of devices is an important index to evaluate the reliability of SiC MOSFETs, which is usually evaluated by the unclamped inductive switch (UIS) test.

In order to explore the UIS characteristics and failure mechanism of SiC MOSFET, many research works have been carried out [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17]. Several studies have shown that in the UIS process when the temperature of the source aluminum layer exceeds the melting point, UIS failure occurs [4], [5], [6]. The parameter degradation and failure mechanism of SiC MOSFET under repetitive avalanche stress were studied in detail [7], [8], [9], [10], [11]. Further, the avalanche reliability of SiC MOSFETs is related to the internal cell structure and parameter. In terms of device types, the UIS characteristics of the asymmetric trench and double trench SiC MOSFETs were compared and analyzed [12], [13], [14], [15]. The results show that the failure of the asymmetric trench structure is due to the thermal failure of the metal layer, while the failure of the double trench structure is due to the high electric field of the gate oxide layer. In addition, in terms of structural parameters, Bai et al. [16] and Zhu et al. [17] simulated the influence of cell structure parameter deviation on UIS characteristics. In addition to structural parameters, cell topology is also very important in device design. Previous studies have evaluated the static characteristics and high-frequency performance of SiC MOSFETs with different cell topologies [18], [19], [20], but there is no relevant detailed research on the effects of different cell topologies on the UIS characteristics.

In this article, four cell topologies of linear, current sharing linear, square, and hexagonal in SiC MOSFETs are designed

Manuscript received 3 December 2022; revised 26 December 2022; accepted 29 December 2022. Date of publication 6 January 2023; date of current version 24 February 2023. This work was supported in part by the General Fund for Pre-Research of Military Program under Grant 61404140404, in part by the General Program of National Natural Science Foundation of China under Grant 62071073, in part by the Frontier Innovation Program (National Defense Science and Technology Innovation Special Zone) under Grant 19-163-00-KX-002-024-01, in part by the Key Laboratory Open Fund under Grant GD20201, and in part by the Chongqing Municipal Technology Innovation and Application Development Program (Military-Civilian Integration) under Grant JG2021083. The review of this article was arranged by Editor T. Kimoto. *(Huan Wu and Houcai Luo contributed equally to this work.) (Corresponding author: Xianping Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3233816.

Digital Object Identifier 10.1109/TED.2022.3233816

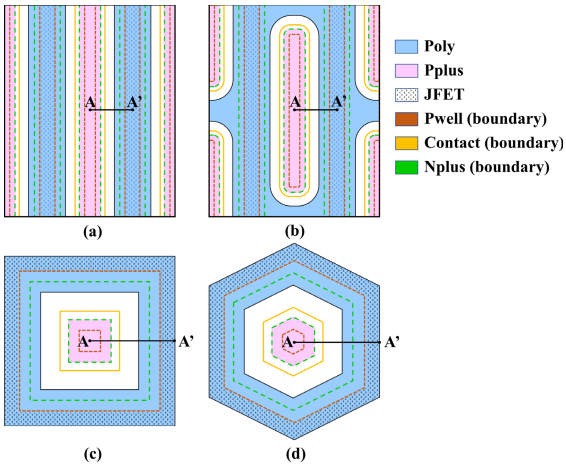

Fig. 1. Four cell topologies for fabricated 1200 V 4H-SiC MOSFETs. (a) Linear_1. (b) Linear_2. (c) Square. (d) Hexagon.

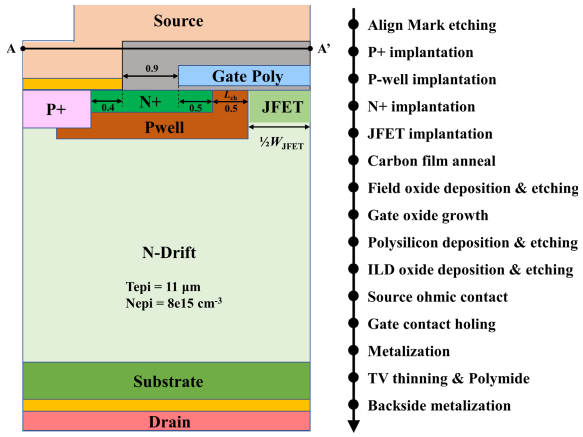

Fig. 2. MOSFET cell cross section at A–A′ and the fabrication process flow for all cell topologies.

and manufactured under the standard SiC MOSFET self-aligned process platform. The UIS characteristics of different devices are tested and studied. Further, by using the mixed mode simulation, the UIS process is simulated and analyzed. A theoretical model is proposed to explain the test results.

II. Device Fabrication and Test Platform

At present, the main cell topologies of commercial SiC MOSFETs can be divided into three types: linear, square, and hexagonal [18], [19], [20]. The linear can be divided into the common linear and the current sharing linear. The adjacent polysilicon gates of common linear topology are not interconnected as the square and the hexagonal. Especially in MOSFETs with large chip sizes, long linear polysilicon gate bars only converge at the edge, which will lead to unbalanced gate current transmission, delayed opening of channels near the middle position, and affect the switching characteristics. The current-sharing linear topology improves the balance of the gate current and optimizes the switching characteristics through alternating connections between adjacent gates. The four cell topologies are shown in Fig. 1, in which Linear_1 is a common linear topology and Linear_2 is a current sharing linear topology.

Fig. 2 shows the cell cross-sectional structure diagram at A–A′ in Fig. 1 and the self-aligned manufacturing process flow of 1200 V SiC MOSFETs. These SiC MOSFETs are made in 6-in SiC FAB with an epitaxial layer thickness of 11 μm and a concentration of 8e15 cm^{-3}. First, the ion implantation is carried out in the P+ source region and P-base region. Based on the self-aligned process, 0.5 μm spacers are grown on polysilicon, and then N+ source ion implantation is performed. The JFET region is formed by full implantation of the active region, with a width ranging from 1.2 to 2.0 μm. Then, after depositing a layer of carbon film, the implanted ions are annealed and activated at 1700 °C for 30 min. A 50 nm gate oxide layer is grown on which polysilicon gates are deposited and etched. An insulating layer with a thickness of 0.9 μm is formed between the gate and the source. Then the aluminum layer is deposited and etched to complete

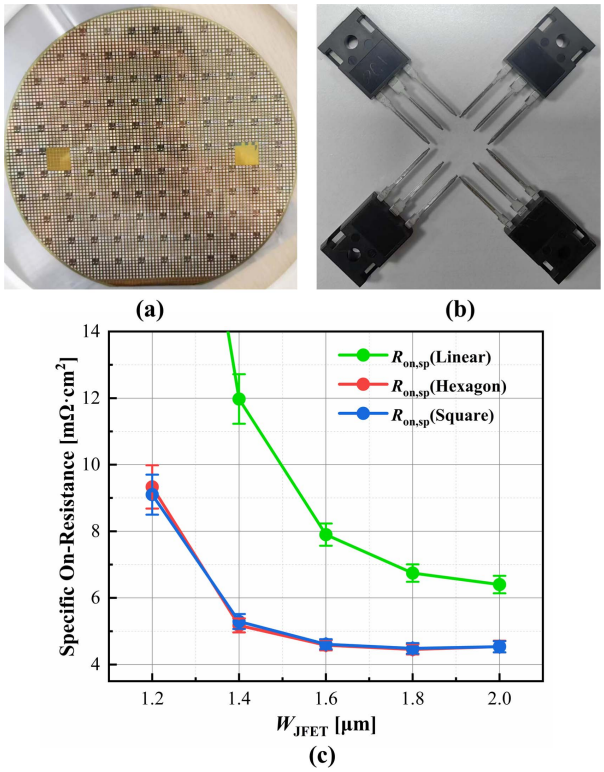

Fig. 3. (a) 1200 V SiC MOSFET wafer. (b) TO-247 packaged devices. (c) Specific ON-resistance of SiC MOSFETs with different cell topologies and different W_{JFET}.

the metallization of the front source and gate. Finally, the metallization of the drain on the back of the chip is completed. Except for different cell topologies, the four SiC MOSFETs all use the same manufacturing process and parameters and have the same die size.

The finished wafer photo is shown in Fig. 3(a), and TO-247 packaging is completed in the standard SiC device packaging factory, as shown in Fig. 3(b). The specific ON-resistance $R_{ON,sp}$ of linear, square, and hexagonal cells is shown in Fig. 3(c). It can be seen that the square and the hexagonal have similar $R_{ON,sp}$ and are both lower than the linear cell topology.

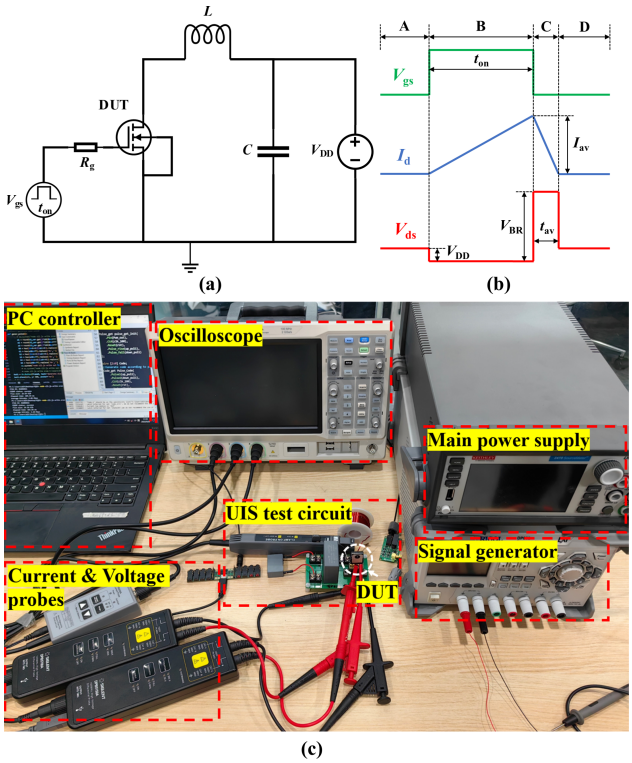

Fig. 4. (a) Schematic of UIS test circuit. (b) Ideal UIS test process. (c) Physical diagram of test platform.

This is because square and hexagonal cell topologies have the same channel density, which is higher than that of linear. This also shows that square and hexagonal cell topology devices have better static characteristics. When the width of the JFET region (W_{JFET}) is less than 1.6 μm, the $R_{ON,sp}$ of the device shows a decreasing trend with the increase of the width of the JFET region. This is because when the W_{JFET} is small, the decrease in the resistance of the JFET region brought about by increasing the W_{JFET} is more dominant than the increase in the cell pitch. However, the $R_{ON,sp}$ of the square and hexagonal cell topologies no longer decrease when the width of the JFET region is greater than 1.6 μm because the increase of the cell pitch caused by the increase of the W_{JFET} gradually surpasses the effect of the decrease of the resistance of the JFET region.

The schematic of the UIS test circuit is shown in Fig. 4(a). The device under test (DUT) is connected in series with the inductor, and the capacitor is connected in parallel with the dc power supply V_{DD}. Fig. 4(b) shows the UIS test process, which can be divided into four phases. In phase A, the DUT is not turned on, and the drain to source voltage V_{ds} keeps the dc voltage V_{DD} unchanged. In phase B, the gate drive voltage V_{gs} is switched to a high level, the DUT enters the ON state, V_{ds} drops to 0, and the drain current I_d gradually rises to the required avalanche current value I_{av}. I_{av} can be adjusted by changing the V_{gs} high level time. During phase C, V_{gs} switches to negative voltage and DUT is turned off and enters avalanche operation mode. V_{ds} increases rapidly to the breakdown voltage V_{BR}. Due to the existence of the inductor, the avalanche current drops slowly, and the energy stored in the inductor is released slowly through the DUT. The energy stored in the inductor is released in the form of heat in the avalanche process, forming an instantaneous high temperature inside the device. During phase C, DUT operates under high voltage and high current. The single pulse avalanche energy E_{as} of DUT is obtained by integrating avalanche voltage and avalanche current during phase C, as follows:

$$E_{as} = \int V_{ds} \cdot I_{ds} dt. \tag{1}$$

When E_{as} is small, I_{av} drops to 0, and the DUT turns off normally. However, when E_{as} is too large, the high temperature generated by E_{as} exceeds the tolerance limit of DUT. The I_{av} decreases first, then rises rapidly, causing irreversible avalanche failure.

The UIS test platform is shown in Fig. 4(c), where the DUTs are SiC MOSFETs with four different cell topologies. In the UIS test circuit, the dc power supply V_{DD} is 200 V, the 0.5 mH inductor is used to charge the avalanche energy, and the gate voltage V_{gs} is a single pulse signal of −5/15 V. The main power supply provides stable dc voltage V_{DD} and the signal generator cooperates with the PC controller to generate the gate drive signal. Current and voltage probes are used to accurately measure the real-time current and voltage values of key nodes. During UIS testing, the charging time t_{ON} for each V_{gs} pulse was extended by 2 μs until the DUT had an irreversible avalanche failure. In order to facilitate the comparison of UIS characteristics of DUTs with different cell topologies, the maximum tolerable UIS energy density E_{ava} is used as the comparison value. E_{ava} is the ratio of single pulse avalanche energy to the active area of the chip, as follows:

$$E_{ava} = \frac{E_{as}}{S_{act}} \tag{2}$$

where E_{as} is the single pulse avalanche energy, given by (1), and S_{act} is the active area of the chip.

III. Results and Discussion

Four cell topology devices with $W_{JFET} = 1.4$ μm were selected, and UIS tests were performed under the same test conditions. Fig. 5 shows the measured UIS waveforms of four cell topologies SiC MOSFETs, just before the single pulse avalanche failure and when the failure occurred. The key test data are shown in Table I.

As shown in Fig. 5, the avalanche energy densities E_{ava} of SiC MOSFETs with common linear, current sharing linear, square, and hexagonal cell topologies are 4.699, 4.493, 2.773, and 3.164 J/cm^2. Comparing the E_{ava} of the four cell topologies, it can be found that the E_{ava} of the two linear cell topologies is significantly better than the square and hexagonal cell topologies. There is only a slight difference in E_{ava} corresponding to the traditional linear and the current sharing linear cell topology. The E_{ava} of the Linear_1 is about 1.69 times that of the square and 1.49 times that of the hexagon. Similar results were obtained from UIS tests on several samples. It can be seen that although the specific ON-resistance of square and hexagonal cell topology SiC MOSFET is lower than that of the linear cell, the linear cell topology is superior to square and hexagonal cell topology in terms of avalanche reliability.

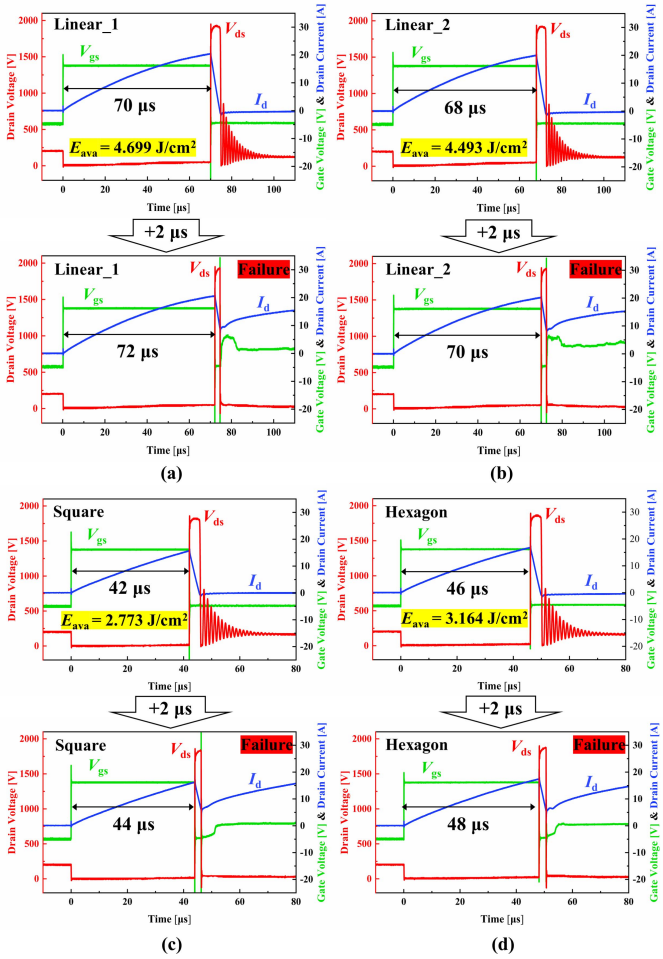

Fig. 5. Measured UIS waveforms of four cell topologies SiC MOSFETs, just before failure and when failure occurred. (a) Linear_1. (b) Linear_2. (c) Square. (d) Hexagon.

TABLE I
DATA FROM UIS TEST OF DEVICES WITH FOUR CELL TOPOLOGIES

	Linear_1	Linear_2	Square	Hexagon
$R_{ds(on)}$ [mΩ]	692.17	690.56	305.17	298.40
$R_{on,sp}$ [mΩ·cm²]	12.002	11.974	5.292	5.174
t_{on} [µs]	70	68	42	46
V_{BR} [V]	1925	1917	1825	1858
I_{av} [A]	20.83	20.17	16.17	17.46
t_{av} [µs]	4.95	4.85	4.11	4.23
E_{as} [mJ]	81.48	77.91	48.08	54.86
S_{act} [cm²]	0.01734	0.01734	0.01734	0.01734
E_{ava} [J/cm²]	4.699	4.493	2.773	3.164

* $R_{ds(on)}$ @ V_{gs} = 20 V, I_{DS} = 5 A;
* E_{ava} @ V_{DD} = 200 V, L = 0.5 mH

Therefore, it is necessary to decide which cell topology to use according to the reliability requirements of specific application scenarios.

The four DUTs with UIS test failure are tested, respectively, which shows that the gate–source and drain are short-circuited to each other. In order to study the reason for the

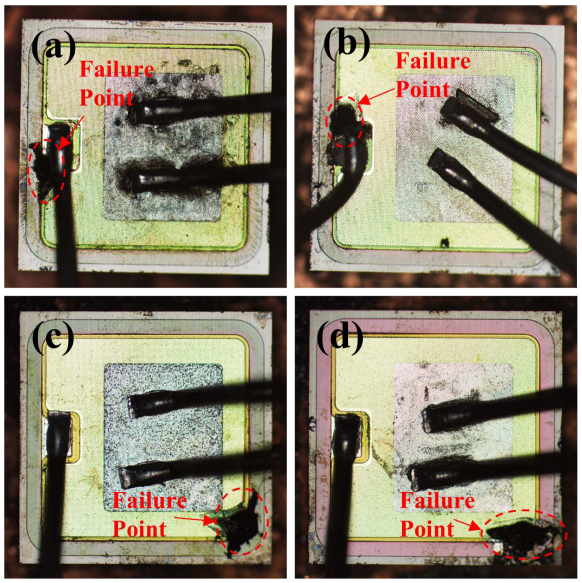

Fig. 6. Top view of decapsulated DUTs after the failure of UIS test. (a) Linear_1. (b) Linear_2. (c) Square. (d) Hexagon.

above results, the four DUTs that failed in the UIS test were decapsulated, as shown in Fig. 6. Clear burn-out failure points can be observed in the active regions of the four failed DUTs, indicating that the failure is caused by thermal runaway rather than gate oxide breakdown. In addition, the thermal failure point of the two linear is close to the gate pad, while the thermal failure point of the square and hexagonal is close to the corner of the terminal. Similar results were obtained in repeated comparative experiments. The specific location of the avalanche burn point seems to be related to the chip manufacturing process and layout design. Here, a possible explanation is given for the differences in layout. Because square and hexagonal topologies have smaller cell sizes than linear cells, the square and the hexagonal have higher cell density at the corners of chips with the same active region radius. The avalanche energy is generated in the active region and gradually transfers heat to the entire chip. However, the terminal region and the gate pad region do not generate avalanche energy. After the device enters the avalanche mode, the corner temperature rises rapidly, and there is a large temperature difference with the terminal, resulting in thermal burning. However, the linear cells have many gate bars around the gate pad region. Therefore, after the device enters the avalanche mode, the temperature of the active region around the gate pad region rises rapidly, which forms a large temperature difference with the gate pad, where thermal burns occur.

In order to further analyze the reasons for the difference in E_{ava} of SiC MOSFETs with different cell topologies, the UIS characteristics of the devices were simulated and analyzed by using the 2-D technology computer-aided design (TCAD) physical simulation. As shown in Fig. 7(a), the half-cell SiC MOSFET is established, and the structure size and doping distribution of the simulated cell are basically consistent with the real device. The cell pitch is 8 μm, and the simulated

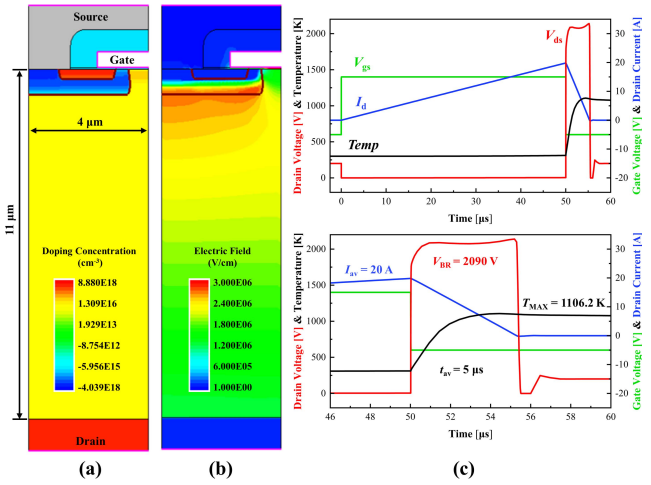

Fig. 7. Device simulation results of SiC MOSFET in avalanche mode, including (a) device structure and doping concentration distribution, (b) electric field distribution, and (c) UIS test results.

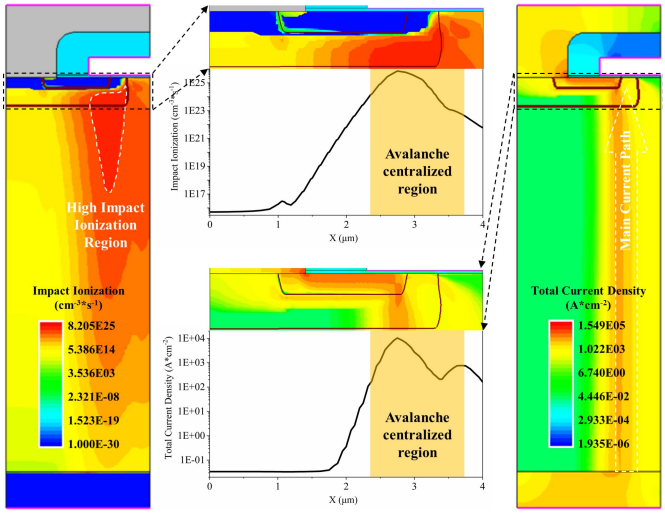

Fig. 8. Impact ionization and avalanche current distribution of SiC MOSFETs in avalanche mode.

breakdown voltage V_{BR} is 2090 V, which is close to the test results of the real device. Although the simulation model cannot quantitatively study the device characteristics, it can qualitatively study the UIS characteristics of DUTs.

The mixed-mode simulation is used to analyze the avalanche process, and the simulation circuit is shown in Fig. 4(a). Okuto–Crowell model is used to simulate the avalanche breakdown characteristics. The parameters of the mixed mode are the same as those of the real UIS test circuit. Fig. 7(b) shows the electric field distribution after the device operates in avalanche mode for 1 μs. Except for the high electric field in the center of the gate oxide, other high electric fields are concentrated at the P-base corner. Fig. 7(c) shows the UIS results of the mixed-mode simulation and the enlarged view of the avalanche process. The t_{ON} is 50 μs to make the I_{av} reach 20 A. The reason why the simulated t_{ON} is different from the real test of the linear cell is that the $R_{ds(ON)}$ of the linear cell DUT is large and the saturation current is small, which leads to the gradual slowing of the rise speed of I_d during the ON state. Therefore, the I_{av} with a linear cell DUT of 20 A requires a t_{ON} of 70 μs, while only 50 μs is required in the simulation. Under the condition of ensuring the same I_{av}, the accuracy of simulation results will not be affected. The simulated t_{av} is 5 μs, which is close to the measured results. During the avalanche, the maximum temperature T_{MAX} of the simulation device reached 1106.2 K, which exceeded the melting point of aluminum (933 K). The metal layer melts, resulting in device failure [4], [5], [6].

Impact ionization and avalanche current density are usually used to quantify avalanche breakdown strength. The impact ionization and avalanche current density of the device in avalanche mode are shown in Fig. 8, and the distribution difference curves at the junction depth are given, respectively. It can be clearly seen that the high-impact ionization and high avalanche current density are concentrated near the corner of the P-base region. As shown in the yellow area of the curve, the avalanche concentration region ranges from 2.5 to 3.65 μm.

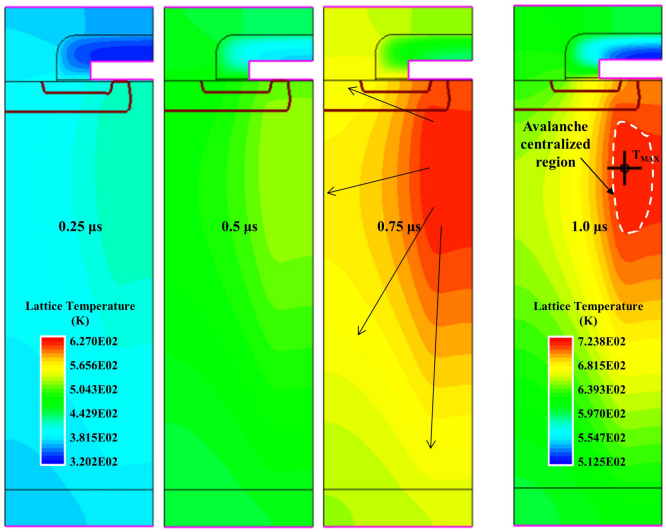

Fig. 9. Lattice temperature distribution of SiC MOSFET in 1 μs after entering avalanche mode.

In order to more clearly show the lattice temperature change process in devices under avalanche mode, Fig. 9 shows the lattice temperature distribution change of SiC MOSFET within 1 μs after entering avalanche mode. Wherein, 0.25, 0.5, and 0.75 μs use the same legend. In order to show the avalanche concentration region more clearly, the lattice temperature distribution of 1.0 μs is displayed separately, and the avalanche concentration region and the highest temperature point are marked. It can be clearly seen that in the avalanche mode, the device first heats from the corner of the P-base region and gradually diffuses to the entire cell, which is consistent with the avalanche current distribution in the avalanche mode. Although avalanche current also exists in the JFET area, which also generates avalanche heat, it can be seen from Fig. 8 that the impact ionization and avalanche current density at the corner of the P-base region are significantly higher than those in the JFET region. Based on the electric

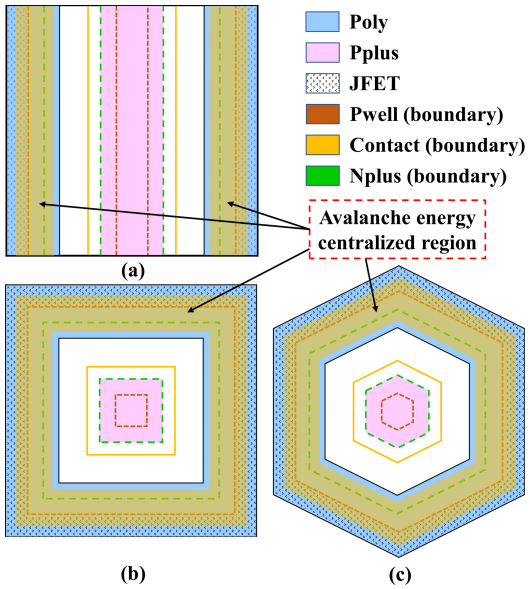

Fig. 10. Avalanche energy concentration regions corresponding to different cell topologies. (a) Linear. (b) Square. (c) Hexagon.

field distribution, the impact ionization rate distribution, the avalanche current distribution, and the lattice temperature change under avalanche mode, it can be concluded that the avalanche energy generated by SiC MOSFET under the UIS test is concentrated near the corner of P-base region, including the channel region, the overlapping part of gate and N+ region, and part of the JFET region.

Fig. 10 shows the avalanche energy concentration regions with the gold area on the cell topologies. The size of the linear is the same as that of the square so that the distribution difference of avalanche energy concentration region can be displayed more intuitively. Because the difference of E_{ava} between the two linear is very small and the distribution of avalanche energy concentration region is similar, for the convenience of comparison, the common linear is used to replace the two. The proportion of avalanche energy concentration regions in linear, square, and hexagonal topologies is 28.7%, 44.2%, and 36.8%, respectively. It can be found that the E_{ava} of the four DUTs is inversely proportional to the proportion of the avalanche energy concentration region of the corresponding topology. The larger the proportion of avalanche energy concentration region, the lower the corresponding UIS energy density E_{ava}.

Considering that during the UIS test, the thermal burning of a cell in the active region will lead to the failure of the DUT, it is only necessary to pay attention to whether the temperature of a single cell reaches the device burning temperature. Define the heat required for a single cell to rise from room temperature to burn-out temperature as Q_s, which is the area of avalanche energy concentration region multiplied by avalanche energy density, as follows:

$$Q_s = E_{\text{ava}} \cdot P_a \cdot S \tag{3}$$

where, E_{ava} is the avalanche energy per unit area, P_a is the proportion of avalanche energy concentration area of cells, and S is the area of a single cell.

The area of a single cell with different shapes is different, so the Q_s required are different. However, the heat required for the cells of the unit area to rise to the burning temperature is the same, which is defined as Q_a, $Q_a = Q_s/S$, and is as follows:

$$Q_{\text{a}} = E_{\text{ava}} \cdot P_{\text{a}}. \tag{4}$$

It is speculated that Q_a is related to the process platform and parameters of the wafer. Different metal layer thicknesses, different contact hole sizes, and other parameters affecting heat transfer may lead to different Q_a. But under the same process platform parameters, whether linear, square, or hexagonal, cell topology devices have the same Q_a, so E_{ava} is inversely proportional to P_a. Based on the UIS test and simulation results, the corresponding Q_a of the four cells in this article is 1.256 ($\pm$0.093) J/cm^2. The reason for a little deviation is related to the value range of the avalanche energy concentration region. This model is in good agreement with the experimental and simulation results.

According to the above model, because the proportion of avalanche energy concentration regions of the square and the hexagonal are higher than that of the linear cell topologies, the avalanche energy density E_{ava} of linear cell topologies devices is higher than that of the square and the hexagonal, which has better UIS reliability. Therefore, when designing SiC MOSFET cell topology, it is necessary to make a trade-off between $R_{\text{ON,sp}}$ and avalanche reliability according to the avalanche reliability requirements of the application scenario.

IV. Conclusion

Based on the standard SiC MOSFET self-aligned process platform, the 1200 V SiC planar MOSFETs wafers with four cell topologies of linear, current sharing linear, square, and hexagon are completed.

The UIS test platform was built and the UIS characteristics of the four cell topologies were tested under the same test conditions. The avalanche energy densities obtained were 4.699, 4.493, 2.773, and 3.164 J/cm^2, respectively. The results show that the single pulse avalanche energy density of linear cell topologies is 1.69 times that of a square and 1.49 times that of a hexagon.

Using TCAD to build a half-cell model, the UIS test process was simulated using mixed-mode simulation. It was found that the avalanche energy of the device was concentrated near the corner of the P-base region in the UIS mode. From this, the avalanche energy distribution differences of the linear, square, and hexagon cell topology were analyzed and compared. A theoretical model of avalanche heating per unit area is proposed, which shows that the avalanche energy density is inversely proportional to the proportion of avalanche energy concentration region. It is proven that the linear was superior to the square and hexagon cell topology in UIS characteristics.

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