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An Adaptive Piling-Up Rectifier-Less SSHI Circuit With Extended Operation Range and Adjustable Peak Power for Piezoelectric Energy Harvesting

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***Abstract*—This article presents a self-powered adaptive piling-up rectifier-less synchronized-switch-harvesting-on-inductor (APReL-SSHI) interface for piezoelectric energy harvesting. The proposed interface introduces two distinct operational modes, energy transfer mode and voltage piling-up mode, that adaptively select the optimal mode based on varying vibration excitation levels to maximize energy extraction. This adaptive mechanism addresses the narrow optimal rectified voltage range (ORVR) limitation inherent in conventional S-SSHI rectifiers by enabling capacitor charging beyond standard thresholds. Experimental results demonstrate that the proposed APReL-SSHI circuit achieves up to 5.27 times the maximum output power compared to a full-bridge rectifier and expands the ORVR by 4.16 times compared to a conventional S-SSHI circuit. Consequently, the APReL-SSHI delivers superior balance between these two key performance metrics compared to existing state-of-the-art rectifiers. Moreover, the circuit uniquely exhibits a secondary output power peak, reaching approximately 94% of maximum power when operated above the standard maximum power point (MPP) voltage. Under constant input conditions, the voltage associated with this secondary power peak is easily adjustable, thereby facilitating direct voltage matching for diverse load requirements and achieving near-MPP tracking efficiency of 94% without the need for an additional MPPT controller.**

***Index Terms*—Adaptive piling-up, optimal rectified voltage range (ORVR), piezoelectric energy harvesting (PEH), rectifier-less, self-powered, synchronized switch harvesting on inductor (SSHI).**

NOMENCLATURE

PEH	Piezoelectric Energy Harvesting.
PT	Piezoelectric Transducer.
ETM	Energy Transfer Mode.
VPM	Voltage Piling-up Mode.
APReL	Adaptive Piling-up Rectifier-less.
SSHI	Synchronized switch harvesting on inductor.
S-SSHI	Series Synchronized switch harvesting on inductor.
P-SSHI	Parallel Synchronized switch harvesting on inductor.
ReL-SSHI	Rectifier-less Synchronized switch harvesting on inductor.
SECE	Synchronized Electric Charge Extraction.
ORVR	Optimal Rectified Voltage Range.
FBR	Full-bridge Rectifier.
MPP	Maximum Power Point.
MPPT	Maximum Power Point Tracking.
ROI	Region of Interest.
FoM	Figure of Merit.

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I. INTRODUCTION

THE proliferation of Internet of Things (IoT) technology has facilitated ubiquitous connectivity in modern society. However, ensuring sustainable operation of distributed wireless sensor networks (WSNs) remains a significant challenge. Energy harvesting technologies, capable of converting ambient sources such as solar, thermal, and kinetic energy into electrical power, have thus emerged as promising solutions to enable autonomous WSN nodes [1], [2], [3], [4], [5]. Among these techniques, piezoelectric energy harvesting (PEH), based on PTs, offers notable advantages, including high energy density, resilience to environmental conditions, and the capacity to harvest widely available kinetic energy [6]. In addition, PEH contributes to achieving net-zero emissions and promotes sustainability by utilizing renewable energy sources.

Typically, a weakly coupled PT operating near its resonant frequency can be modeled as a sinusoidal current source I_p, in parallel with a parasitic capacitor C_p and an internal resistor R_p, as illustrated in Fig. 1 [7]. Given that PT outputs an alternating current (AC) voltage while most WSN nodes require direct current (DC) power, an interface circuit with rectification and voltage regulation capabilities becomes essential [8]. Over the past decades, extensive research has been conducted on various interface circuits, including FBRs [9], [10], [11], SSHI [12],

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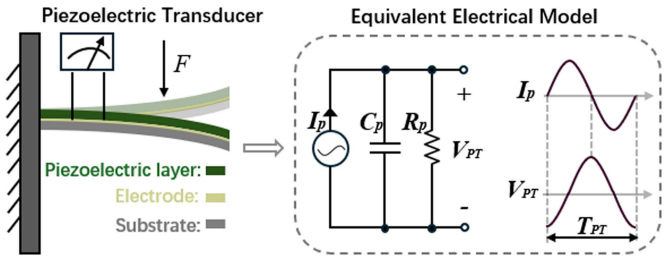


Fig. 1. Piezoelectric transducer and its equivalent circuit.

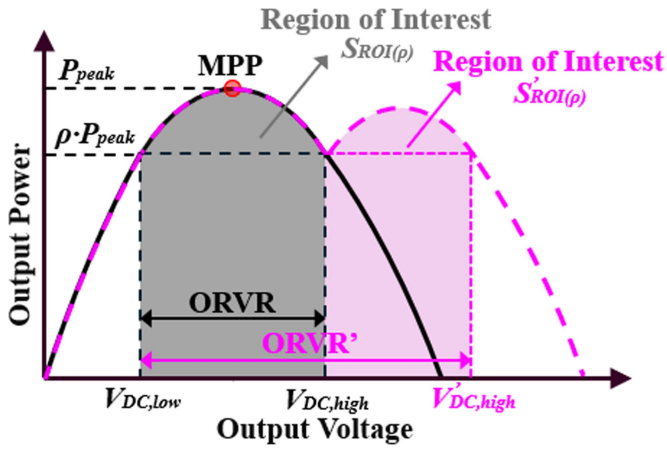


Fig. 2. Rectifier power curves before and after ORVR extension.

[13], [14], [15], [16], [17], [18], [19], SECE [20], [21], [22], [23], [24], [25], and synchronized switch harvesting on capacitors (SSHC) circuits [26], [27], [28], [29], [30].

The simplest interface circuit is the FBR, which comprises four diodes and a storage capacitor. However, due to the internal capacitor C_p of a PT, a significant amount of PT-generated charge is wasted to charge and discharge C_p, which results in a poor energy-extraction performance [31]. To mitigate the effects of C_p, the SSHI technique was proposed [12]. It incorporates an inductor into the circuit, enabling rapid flipping of the PT voltage at its peaks via LC resonance within half of the LC oscillation period. The SSHI circuit can be further classified into series-SSHI (S-SSHI) and parallel-SSHI (P-SSHI) topologies, depending on whether the inductor is connected in series or in parallel with the PT. Several advanced SSHI topologies have been proposed to improve the performance. Chen [14] and Wang [15] separately proposed self-powered BJT-switched P-SSHI and S-SSHI circuits, with 3.6× and 5.9× maximum power-extraction enhancement over FBR, respectively. Jeong et al. [17] introduced an N-step SSHI rectifier with 11.7× enhancement via reduced inductor root-mean-sqaure (RMS) current. Yue et al. [19] demonstrated a dual-mode P-SSHI rectifier solving startup issues while delivering 11.8× higher power than an FBR.

The SECE technique, first proposed in 2005 [20], is another widely used method that employs LC resonance to improve energy extraction efficiency. It extracts energy from C_p to the inductor within a quarter of the LC oscillation period, and subsequently transfers it to the storage capacitor. In contrast with SSHI, it can eliminate the power load dependency and has a wider operation range, but at the cost of a lower maximum output power. Chen et al. [21] proposed a novel rectifier-less SECE circuit, which extracts partial charges and inverts the remaining energy across C_p. A self-powered SECE-based multi-PT interface circuit (MI-SP-SECE) was proposed in [22], demonstrating a 2.8× power improvement compared to conventional multiinput FBR. To achieve full on-chip integration, Du et al. first proposed the SSHC technique in 2017 [26], which replaces bulky off-chip inductors with switched capacitors to accomplish the flipping of the PT voltage. Yue et al. [27] proposed an improved SSHC rectifier which reused storage capacitors as flying capacitors for bias-flip operations and reached a 7.58× power enhancement.

For the majority of interface circuits mentioned above, they mainly focus on improving the maximum output power. However, it is not the sole metric for evaluating the performance of PEH interface circuits. The ORVR is an equally critical metric, which is the ideal output voltage window where the interface circuits can deliver satisfactory output power [32]. A good PEH interface circuit should achieve a good balance between these two metrics. But all the aforementioned fundamental topologies exhibit suboptimal balance between these metrics due to inherent limitations in their operating principles. To achieve a better balance, Xia et al. [32] proposed a self-powered hybrid rectifier combining S-SSHI and SECE techniques, which achieves 1.55× maximum output power of SECE and 4.58× ORVR of S-SSHI. Wang et al. [18] advanced the development with an SSHI-SECE hybrid rectifier for multi-PT systems, demonstrating 3.61× higher maximum power and 2.64× wider ORVR compared to multi-input FBRs. Chen et al. [23] designed an on-chip synchronous inversion and change extraction interface circuit, which also synergistically combines the advantages of both SSHI and SECE.

This article proposed a novel adaptive piling-up rectifier-less SSHI (APReL-SSHI) interface for PEH. By incorporating an adaptively controlled switch and optimizing the PT voltage flipping strategy, the proposed circuit can achieve a superior balance between these two metrics. Moreover, it features a voltage-adjustable second peak power point, enabling direct voltage matching across varying load requirements without DC–DC converters and MPPT controllers, further extending the ORVR.The rest of this article is organized as follows. Section II details the theoretical analysis of the proposed APReL-SSHI circuit. The circuit implementations and operating principles are described in Section III, followed by simulation analysis in Section IV. Section V provides measured results and comparisons with state-of-the-art interface circuits. Finally, Section VI concludes this article.

II. APReL-SSHI Interface Circuit

A. Design Motivation

As discussed previously, a high-performance rectifier should well balance its maximum output power and ORVR. The black curve in Fig. 2 represents the typical output power characteristic

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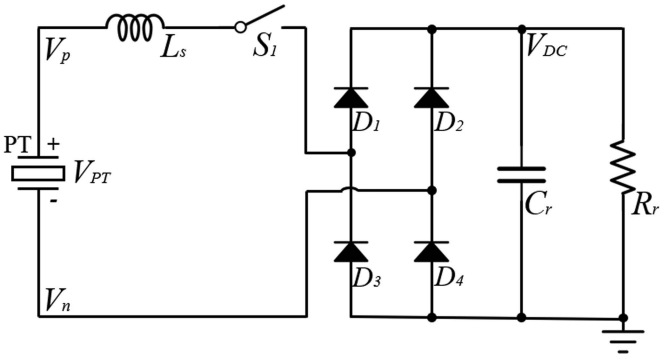


Fig. 3. Topological structure of conventional S-SSHI circuit.

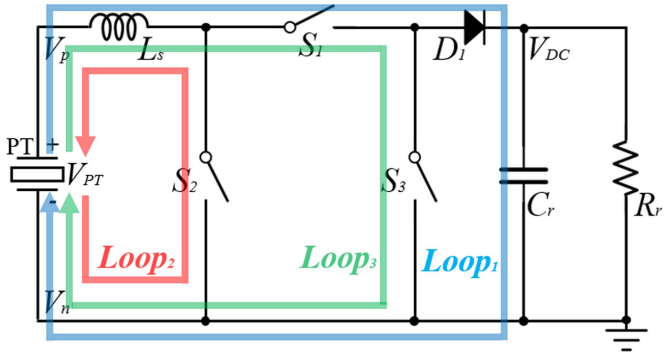


Fig. 4. Topological structure of proposed APReL-SSHI circuit.

of a rectifier versus its output voltage, where P_{peak} denotes the maximum output power. Given a typical coefficient range of $\rho \in [0.8, 0.95]$, the output power level $\rho \cdot P_{\text{peak}}$ corresponds to a voltage range $[V_{\text{DC,low}}, V_{\text{DC,high}}]$, which defines the ORVR. To establish a metric for the comprehensive evaluation of both the maximum output power and the ORVR, the gray-shaded area is defined as the region of interest (S_{RoI_ρ}) of the rectifier, which can be approximately calculated as below [32]

$$S_{\text{RoI}_\rho} = 0.5\left(V_{DC,\text{high}} - V_{DC,\text{low}}\right)(1+\rho)\,P_{\text{peak}}. \tag{1}$$

Fig. 3 shows a conventional S-SSHI topology; the fundamental reason for its narrower ORVR performance compared to SECE and P-SSHI lies in the essential involvement of its storage capacitor C_r in every LC resonant cycle. Consequently, the inversion of V_{PT} is centered at the output voltage V_{DC}, causing energy extraction performance degradation as V_{DC} increases. Once V_{PT} drops close to V_{DC}, the PT can no longer transfer energy, restricting its theoretical maximum output voltage to the open-circuit voltage (V_{OC}) of the PT. Since this inherent drawback restricts the application of the S-SSHI circuit in scenarios requiring wider voltage adaptability, we proposed the APReL-SSHI circuit, which can significantly extend the ORVR while preserving the peak output power performance, as shown by the dashed pink curve in Fig. 2. While maintaining the maximum output power, its ORVR is extended to $[V_{\text{DC,low}}, V'_{\text{DC,high}}]$. This enhancement consequently yields an enlarged region of interest area calculated as below

$$S'_{\text{RoI}_\rho} = 0.5\left(V'_{DC,\text{high}} - V_{DC,\text{low}}\right)(1+\rho)\,P_{\text{peak}}. \tag{2}$$

Compared to rectifiers with high maximum output power but limited ORVR, such as S-SSHI topology, this method enables superior tradeoff optimization between these two critical metrics. The operation principle of the APReL-SSHI circuit will be detailed in the next section.

B. Operation Principle

The topological structure of the proposed APReL-SSHI circuit is depicted in Fig. 4 while its circuit implementation details will be given in later parts. Advancing the architecture of the ReL-SSHI topology presented in [15], the APReL-SSHI circuit introduces an additional switch S_3 and a diode D_1, along with further optimized control strategies. In this way, it can adaptively pile up V_{PT} to prevent energy extraction performance from degrading as V_{DC} increases, thus maintaining maximum output power while significantly expanding the ORVR.

In each vibration cycle, the APReL-SSHI circuit can operate in either of two distinct modes: ETM and VPM, and the operation waveforms of these two modes are shown in Fig. 5. During the initial startup period, the V_{DC} is low, and the circuit operates only in ETM. In this mode, circuit control is exclusively governed by switches S_1 and S_2, which exhibit identical operating principles to ReL-SSHI. During most of the time in both positive and negative half-cycles, S_1 and S_2 remain open, so all energy accumulates in the internal capacitance of the PT, C_p, to increase the absolute value of V_{PT}. When V_{PT} reaches its positive peak, S_1 will close to form a resonant loop, $Loop_1$, composed of C_p, D_1, C_r and the inductor L_s, allowing energy transfer from the PT to C_r and voltage flipping of V_{PT} for half of the LC resonance period. Similarly, at the negative peak of V_{PT}, S_2 will close to form $Loop_2$. This operation simply flips V_{PT} without transferring energy to C_r, which contributes to eliminating the need for a rectifier.

However, as V_{DC} progressively increases, if the circuit only works in the energy transfer mode (ETM), the peak of V_{PT} will continuously decrease until it approaches V_{DC}, ultimately reaching a state where the PT can hardly transfer energy to C_r. Hence, when V_{DC} exceeds a predetermined threshold, the system enters the VPM to increase the peak of V_{PT}. The specific threshold-setting methodology for entering VPM will be detailed in the next section. In this mode, all three switches (S_1, S_2, and S_3) participate in the control mechanism. Specifically, when V_{PT} reaches its positive peak, both S_1 and S_3 close, forming the LC resonant loop $Loop_3$ with C_p and L_s. After half of the LC resonance cycle, the V_{PT} is reversed. Then, at the negative V_{PT} peak, S_2 will close to form a LC resonant loop $Loop_2$. Similarly, after another half resonance period, V_{PT} reverses polarity again. After a vibration cycle in the VPM, V_{PT} increases to a higher voltage level since the energy harvested from the PT is dedicated to the accumulation of V_{PT} rather than transferring to C_r. Consequently, if V_{DC} increases and V_{PT} decays to the predetermined threshold, the circuit will first

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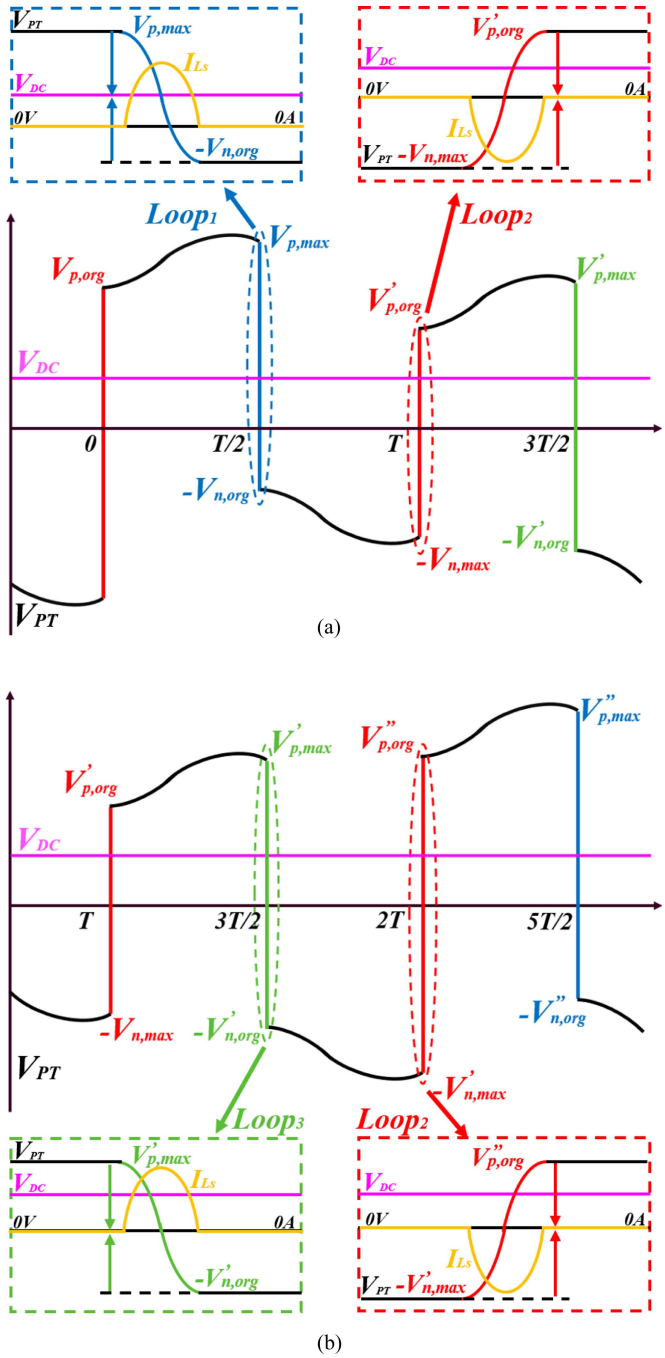


Fig. 5. Theoretical operation waveforms of APReL-SSHI. (a) Waveforms under Energy Transfer Mode. (b) Waveforms under Voltage Piling-Up Mode.

enter VPM for one or more cycles to pile up V_{PT}. Only after successful V_{PT} voltage recovery does the circuit switch back to ETM for energy transfer, enabling efficient energy transfer even at high V_{DC} and theoretically extending the output range to the maximum achievable value of V_{PT}, fundamentally overcoming the ORVR limitation of S-SSHI.

C. Theoretical Analysis

For the LC resonant loops Loop_1, Loop_2 and Loop_3 shown in Fig. 4, we define the corresponding electrical quality factors as Q_1, Q_2, and Q_3, respectively. Based on this, the voltage inversion factors of each LC loop can be expressed as

$$\begin{cases} \gamma_1 = e^{-\frac{\pi}{2Q_1}}, & 1 > \gamma_1 > 0 \\ \gamma_2 = e^{-\frac{\pi}{2Q_2}}, & 1 > \gamma_2 > 0 \\ \gamma_3 = e^{-\frac{\pi}{2Q_3}}, & 1 > \gamma_3 > 0. \end{cases} \tag{3}$$

As described in Section I, the PT can be modeled as a sinusoidal current source I_p in parallel with a capacitance C_p and resistance R_p. The total charge Q_{total} delivered by the PT during half of a vibration cycle ($T/2$) can be calculated as

$$Q_{total} = \int_0^{T/2} I_p \, dt. \tag{4}$$

Accordingly, the open-circuit voltage variation across the PT over this half-cycle is

$$\begin{aligned} \Delta V &= V_{p,\max} - V_{p,\text{org}} = V_{n,\max} - V_{n,\text{org}} \\ &= V'_{p,\max} - V'_{p,\text{org}} = V'_{n,\max} - V'_{n,\text{org}} \\ &= V''_{p,\max} - V''_{p,\text{org}} = \frac{Q_{total}}{C_p} = \frac{2\alpha U_M}{C_p}. \end{aligned} \tag{5}$$

Here, α is the force-to-voltage conversion factor of the PT and U_M is the displacement amplitude. The voltage variables such as $V_{p,\max}$ and $V_{p,\text{org}}$ correspond to different time points as illustrated in Fig. 5. Under a constant vibration frequency and maximum amplitude, both Q_{total} and ΔV remain fixed.

When the APReL-SSHI circuit operates in ETM, at the positive peak of V_{PT}, $V_{p,\max}$ inverts across the V_{DC} axis, producing $-V_{n,\text{org}}$. At the negative peak, $-V_{n,\max}$ inverts across the time axis, giving $V'_{p,\text{org}}$. These behaviors lead to the following expressions:

$$\begin{cases} V_{n,\text{org}} + V_{DC} = \gamma_1 (V_{p,\max} - V_{DC}) \\ V'_{p,\text{org}} = \gamma_2 V_{n,\max}. \end{cases} \tag{6}$$

Here, V_{DC} denotes the output voltage of APReL-SSHI. Following the theoretical framework in [15], [33], when the circuit remains in ETM during the initial operation stage, the maximum output power is given by

$$\begin{aligned} P_{\text{ETM},\max} &= \frac{f C_p \Delta V^2}{4} \frac{(1+\gamma_1)(1+\gamma_2)}{1-\gamma_1\gamma_2} \\ &= \frac{f \alpha^2 U_M^2}{C_p} \frac{(1+\gamma_1)(1+\gamma_2)}{1-\gamma_1\gamma_2}. \end{aligned} \tag{7}$$

The corresponding optimal output voltage can be expressed as follows:

$$V_{\text{DC},\text{opt}} = \frac{\Delta V}{2} = V_{\text{OC,org}} \tag{8}$$

where $V_{\text{OC,org}}$ is the intrinsic open-circuit voltage of the PT.

As V_{DC} keeps rising after exceeding $V_{\text{DC},\text{opt}}$, the circuit enters voltage piling-up mode (VPM) upon reaching a predefined threshold. In this mode, the system alternates between VPM and ETM. When V_{PT} is insufficient, VPM operates for several vibration cycles to accumulate energy before switching to ETM for a single cycle to transfer the harvested energy to C_r. An example case is analyzed where one VPM cycle is followed by

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one ETM cycle. The voltage relationships in this scenario are

$$\begin{cases} V'_{n,\text{org}} = \gamma_3 V'_{p,\max} \\ V''_{p,\text{org}} = \gamma_2 V'_{n,\max} \\ V''_{n,\text{org}} + V_{DC} = \gamma_1 (V''_{p,\max} - V_{DC}). \end{cases} \tag{9}$$

Combining (5) and (9), it can be derived that

$$V''_{n,\text{org}} = \frac{\Delta V \gamma_1 \left(1 + \gamma_2 + \gamma_2\gamma_3 + \gamma_2^2\gamma_3\right) - V_{DC}\left(1+\gamma_1\right)}{1 - \gamma_1\gamma_2^2\gamma_3} \tag{10}$$

and

$$V''_{p,\max} + V''_{n,\text{org}} = \frac{\Delta V \left(1 + \gamma_2 + \gamma_2\gamma_3 + \gamma_2^2\gamma_3\right)\left(\gamma_1 + 1\right)}{1 - \gamma_1\gamma_2^2\gamma_3} - \frac{V_{DC}\left(1 + \gamma_2^2\gamma_3\right)\left(\gamma_1 + 1\right)}{1 - \gamma_1\gamma_2^2\gamma_3}. \tag{11}$$

In this case, the circuit transfers energy from the PT to C_r once every two vibration cycles through an LC resonant process. The transferred energy can be calculated as follows:

$$E_{\text{ReL}} = \int_0^{T_{LC}/2} V_{\text{DC}} \cdot I_{Ls} dt = V_{\text{DC}} C_p \left(V''_{p,\max} + V''_{n,\text{org}}\right). \tag{12}$$

Therefore, the output power can be expressed as

$$P_{\text{VPM}} = \frac{f}{2} V_{\text{DC}} C_p \left(V''_{p,\max} + V''_{n,\text{org}}\right) = \frac{f C_p V_{\text{DC}} \left(\frac{(1+\gamma_2)(1+\gamma_2\gamma_3)}{1+\gamma_2^2\gamma_3}\Delta V - V_{\text{DC}}\right)\left(1+\gamma_1\right)\left(1+\gamma_2^2\gamma_3\right)}{2\left(1-\gamma_1\gamma_2^2\gamma_3\right)}. \tag{13}$$

Then, by differentiating (13) with respect to V_{DC} and setting the derivative to zero, the optimal output voltage is obtained

$$V'_{\text{DC},\text{opt}} = \frac{\left(1+\gamma_2\right)\left(1+\gamma_2\gamma_3\right)}{2\left(1+\gamma_2^2\gamma_3\right)}\Delta V \geq \frac{\left(1+\gamma_2\right)}{2}\Delta V = \left(1+\gamma_2\right) V_{\text{OC,org}}. \tag{14}$$

The corresponding maximum output power is

$$P_{\text{VPM,max}} = \frac{f C_p \Delta V^2}{4} \frac{\left(1+\gamma_2\right)^2\left(1+\gamma_2\gamma_3\right)^2\left(1+\gamma_1\right)\left(1+\gamma_2^2\gamma_3\right)}{2\left(1-\gamma_1\gamma_2^2\gamma_3\right)\left(1+\gamma_2^2\gamma_3\right)^2} \geq \frac{f C_p \Delta V^2}{4} \frac{\left(1+\gamma_2\right)^2\left(1+\gamma_2\gamma_3\right)\left(1+\gamma_1\right)}{2\left(1-\gamma_1\gamma_2^2\gamma_3\right)} = \frac{f\alpha^2 U_M^2}{C_p} \frac{\left(1+\gamma_2\right)^2\left(1+\gamma_2\gamma_3\right)\left(1+\gamma_1\right)}{2\left(1-\gamma_1\gamma_2^2\gamma_3\right)}. \tag{15}$$

By comparing (8) and (14), it is observed that activating the VPM increases the output voltage at the MPP of the APReL-SSHI circuit beyond that achieved by the ETM alone. This indicates that once VPM is activated and the output voltage exceeds $V_{\text{OC,org}}$, the circuit exhibits a second output power peak. Moreover, a comparative analysis of (7) and (15) reveals that with appropriately selected voltage inversion factors γ_1, γ_2, and γ_3, the second power peak can theoretically exceed the first peak (equivalent to the maximum output power of ReL-SSHI). Under ideal conditions where $\gamma_1 < \gamma_2 = \gamma_3 = 1$ (noting that the equivalent series resistance of C_r in $Loop_1$ inherently keeps γ_1 smaller), substituting into (7) and (15) shows that the second power peak reaches twice the magnitude of the first, independent of the specific value of γ_1. Furthermore, as established in [34], the maximum power of conventional S-SSHI (16) is merely one-quarter of this second power peak

$$P_{\text{S-SSHI,max}} = \frac{f\alpha^2 U_M^2}{C_p} \frac{1+\gamma_1}{1-\gamma_1}. \tag{16}$$

Based on the above analysis, incorporating VPM into the proposed APReL-SSHI circuit enhances both ORVR and peak output power. It should be noted, however, that this represents the theoretically ideal harvestable power. In practical implementations, parasitic components in the resonant loop reduce voltage inversion efficiency, thereby degrading circuit performance.

III. Implementation of APReL-SSHI Circuit

The detailed implementation of the proposed APReL-SSHI circuit is illustrated in Fig. 6. The system comprises three main functional modules: 1) a synchronized switch; 2) an envelope extractor; and 3) a switch controller. In addition, D_1 is selected as a Schottky diode to mitigate the impact of the diode voltage drop on the circuit.

The synchronized switch is built using four BJTs and a peak-detection capacitor C_1[15]. Among them, the NPN transistor Q_2 and the PNP transistor Q_4 serve as the main switching elements for the LC resonant loop, corresponding to switches S_1 and S_2 in Fig. 4, respectively. The remaining transistors Q_1 and Q_3, together with C_1, form the peak detection unit that senses the maximum of V_{PT} and generates control signals to drive Q_2 and Q_4 accordingly.

The envelope extractor is implemented using two high-resistance resistors (R_1, R_2), a diode D_2, and a capacitor C_2. The diode and capacitor capture the peak envelope of V_{PT} during each positive half-cycle. The resistors R_1 and R_2 form a voltage divider that attenuates this peak signal, producing an output voltage V_{PG}. Assuming the voltage division ratio is $k = R_2/(R_1 + R_2)$ and neglecting the diode's forward voltage, we can get the divided output V_{PG} which is equal to $kV_{PT,max}$. It varies from zero to the peak of V_{PT} depending on the chosen k.

The switch controller includes a comparator, a low-dropout regulator (LDO), an NMOS transistor MP_1, and a zener diode D_3. In this setup, MP_1 acts as the control switch for voltage piling-up mode (VPM), corresponding to S_3 in Fig. 4. The LDO and zener diode together regulate the V_{DC} level to match the comparator's supply requirement. The zener diode is optionally included depending on the type of LDO used. It prevents premature activation of the LDO under low V_{DC} and partially protects the LDO from an overrange input voltage. It should also be noted that, due to the input/output voltage range limitations of the LDO and the allowable supply voltage range of the comparator, the

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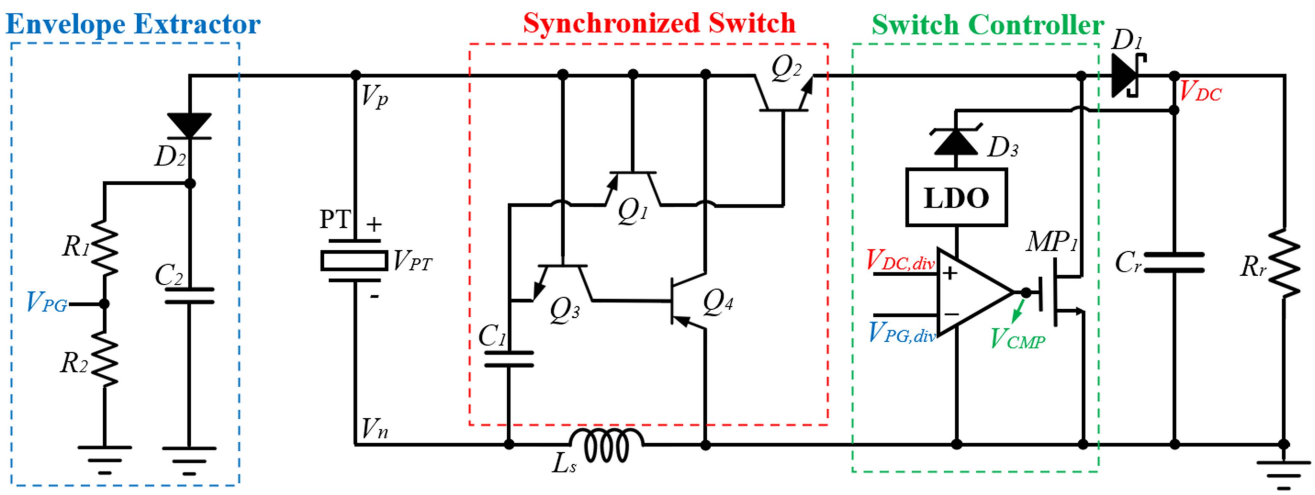


Fig. 6. Schematic of the proposed APReL-SSHI circuit.

appropriate component models should be selected based on the vibration conditions of the PT.

The comparator monitors V_{DC} and V_{PG} and generates a control signal V_{CMP} to drive MP_1. In practical testing, both V_{DC} and V_{PG} must be attenuated before being fed into the comparator to ensure that their magnitudes remain within the acceptable input and supply ranges. These scaled voltages are denoted $V_{DC,div}$ and $V_{PG,div}$.

The detailed operation of the APReL-SSHI circuit is described as follows. Let V_{be} represent the base-emitter voltage drop of the BJTs. When the circuit operates in energy transfer mode (ETM), during the positive half-cycle of V_{PT} ($V_{PT} > 0$), current flows through the base-emitter junction of Q_3, charging capacitor C_1. When V_{PT} reaches its maximum value $V_{PT,\max}$, the voltage across C_1 becomes $V_{PT,\max} - V_{be}$. As V_{PT} decreases, C_1 holds its voltage due to the absence of a discharge path. When V_{PT} drops to $V_{PT,\max} - 2V_{be}$, the emitter-base junction of Q_1 becomes forward-biased, turning on Q_2 and forming an LC resonance loop comprising C_p, Q_2, C_r, D_1, and L_s, corresponding to Loop_1 in Fig. 4. The negative half-cycle operation follows an analogous mechanism, activating Q_4 instead.

As V_{DC} keeps rising, the circuit will enter the VPM when the predefined threshold is reached. We define this threshold by satisfying three conditions simultaneously: 1) V_{DC} must be sufficiently high to power the comparator; 2) V_{DC} must exceed V_{PG}; 3) Q_2 must be in the conduction phase. Based on prior analysis, it is established that Q_2 conducts only during the positive half cycle at the moment when V_{PT} drops to $V_{PT,\max} - 2V_{be}$. If conditions 1) and 2) are also satisfied at this precise moment, the comparator outputs a high-level V_{CMP} signal, driving MP_1 to turn ON. This triggers the transition of the circuit into the VPM. At this point, current will not flow through D_1 and C_r, and instead forms a new LC resonant loop involving C_p, Q_2, MP_1, and L_s, defined as Loop_3 in Fig. 4.

To illustrate the overall behavior, we analyze the circuit waveforms across one and a half vibration cycles, during which the APReL-SSHI transitions between ETM and VPM. The waveform is divided into nine temporal phases, and Fig. 7 presents the corresponding current flow for six key phases. A detailed discussion of each phase is provided in the next subsection.

A. *Natural Charging Phase* ($t_0 \sim t_1$; $t_3 \sim t_4$; $t_6 \sim t_7$)

At the beginning of each half-cycle of V_{PT}, the circuit first enters the natural charging phase. During the positive charging phase ($t_0 \sim t_1$; $t_6 \sim t_7$), the equivalent current source of the PT I_p charges the internal capacitor C_p, while simultaneously charging C_1 through the transistor Q_3. During this period, the voltage across the PT can be described as

$$V_{PT}(t) = V_{PT,t_0} + \frac{\int_{t_0}^{t} I_p dt}{C_p + C_1} = V_{PT,t_0} + \frac{\int_{t_0}^{t} A\sin(\omega t) dt}{C_p + C_1}. \tag{17}$$

When I_p passes through half of the vibration period ($T/2$) and is about to reverse direction, V_{PT} reaches its maximum value

$$\begin{aligned} V_{PT,\max} &= V_{PT,t_0} + \frac{\int_{t_0}^{t_0+T/2} I_p \, dt}{C_p + C_1} \\ &= V_{PT,t_0} + \frac{2A}{\omega(C_p + C_1)}. \end{aligned} \tag{18}$$

At this instant, the voltage stored on C_1 becomes

$$V_{C1,\max} = V_{PT,\max} - V_{be} \tag{19}$$

where V_{be} is the base-emitter voltage drop of transistor Q_3. It is important to note that the inclusion of C_1 results in nonnegligible energy loss during the half cycle, as it shares charge with C_p. The corresponding energy loss is calculated as

$$\begin{aligned} E_{loss_1} = &\frac{1}{2} C_p \left(V_{PT,t_0} + \frac{2A}{\omega C_p} \right)^2 \\ &- \frac{1}{2} C_p \left(V_{PT,t_0} + \frac{2A}{\omega(C_p + C_1)} \right)^2. \end{aligned} \tag{20}$$

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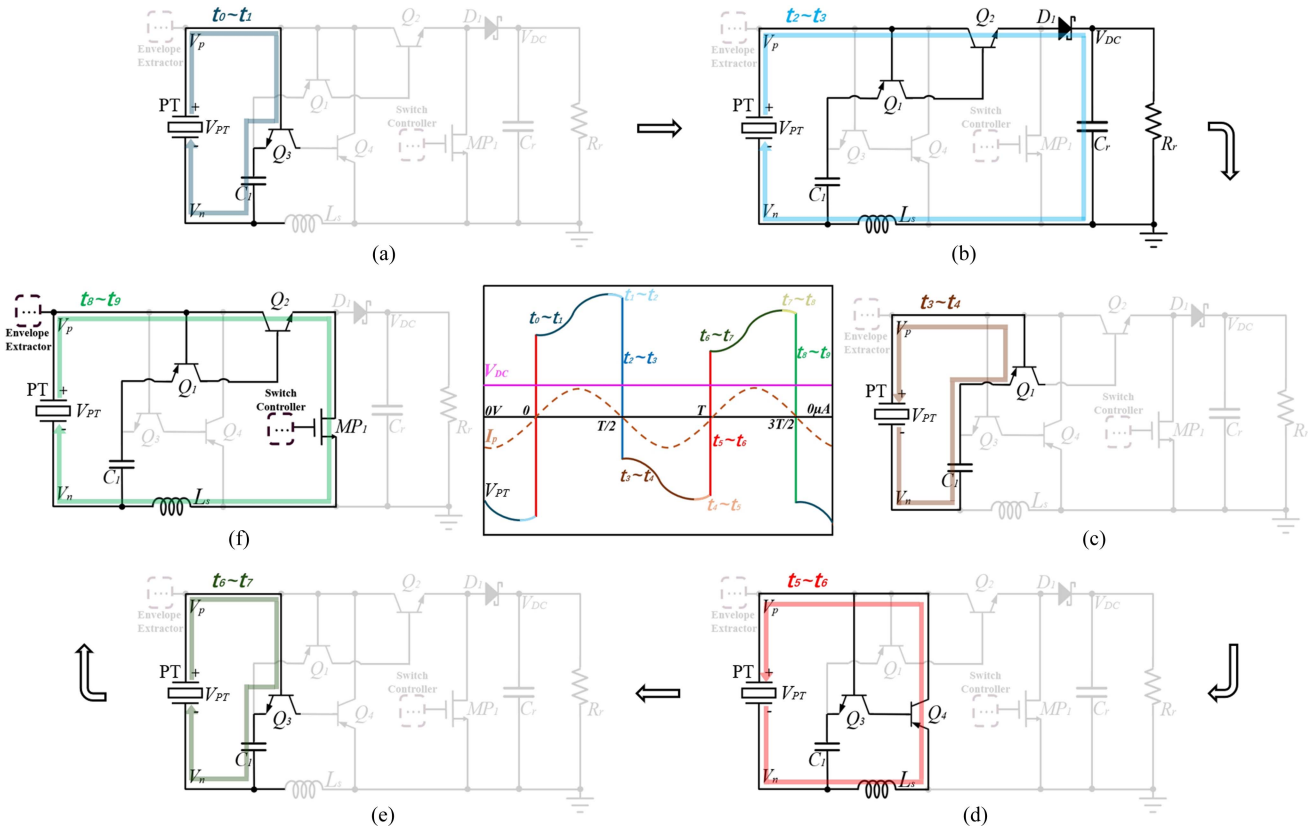


Fig. 7. Current flow direction in six phases: (a) positive natural charging ($t_0 \sim t_1$); (b) energy transfer ($t_2 \sim t_3$); (c) negative natural charging ($t_3 \sim t_4$); (d) negative voltage inversion ($t_5 \sim t_6$); (e) positive natural charging ($t_6 \sim t_7$); and (f) positive voltage inversion ($t_8 \sim t_9$).

To minimize this loss, C_1 should be kept as small as possible. However, as discussed in [15], it must satisfy the constraint

$$C_1 > \frac{1}{\beta} C_p \tag{21}$$

where β is the current gain of the transistors in the synchronous switch. If C_1 is set too small, it may cause unreliable switching behavior. During the negative natural charging phase ($t_3 \sim t_4$), the operation principle remains the same and follows an identical analytical procedure.

B. Current Reversion Phase ($t_1 \sim t_2$; $t_4 \sim t_5$; $t_7 \sim t_8$)

At the beginning of the positive current reversion phase (t_1 and t_7), the direction of I_p reverses, initiating the discharge of C_p. The voltage across C_1 remains fixed at $V_{C_1,\max}$, as defined in (19), due to the absence of a discharge path. As V_{PT} decreases and reaches $V_{C_1,\max}$, transistor Q_3 turns off. As V_{PT} continues to fall and reaches $V_{C_1,\max} - V_{be}$ at t_2 and t_8, the base-emitter junction of Q_1 becomes forward-biased, which activates Q_2.

The resulting phase lag between the peak of V_{PT} and the switching event can be expressed as

$$\theta = \cos^{-1}\left(\frac{V_{PT,\max} - 2V_{be}}{V_{PT,\max}}\right). \tag{22}$$

The same principle applies for the negative current reversion phase ($t_4 \sim t_5$), and the lag is calculated using the same approach.

C. Energy Transfer Phase ($t_2 \sim t_3$)

During this phase, energy is transferred from the PT and C_1 to the storage capacitor C_r via LC resonance. The voltage relationship between the start and end of this phase is given by

$$V_{PT,t_3} + (V_{DC} + V_{ce} + V_{D1}) = \gamma_1[V_{PT,t_2} - (V_{DC} + V_{ce} + V_{D1})]. \tag{23}$$

Here, V_{ce} represents the voltage drop across Q_2, V_{D1} is the forward voltage drop of diode D_1, and γ_1 is the voltage inversion factor defined in (3). Energy losses during this phase arise from conduction through Q_2, D_1, and the equivalent series resistance (ESR) of the inductor L_s. These losses can be quantified as

$$E_{loss_2} = \int_0^{\pi\sqrt{LC}} [(V_{ce} + V_{D1})I_L + R_{ESR}I_L^2]dt \tag{24}$$

where I_L is the current through inductor L_s.

D. Voltage Inversion Phase ($t_5 \sim t_6$; $t_8 \sim t_9$)

During the positive inversion phase ($t_8 \sim t_9$), both Q_2 and MP_1 are turned ON, forming an LC resonant loop that includes C_p, L_s, Q_2, and MP_1, as shown in Fig. 7(f). After half of the LC resonant period, the charge stored in C_p is transferred from the V_p terminal to the V_n terminal, thereby inverting V_{PT}. The relationship between V_{PT} at the beginning and end of this phase

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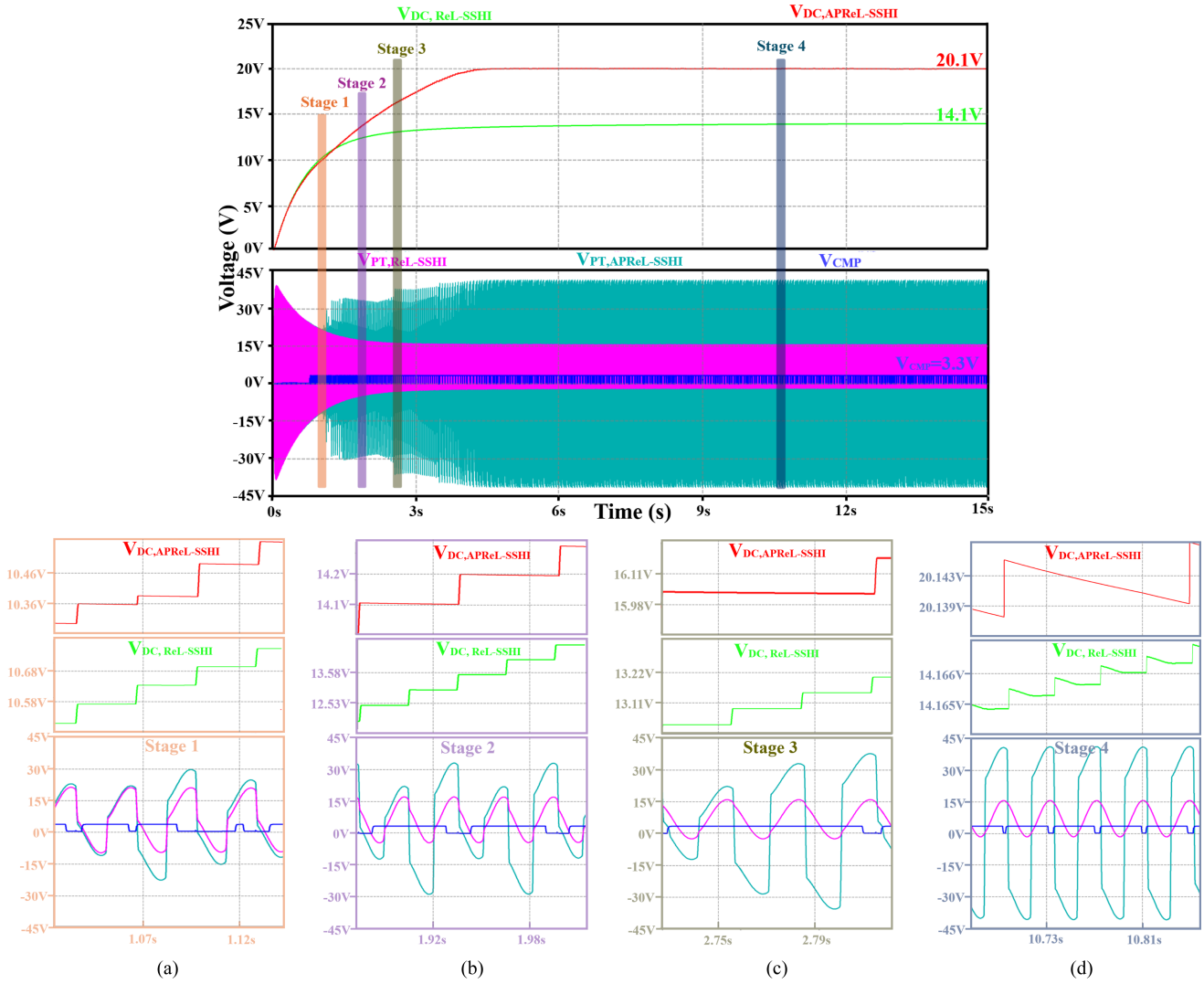


Fig. 8. Simulation waveforms of V_{DC} and V_{PT} for APReL-SSHI (compared with ReL-SSHI). (a) Stage 1: Comparator starts working. (b) Stage 2: Charging once every 2 cycles. (c) Stage 3: Charging once every 3 cycles. (d) Stage 4: Just flipping every cycle.

can be expressed as

$$V_{PT,t_9} + V_{ce} = \gamma_3[V_{PT,t_8} - V_{ce}]. \tag{25}$$

In addition to the losses from switch conduction and inductor ESR, which follow a similar form as in (24), the power dissipation in the LDO and comparator must also be considered. These can be expressed as

$$E_{loss,LDO} = \int_0^{\pi\sqrt{LC}} [V_{DC} I_{Q,LDO} + (V_{DC} - V_{supply}) I_{load}] dt \tag{26}$$

$$E_{loss,CMP} = \int_0^{\pi\sqrt{LC}} [V_{supply} I_{load}] dt. \tag{27}$$

Here, $I_{Q,\mathrm{LDO}}$ is the LDO's quiescent current, V_{supply} is the supply voltage of the comparator, and I_{load} is the total current drawn by the comparator and associated logic.

In order for MP_1 to turn ON, V_{DC} must not only be sufficient to power the comparator, but also must exceed the comparator threshold

$$V_{DC} > V_{PG} = k \cdot V_{PT,max} = \frac{R_2}{R_1 + R_2} V_{PT,max}. \tag{28}$$

By adjusting the value of k, the threshold voltage at which the comparator activates can be modified. This provides a means to control the triggering point of the VPM, thereby tailoring the output voltage characteristics to match varying load requirements.

The negative inversion phase ($t_5 \sim t_6$) operates in the same manner and is not further discussed here for brevity.

IV. Simulation Analysis

To validate the theoretical analysis, the APReL-SSHI circuit shown in Fig. 6 was simulated using LTSpice. The PT of $C_p = 190$ nF is excited at $f = 32$ Hz, consistent with the measurement setup in the next section. Fig. 8 compares the

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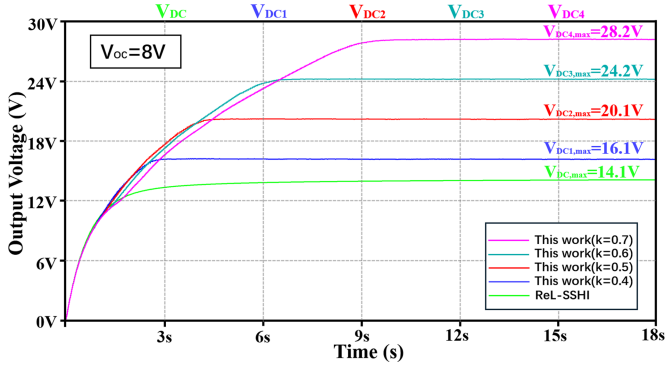


Fig. 9. Output voltage under different k.

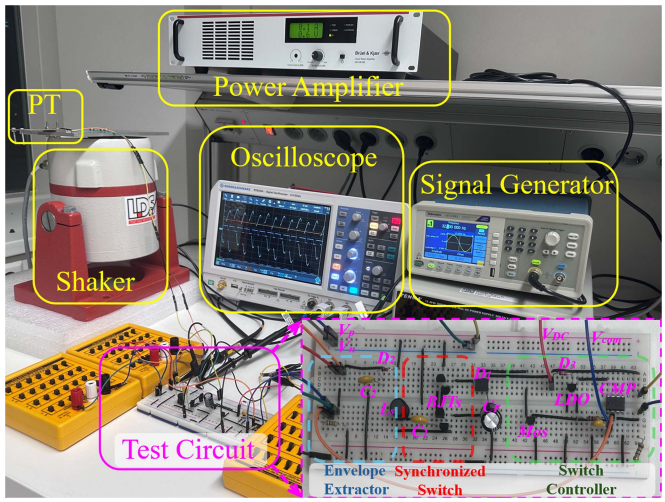


Fig. 10. Experimental setup.

simulation waveforms of the PT voltage V_{PT} and the output voltage V_{DC} for both the proposed APReL-SSHI circuit and the conventional ReL-SSHI circuit. To illustrate the behavior of the VPM, the comparator output voltage V_{CMP} is also given. All simulations were conducted under identical input conditions with $V_{oc} = 8$ V. For the APReL-SSHI circuit, the NMOS switch activation threshold was set at $k = 0.5$. As illustrated in the main waveform, VPM enables V_{PT} to increase again after falling below a certain level, thereby extending the output voltage range. Compared to the 14.1 V maximum achieved by ReL-SSHI, the APReL-SSHI circuit reaches approximately 20 V. The four subplots in Fig. 8 highlight key operational stages of the APReL-SSHI circuit as it transitions between the ETM and VPM.

In stage 1 [Fig. 8(a)], V_{DC} initially increases and triggers the comparator to activate the NMOS switch. However, due to early-stage instability, the circuit may temporarily revert to ETM after just one VPM cycle. In stage 2 [Fig. 8(b)], the circuit enters a steady state where VPM and ETM alternate every two vibration cycles. During this stage, the energy on PT is transferred to the storage capacitor once every two cycles. As the output voltage V_{DC} continues to increase, V_{PT} can no longer accumulate to a sufficient level for charging C_r even after one VPM cycle. At this point, the APReL-SSHI enters stage 3 [Fig. 8(c)]. In this stage, the circuit operates in VPM for two cycles, followed by ETM for one cycle within every three vibration cycles. Consequently, energy is transferred to the storage capacitor once every three cycles. In stage 4 [Fig. 8(d)], V_{DC} reaches a level that keeps the NMOS switch continuously on during Q_2 conduction. The circuit then operates almost entirely in VPM, and the energy harvested each half-cycle is primarily used to compensate for system losses.

Fig. 9 shows the simulated output voltage of the APReL-SSHI circuit under varying values of k, with V_{oc} fixed at 8 V. For comparison, the output characteristics of the ReL-SSHI under the same input conditions are also shown. As k increases from 0.4 to 0.7, the output voltage of APReL-SSHI increases from 16.1 to 28.2 V. Theoretically, when k approaches 1, the circuit may reach a maximum output voltage close to the V_{PT} peak of approximately 40 V. However, beyond a certain point, expanding the voltage range further provides diminishing returns in power output. Therefore, k should be selected to balance range extension with output power efficiency.

V. Experiment Verification

A. Experimental Setup

To validate the theoretical and simulation results, we constructed an experimental test bench consisting of a signal generator, a power amplifier, a shaker, a piezoelectric transducer (PT), an oscilloscope, and the proposed APReL-SSHI circuit, as shown in Fig. 10. The PT used is the MIDE PPA-2011, featuring a parasitic capacitance of 190 nF, with one end mounted on the shaker. The signal generator determines the vibration frequency, while the power amplifier provides adjustable vibration amplitude.

By tuning the signal generator under fixed amplifier settings, the resonant frequency of the PT was determined to be approximately 32 Hz, corresponding to the point of maximum open-circuit voltage. The APReL-SSHI prototype was implemented using 2N3906 and 2N3904 BJTs (for PNP and NPN, respectively), an SS34 Schottky diode (D_1), a 1N4148 diode (D_2), an NZX3V9C Zener diode (D_3), a 47 μF electrolytic storage capacitor (C_r), two ceramic capacitors ($C_1 = 1.5$ nF, $C_2 = 1$ nF), and a Bourns RLB9012 inductor (15 mH, internal resistance 48.9 Ω). The LDO used was the S-812C52AY-Z2-U (fixed 5.2 V output), the comparator was the MCP6547, and the MOSFET switch was 2N7000TA.

B. Measurement Methodology

To evaluate the circuit performance, both the output voltage range and the output power across various voltage levels were measured. To obtain the voltage range, only the storage capacitor C_r was connected as the load, allowing the output voltage V_{DC} to rise naturally over time. The steady-state value of this curve represents the maximum output voltage of the system.

To measure the output power at specific voltage levels, a variable resistor R_r was connected in parallel with C_r. By adjusting

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R_r, the circuit was stabilized at different V_{DC} values, and the corresponding output power was computed using $P = V_r^2/R_r$.

To ensure fair and comparable evaluation across various interface circuits, we employed normalization metrics defined in [32], accounting for variations in C_p, vibration frequency f, and open-circuit voltage V_{oc}. These metrics include

$$\begin{cases} \text{FoM} = \frac{P_{\text{peak}}}{fC_pV_{\text{oc}}^2}, \\ \text{BW}_\rho = \frac{(V_{DC,\text{high}} - V_{DC,\text{low}})}{V_{\text{oc}}}, \\ \text{RoI}_\rho = \frac{S_{\text{RoI}_\rho}}{fC_pV_{\text{oc}}^3} = 0.5\,(1+\rho)\cdot \text{FoM}\cdot \text{BW}_\rho. \end{cases} \tag{29}$$

Here, FoM, BW_ρ, and RoI_ρ represent the normalized maximum output power, ORVR, and the corresponding region of interest, respectively. A high-performance interface circuit should perform well across all three.

C. Experimental Results and Analysis

Fig. 11 presents the measured transient waveforms of V_{PT}, V_{DC}, and V_{CMP} during the charging of C_r, comparing cases with and without voltage piling-up mode (VPM). Without VPM (Fig. 11(a)), the waveform closely resembles that of a ReL-SSHI circuit, with V_{PT} gradually decreasing as V_{DC} increases. When V_{DC} reaches 13.2 V, energy transfer halts.

When VPM is enabled (Fig. 11(b)), the output voltage range extends to 17.6 V. Initially, the VPM is triggered at $V_{DC} > kV_{PT}$ with $k = 0.55$. To visually demonstrate the influence of the variation of k on the output voltage range, k was manually adjusted from 0.55 to 0.65 when V_{DC} exceeded 14 V. It can be clearly observed that V_{DC} increases significantly as k value increased, thereby enabling further expansion of the output voltage range. Throughout the process, the circuit gradually requires from one to multiple VPM cycles to sufficiently raise V_{PT} for energy transfer, eventually reaching a state of continuous flipping with minimal net transfer to C_r. As the test waveforms for the individual cases of $k = 0.55$ and $k = 0.65$ are similar to that shown in Fig. 11(b), they are not repeated here. The corresponding detailed test curves will be presented in Figs. 13 and 14.

Fig. 12 presents the transient waveform of the APReL-SSHI circuit that transitions from stage 2 to stage 3. From the waveforms during the PT charging C_r phases in both stages, we observe that after V_{PT} flips to approximately 7 V through *LC* resonance relative to V_{DC}, the VPM immediately drives V_{PT} to flip again to a negative voltage. This action prevents the energy loss that would otherwise occur if V_{PT} had to first discharge from 7 to 0 V during the negative half-cycle before subsequent charging. In addition, it can be observed in stage 3 that after two cycles of VPM operation, the peak V_{PT} stabilizes at approximately 28 V with negligible further improvement in the third cycle, representing the practical maximum achievable in this implementation. Compared to the around 40 V peak obtained in the simulations, this discrepancy stems from unmodeled losses in inversion efficiency in the physical circuit, including internal resistances of discrete components and parasitic resistances in interconnects, none of which are fully accounted for in the idealized simulation environment despite using components with matched specifications.

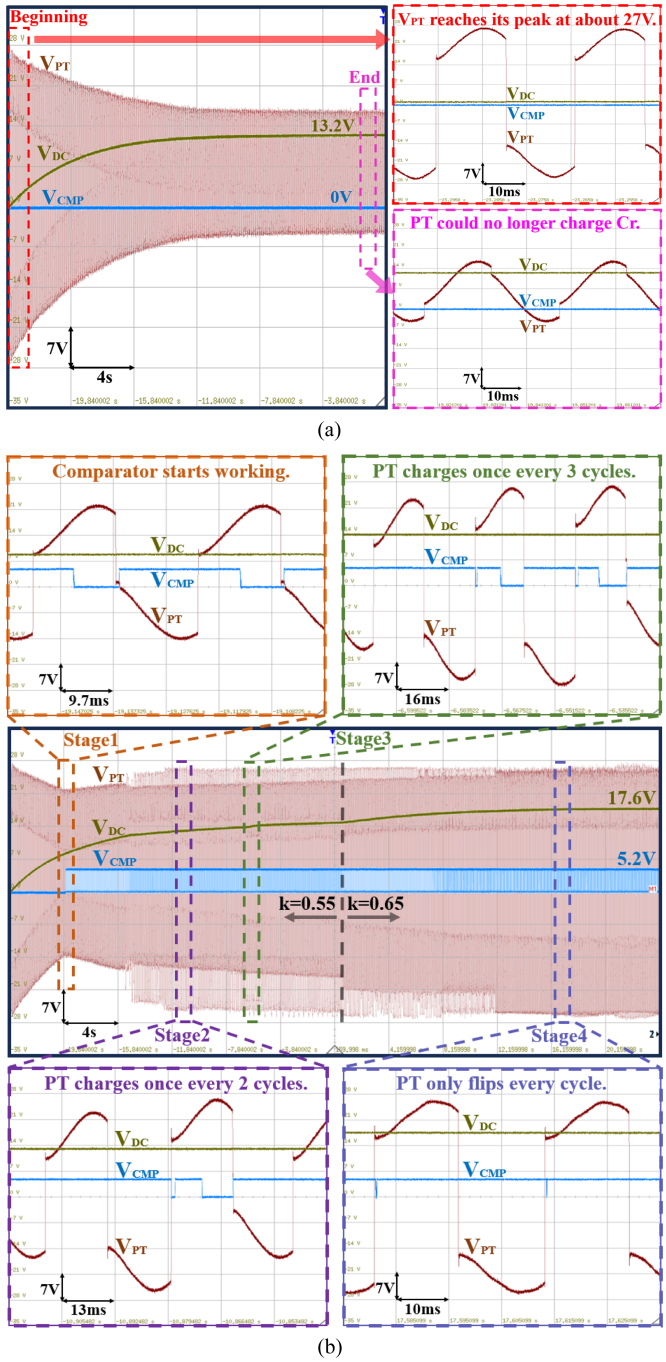


Fig. 11. Measured waveforms of V_{PT}, V_{DC}, and V_{CMP} during C_r charging. (a) Without Voltage Piling-Up Mode. (b) With Voltage Piling-Up Mode.

Fig. 13 shows the simulated and experimental output power curves of the proposed APReL-SSHI circuit under $V_{oc} = 8$ V, in comparison with those of the conventional ReL-SSHI circuit. By tuning the parameter k, VPM in the APReL-SSHI circuit is triggered when the output power drops to approximately $0.9P_{peak}$ or $0.8P_{peak}$, resulting in two distinct operational curves.

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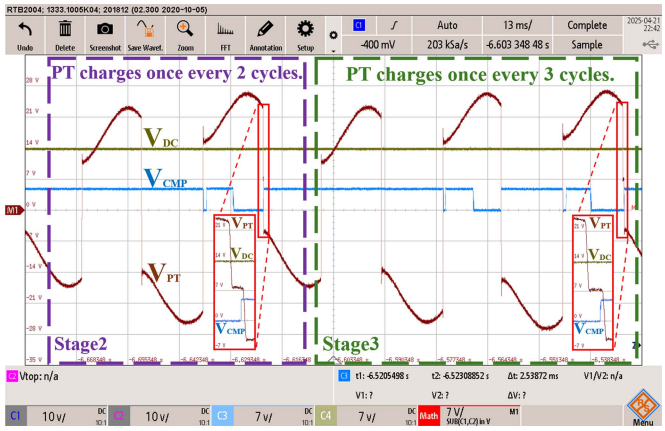


Fig. 12. Transient experimental waveform of V_{PT}, V_{DC} and V_{CMP} from stage 2 to stage 3.

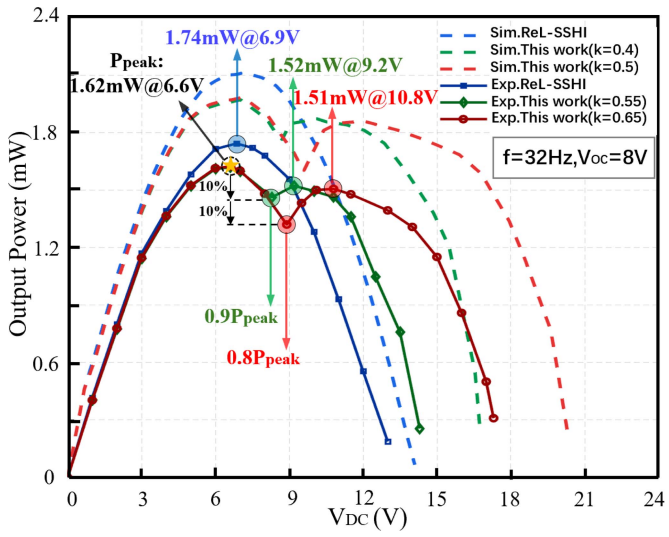


Fig. 13. Power vs V_{DC} for ReL-SSHI and APReL-SSHI under different switching time.(Sim:Simulation; Exp:Experimental).

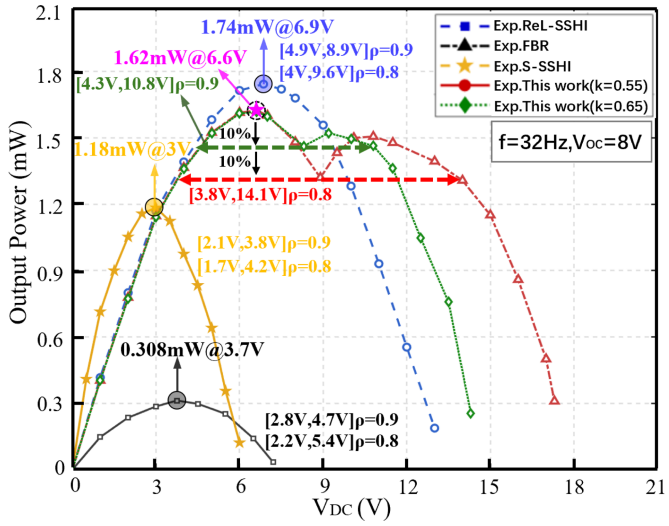


Fig. 14. Power vs V_{DC} for FBR, S-SSHI, ReL-SSHI and the proposed APReL-SSHI when $V_{oc} = 8V$. (Exp:Experimental).

Although the APReL-SSHI circuit exhibits a slight reduction in peak output power compared to the ReL-SSHI circuit, its ORVR is significantly extended due to the VPM mechanism. Since ReL-SSHI originates from the S-SSHI topology, it inherently suffers from a trade-off between high P_{peak} and limited ORVR. The proposed APReL-SSHI architecture overcomes this limitation by providing a better balance between output power and voltage adaptability.

Notably, both APReL-SSHI curves display a secondary power peak at roughly 94% of P_{peak}, located at a higher output voltage. This secondary peak shifts rightward as k increases, corresponding to a later activation of VPM. This behavior enables the circuit to maintain near-optimal power levels across a broad voltage range through simple adjustment of a resistor that sets k. As illustrated in the figure, this extended operating range surpasses the typical 6.6–10.8 V reference window.

In conventional systems, AC–DC rectifiers are followed by DC–DC converters with MPPT control to maintain operation near the maximum power point, incurring additional losses. In contrast, APReL-SSHI achieves similar functionality through passive k tuning alone, eliminating the need for extra power-processing stages and their associated energy overhead.

Finally, the k values required to initiate VPM at $0.9P_{peak}$ or $0.8P_{peak}$ differ between simulation and experiment. This discrepancy is due to reduced practical voltage inversion efficiency in the experimental circuit, arising from parasitic resistances and component mismatches that affect the achievable V_{PT} peak and thus shift the VPM activation threshold.

Fig. 14 presents the experimentally measured output power curves of four interface circuits: FBR, S-SSHI, ReL-SSHI, and the proposed APReL-SSHI. Based on the normalized performance metrics in (29), the APReL-SSHI achieves a maximum output power that is 5.27 times higher than FBR and 1.37 times higher than S-SSHI. When the coefficient ρ is set to 0.9, the corresponding BW0.9 values for APReL-SSHI, ReL-SSHI, S-SSHI, and FBR are 0.81, 0.50, 0.21, and 0.24, respectively. This indicates that APReL-SSHI improves the ORVR by factors of 1.62, 3.86, and 3.38 relative to ReL-SSHI, S-SSHI, and FBR. The RoI0.9 values follow a similar trend, measured as 3.22 for APReL-SSHI, compared to 2.12, 0.60, and 0.18 for ReL-SSHI, S-SSHI, and FBR, respectively.

When ρ is set to 0.8, the BW0.8 values increase to 1.29 (APReL-SSHI), 0.70 (ReL-SSHI), 0.31 (S-SSHI), and 0.40 (FBR), while the corresponding RoI0.8 values become 4.86, 2.82, 0.85, and 0.29. In summary, the APReL-SSHI achieves a 4.16× wider ORVR and a 5.71× higher RoI compared to S-SSHI, clearly demonstrating its substantial performance advantages in both voltage adaptability and energy extraction efficiency.

D. Comparison and Discussion

Table I provides a comparative summary of the proposed APReL-SSHI circuit against several state-of-the-art energy harvesting interface circuits. First, we examine the normalized region of interest (RoI), the metric that comprehensively reflects the tradeoff between the ORVR and the peak output power. As

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TABLE I
PERFORMANCE COMPARISON

Circuit	TPEL2019 [35]	TPEL2021 [32]	TPEL2021 [15]	TPEL2022 [36]	TPEL2024 [21]	TPEL2024 [37]	TIE2025 [18]	This work
PT	PT-5A	PPA-2011	PPA-1014	PPA-2011	PPA-2011	PT-5H	PPA-1001	PPA-2011
C_P (nF)	28.42	190	41	170	190	80	100	190
Technology	Discrete	Discrete	Discrete	Discrete	Discrete	Discrete	Discrete	Discrete
Rectifier Scheme	P-S3BF	Hybrid	ReL-SSHI	P-SSHI	ReL-SECEI	Hybrid	Hybrid	APReL-SSHI
Circuit Complexity	Complicated	Moderate	Simple	Moderate	Simple	Moderate	Moderate	Moderate
Self Powered	NO	YES	YES	YES	YES	YES	YES	YES
Inductor (mH)	47	2.21	50	1.56	4.7	10	10	15
$P_{out,max}/P_{FBR,max}$	3.88	3.98	5.9	3.22	4.2	5.15	3.61	5.27
Frequency (Hz)	24.9	18	18.6	77.5	19	30.5	19	32
$V_{oc,org}(V)$	15	6	4-8	3.9-5.8	2-6	5.7-6.2	5.1-6.2	8
FoM (Norm. P_{peak})	2.96*	2.27	4.92*	1.99*	3.09*	4.19*	2.82	4.18
$\mathrm{BW}_{\rho=0.9}$(Norm. ORVR)	2.45*	0.55	0.56*	1.28*	1.25*	0.47*	0.65	0.81
$\mathrm{RoI}_{\rho=0.9}$(Norm. S_{RoI_ρ})	6.88*	1.19	2.62*	2.42*	3.67*	1.87*	1.73	3.22
$\mathrm{BW}_{\rho=0.8}$(Norm. ORVR)	3.8*	0.72*	0.73*	2.07*	1.99*	0.77*	0.82*	1.29
$\mathrm{RoI}_{\rho=0.8}$(Norm. S_{RoI_ρ})	10.12*	1.47*	3.23*	3.7*	5.53*	2.9*	2.08*	4.85

(*) Calculated using the provided data and graphs of the above papers based on Equation (29).

shown in Table I, regardless of whether ρ is set to 0.9 or 0.8, the RoI of the proposed APReL-SSHI circuit surpasses that of most other counterparts, demonstrating its superior balance between maximum power extraction and output voltage flexibility.

Only the circuits reported in [21] and [35] surpass the proposed APReL-SSHI in terms of RoI, however, both exhibit certain disadvantages compared with our design. For the design in [21], it is an improved circuit based on the SECE principle, which grants a high ORVR. However, its higher RoI stems from its higher electrical quality factor Q compared to our circuit, reaching 7.9. The lower Q leads to reduced flipping efficiency, ultimately affecting both ORVR and maximum output power. As for the circuit in [35], it is an enhanced version of the P-SSHI topology, substantially widening the ORVR. Nevertheless, this design requires multiple switches and relies on additional controllers for precise digital control, while also lacking self-starting capability, making it potentially less practical than our proposed circuit.

Next, we separately analyze how the proposed APReL-SSHI performs in peak output power and ORVR compared with the other designs listed in Table I. In terms of peak output power, only the designs in [15] and [37] exhibit slightly higher normalized figures-of-merit (FoM), with improvements of no more than 1.18×. This is primarily due to enhancements derived from their S-SSHI-based architectures. However, when examining the normalized optimal rectified voltage range (BW), particularly $\mathrm{BW}_{0.8}$, the proposed APReL-SSHI achieves at least 1.68× improvement over these designs, indicating its significantly broader voltage adaptability, or better ORVR. Focusing solely on the ORVR metric, the designs reported in [21], [35], and [36] exhibit higher BW than APReL-SSHI. The designs in [21] and [35] have already been analyzed. As for the circuit in [35], it exhibits a much lower FoM, which ultimately results in inferior overall performance compared with the APReL-SSHI.

As for the remaining designs in [32] and [18], none outperform ours across all three metrics, further validating that our circuit achieves superior improvements in both maximum output power and ORVR.

VI. CONCLUSION

This work introduces a novel self-powered APReL-SSHI interface for piezoelectric energy harvesting. Building upon the ReL-SSHI topology through architectural advancement, the proposed APReL-SSHI circuit effectively overcomes its fundamental bottleneck of a narrow ORVR by introducing an ingenious voltage piling-up mechanism. This innovation enables significant expansion of the ORVR while preserving competitive maximum output power, ultimately achieving a superior tradeoff between energy extraction efficiency and operational voltage adaptability. Additionally, the APReL-SSHI circuit introduces the capability to generate a secondary power peak at output voltages beyond the conventional MPP, maintaining approximately 94% of the peak power. The location of this secondary peak can be tuned through simple circuit-level adjustments without modifying input conditions, enabling efficient power delivery across a wide range of load voltages—without the need for dedicated MPPT controllers. Theoretical analysis, circuit simulations, and experimental measurements consistently confirm the enhanced performance, wide operating range, and practical versatility of the APReL-SSHI circuit.

REFERENCES

[1] D. Newell and M. Duffy, "Review of power conversion and energy management for low-power, low-voltage energy harvesting powered wireless sensors," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9794–9805, Oct. 2019.
[2] S. Ghandi, M. Al Janaideh, and L. Zhang, "State of the art on power conditioning for piezoelectric energy harvesters," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3724–3737, Mar. 2024.
[3] Y. Peng et al., "Investigation of frequency-up conversion effect on the performance improvement of stack-based piezoelectric generators," *Renewable Energy*, vol. 172, pp. 551–563, 2021.
[4] T. Ruan, Z. J. Chew, and M. Zhu, "Energy-aware approaches for energy harvesting powered wireless sensor nodes," *IEEE Sensors J.*, vol. 17, no. 7, pp. 2165–2173, Apr. 2017.

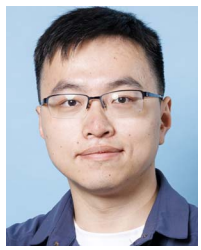
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[5] O. B. Akan, O. Cetinkaya, C. Koca, and M. Ozger, "Internet of Hybrid Energy Harvesting Things," *IEEE Internet Things J.*, vol. 5, no. 2, pp. 736–746, Apr. 2018.
[6] Z. Yang, S. Zhou, J. Zu, and D. Inman, "High-performance piezoelectric energy harvesters and their applications," *Joule*, vol. 2, no. 4, pp. 642–697, 2018.
[7] Z. Chen, Y. Xia, G. Shi, X. Wang, H. Xia, and Y. Ye, "Self-powered multi-input serial SSHI interface circuit with arbitrary phase difference for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9183–9192, Aug. 2021.
[8] M. B. Ammar, G. Bouattour, A. Bouhamed, S. Sahnoun, A. Fakhfakh, and O. Kanoun, "AC-DC single phase rectifiers for nanocomposite based flexible piezoelectric energy harvesters," in *Proc. 18th Int. Multi- Conf. Syst., Signals & Devices*, 2021, pp. 228–234.
[9] Z. J. Chew and M. Zhu, "Adaptive maximum power point finding using direct $V_{OC}/2$ tracking method with microwatt power consumption for energy harvesting," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8164–8173, Sep. 2018.
[10] G. A. Rincón-Mora and S. Yang, "Tiny piezoelectric harvesters: Principles, constraints, and power conversion," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 5, pp. 639–649, May 2016.
[11] Z. J. Chew and M. Zhu, "Adaptive self-configurable rectifier for extended operating range of piezoelectric energy harvesting," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 3267–3276, Apr. 2020.
[12] A. Badel, D. Guyomar, E. Lefeuvre, and C. Richard, "Efficiency enhancement of a piezoelectric energy harvesting device in pulsed operation by synchronous charge inversion," *J. Intell. Mater. Syst. Struct.*, vol. 16, no. 10, pp. 889–901, 2005.
[13] Z. Qiu, S. Maniyil, W. Peng, A. C. van der Ham, and S. Du, "A self-powered bipolar rectifierless series-sshi circuit with dual-polarity energy extraction for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 40, no. 10, pp. 15937–15948, Oct. 2025.
[14] Z. Chen, J. He, J. Liu, and Y. Xiong, "Switching delay in self-powered nonlinear piezoelectric vibration energy harvesting circuit: Mechanisms, effects, and solutions," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2427–2440, Mar. 2019.
[15] X. Wang et al., "A self-powered rectifier-less synchronized switch harvesting on inductor interface circuit for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9149–9159, Aug. 2021.
[16] Z. Long, P. Li, J. Chen, H. S.-H. Chung, and Z. Yang, "Self-powered single-inductor rectifier-less sshi array interface with the mppt technique for piezoelectric energy harvesting," *IEEE Trans. Ind. Electron.*, vol. 69, no. 10, pp. 10172–10181, Oct. 2022.
[17] Y.-W. Jeong, S.-J. Lee, and S.-U. Shin, "A scalable n-step equally split sshi rectifier for piezoelectric energy harvesting with low-q inductor," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3519–3529, Dec. 2023.
[18] X. Wang, L. Qian, X. Wang, G. Shi, and H. Xia, "Self-powered S-SSHI and SECE hybrid rectifier for multi-PZTs energy harvesting," *IEEE Trans. Ind. Electron.*, vol. 72, no. 5, pp. 4822–4832, May 2025.
[19] X. Yue and S. Du, "An adaptive two-mode bias-flip rectifier with lowered cold-startup voltage requirement for multiple piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 8283–8291, Jun. 2025.
[20] E. Lefeuvre, A. Badel, C. Richard, and D. Guyomar, "Piezoelectric energy harvesting device optimization by synchronous electric charge extraction," *J. Intell. Mater. Syst. Struct.*, vol. 16, no. 10, pp. 865–876, 2005.
[21] Z. Chen, Y. Xia, G. Shi, X. Wang, H. Xia, and Y. Ye, "A novel rectifierless synchronous electric charge extraction and inversion interface circuit for pe energy harvesters," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3749–3759, Mar. 2024.
[22] S. S. Sani, "A single-inductor self-powered SECE interface circuit for dynamic load multi-PZTS energy harvesting," *IET Power Electron.*, vol. 17, no. 15, pp. 2613–2630, 2024.
[23] C.-W. Chen, W. Z. Pranoto, H.-S. Chen, and W.-J. Wu, "A 0.25-μm HV-CMOS synchronous inversion and charge extraction interface circuit with a single inductor for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15707–15718, Dec. 2023.
[24] X. Wang et al., "Multi-input SECE based on buck structure for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3638–3642, Apr. 2021.
[25] J. Zheng and W. Wu, "A self-powered multi-input interface circuit for piezoelectric energy harvesting using SECE and one shared coupled inductor," in *Proc. IEEE 2nd Int. Power Electron. Appl., Symp.*, 2023, pp. 761–764.
[26] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct. 2017.
[27] X. Yue and S. Du, "A synchronized switch harvesting rectifier with reusable storage capacitors for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2597–2606, Sep. 2023.
[28] Z. Li et al., "Piezoelectric energy harvesting interface using self-bias-flip rectifier and switched-PEH DC–DC for MPPT," *IEEE J. Solid-State Circuits*, vol. 59, no. 7, pp. 2248–2259, Jul. 2024.
[29] L. G. Salem, "Analysis and optimization of switched-capacitor piezoelectric energy harvesting interface circuits," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 31, no. 9, pp. 1389–1402, Sep. 2023.
[30] X. Yue and S. Du, "Performance optimization of SSHC rectifiers for piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 70, no. 4, pp. 1560–1564, Apr. 2023.
[31] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanopower synchronous charge extractor ic for low-voltage piezoelectric energy harvesting with residual charge inversion," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1263–1274, Feb. 2016.
[32] H. Xia et al., "A self-powered S-SSHI and SECE hybrid rectifier for pe energy harvesters: Analysis and experiment," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1680–1692, Feb. 2021.
[33] X. Wang et al., "A novel MPPT technique based on the envelope extraction implemented with passive components for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12685–12693, Nov. 2021.
[34] E. Lefeuvre, A. Badel, C. Richard, L. Petit, and D. Guyomar, "A comparison between several vibration-powered piezoelectric generators for standalone systems," *Sensors Actuators A: Phys.*, vol. 126, no. 2, pp. 405–416, 2006.
[35] J. Liang, Y. Zhao, and K. Zhao, "Synchronized triple bias-flip interface circuit for piezoelectric energy harvesting enhancement," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 275–286, Jan. 2019.
[36] H. Xia et al., "Self-powered dual-inductor MI-PSSHI-VDR interface circuit for multi-PZTS energy harvesting," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3753–3762, Apr. 2022.
[37] X. Wang, L. Qian, X. Wang, G. Shi, H. Xia, and Z. Zhu, "A self-powered BF and S-SSHI hybrid rectifier for multi-PZTs energy harvesting," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 13828–13841, Oct. 2024.



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