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Ion Depletion Defects in RRAMs: Characterization, Modeling, and Test

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***Abstract*—The commercialization of resistive random access memories (RRAMs) has been invested in by many companies as an alternative to conventional memories. This necessitates a thorough comprehension of manufacturing defects to create high-quality, efficient test and diagnosis solutions that will facilitate high-volume production. This work presents the identification and characterization of a novel defect, called ion depletion (ID), utilizing silicon measurements. In the selected defective device, after excluding the first 100 unstable cycles, 14% of the remaining 836 cycles exhibit ID-defective high resistance state (HRS) degradation, while the low resistance state (LRS) remains unaffected. Furthermore, this unique defect is non-linear and inside the device itself; hence, the conventional defect and fault modeling, which relies on linear resistors beside the device, cannot be applied to model the ID defect. To tackle this issue, the device-aware (DA) defect modeling approach is used. A calibrated RRAM model representing the defective device is developed using measurement data to precisely characterize how the defect influences the electrical properties of the memory hardware. Subsequently, fault analysis is conducted based on the DA defect model, leading to the introduction of suitable fault models. These models demonstrate that the ID defect can trigger undefined state faults. Finally, dedicated test and diagnosis solutions specifically designed for the ID defect are proposed.**

***Index Terms*—Design-for-testability (DfT), device-aware (DA) defect model, fault model, intermittent behavior, resistive random access memories (RRAM), test.**

I. Introduction

RESISTIVE random access memory (RRAM) is a promising technology for next-generation non-volatile memory technologies and new computing paradigms, offering benefits such as 3-D stackability, low access latency, and energy efficiency [1], [2]. Although they have many advantages, the immaturity of the manufacturing process poses major obstacles to the mass production of RRAM, especially as devices scale down [3], [4], [5]. Defects and non-idealities in device characteristics arising during the fabrication process, along with their effects on the final product quality, are widely acknowledged as major challenges [3], [5], [6], [7], [8], [9]. Thus, high-quality yet efficient manufacturing test solutions are required to ensure the quality of products being shipped to end customers. The manufacturing of RRAM involves two stages: front-end-of-line (FEOL) and back-end-of-line (BEOL), both of which may result in fabrication defects [10]. Furthermore, RRAM manufacturing consists of additional processes and the use of new materials, which can cause new failure mechanisms [10]. The defects associated with RRAM are typically complicated and cannot be reliably detected through standard testing for current mainstream memory systems. Hence, it is essential to comprehend the unique RRAM defects and precisely develop models to ensure the high-quality production of RRAMs.

Defect, fault models, and test solutions for RRAMs are attracting a lot of attention. In 2009, coupling faults were investigated by modeling bridge defects [11]. In 2013, a sneak-path testing method was proposed to optimize test time [12]. Chen et al. [13] identified a dynamic write disturbance fault, and a March test to detect it. Mozaffari et al. [14] offered a test method to detect the undefined state faults in RRAMs during the production testing phase. Liu et al. [4] studied a 3-D hybrid RRAM array and designed the design-for-testability (DfT) scheme for it. Nevertheless, all these works only focus on interconnect and contact defects and employ a *linear resistor* in the surrounding interconnections as defect models. Those unique defects, such as the ID, occur inside the RRAM device itself and exhibit the naturally *non-linear*, which cannot be accurately modeled by inappropriate *linear resistors*. To overcome the constraints of the traditional RRAM test method, the "device-aware test (DAT)" method was introduced [8]. The DAT approach effectively models physical defects, facilitating the analysis of realistic fault models and the design of developed test solutions. The effectiveness of this approach has been shown in addressing certain defects in RRAMs, such as intermittent undefined state fault (IUSF) [15]. Besides, unique defects such as IUSF and ID exhibit *intermittent behaviors*, introducing challenges for defect modeling and test development. Furthermore, given the early stages of RRAM technology, it is still imperative to identify, comprehend, and model unique defects caused by device miniaturization or novel materials to provide the most effective testing solutions.

In this article, ion depletion (ID) defects, unique RRAM defects, are investigated and characterized based on silicon measurements. The defect results in intermittent, undefined state faults during the RESET process. In this article, we provide deeper characterizations and analysis of stochasticity compared with [16]. Based on measurements, the DAT defect model has been extended and integrated with *intermittent behavior*. Moreover, the proposed test solution has

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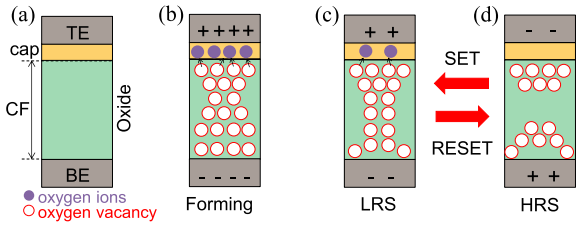


Fig. 1. CF development stages. (a) RRAM structure. (b) Forming process. (c) SET operation. (d) RESET operation.

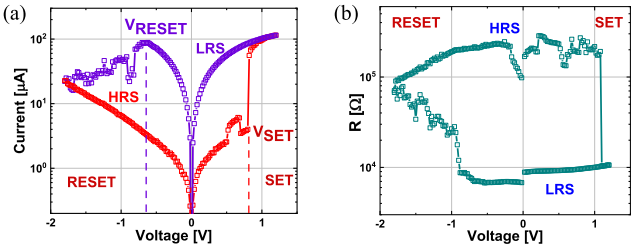


Fig. 2. Electrical switching behavior of RRAM. (a) I–V characteristics under BS switching and (b) R–V characteristics under BS switching.

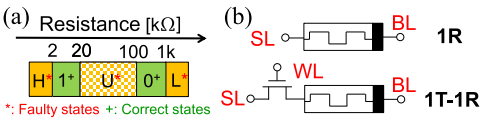


Fig. 3. Overview of RRAM devices, adapted from [16]. (a) Distinct resistance states. (b) Cell architectures including 1R and 1T–1R.

been validated with process variation analysis. The primary contributions of this article are as follows.

1) Identify the ID defect based on silicon measurements.
2) Comprehensive characterization of RRAM devices exhibiting the ID defect, including an in-depth analysis of the underlying physics and its reliability issues across multiple cycles and devices.
3) Develop the device-aware (DA) defect model for the ID defect, which incorporates the intermittent behavior, and calibrate it with measurements to accurately model this defect.
4) Utilize the DA defect model to develop appropriate fault models and subsequently optimal test solutions, validated through simulations. The proposed solutions are optimized for robustness against process variations, ensuring practical applicability and reliability.

The rest of this article is structured as follows. Section II provides an overview of the background on RRAM technology. Section III establishes experimental evidence, characterization, and underlying potential causes of the ID defect. Section IV illustrates the failure of the conventional defect models (linear resistors) and proposes the DA defect model that properly depicts the faulty behavior of a defective RRAM device. The fault modeling and analysis based on this model are presented in Section V. Section VI introduces the corresponding test strategies tailored for the ID defect. Lastly, Section VII summarizes the key findings of the work.

II. Background

A. RRAM Device and Switching Process

The RRAM architecture leverages either oxide-based (OxRAM) or conductive-bridge (CBRAM) memristive elements for data storage [1]. Fig. 1(a) presents a schematic of its metal–insulator–metal (MIM) structure [1], [6], [10]. The device stack typically includes a central metal oxide layer (e.g., TiO_x, HfO_x), capped with an additional layer such as Hf, Ti, or Ta, and is sandwiched between a top electrode (TE) and a bottom electrode (BE) [2], [17].

The bipolar switching (BS) behavior arises from the formation and rupture of conductive filaments (CFs), which are driven by the migration of *oxygen ions* [1], [2]. The forming process is initiated by applying a sufficiently high positive voltage (V_{forming}) across the top and bottom electrodes (TE and BE), which breaks the metal–oxygen ionic bonds within the insulating layer [1]. This voltage drives negatively charged oxygen ions (O^{2-}) away from the lattice, leading to their accumulation at the cap/oxide interface. As a result, positively charged oxygen vacancies (OVs) form, and a *CF* emerges within the insulator between the two electrodes due to this localized deficiency, as depicted in Fig. 1(b). The switching direction is determined by both the polarity and the magnitude of the applied voltage (V_{SET} and V_{RESET}) [1]. By tuning the programming voltage applied to the RRAM cell, the device can transition between different resistance states. When the positive voltage at the TE side (V_{TE}) exceeds a threshold level ($V_{\text{TE}} \geq V_{\text{SET}}$), additional OVs are created, extending the CF, which marks the SET operation, with the resulting resistance referred to as R_{SET} [18], [19], as illustrated in Fig. 1(c). Conversely, during a RESET operation, a negative voltage is applied such that $V_{\text{TE}} \leq V_{\text{RESET}}$, which causes a portion of the O^{2-} to migrate back into the oxide layer, thereby disrupting the filament and increasing the resistance, as illustrated in Fig. 1(d) [18], [19]. The resistance in RESET is denoted as R_{RESET}. Fig. 2(a) shows the I_{TE}-V_{TE} curve during the switching process. Fig. 2(b) shows the corresponding R-V_{TE} curve. The current–voltage (I_{TE}–V_{TE}) hysteresis curve during the switching process is illustrated in Fig. 2(a). As shown in Fig. 2(a), reversing the voltage polarity enables both SET and RESET operations. The resulting resistance state is primarily determined by the length of the CF within the insulating layer between the two electrodes.

The (binary) RRAM cell can be categorized into five distinct resistance levels as the overall resistance increases [see Fig. 3(a)] [8]: 1) a faulty state with abnormally high conductance, denoted as "H"; 2) the normal low resistance state (LRS), labeled as "1"; 3) a known defective condition in the intermediate resistance range between LRS and HRS, represented as the "U" state; 4) the expected high resistance state (HRS), indicated as "0"; and 5) a low-conductance faulty state, denoted as "L."

B. RRAM Cell Design and Array

RRAM is typically provided in applications in the form of array designs. Two commonly adopted RRAM cell configurations are one-resistor (1R) and one-transistor–1R (1T–1R) structures, as shown in Fig. 3(b) [1]. In this study, the 1T–1R architecture is utilized to implement a memory crossbar array, as depicted in Fig. 4. The memory array includes bit lines (BLs), word lines (WLs), and select lines (SLs), which are responsible for controlling access to the cells. The WL manages transistor activation, allowing specific memory cells to be targeted. To enable data writing, appropriate voltage levels are applied to the BL and SL lines. For read operations, a standard voltage-mode sense amplifier (SA) [20] is used, as illustrated

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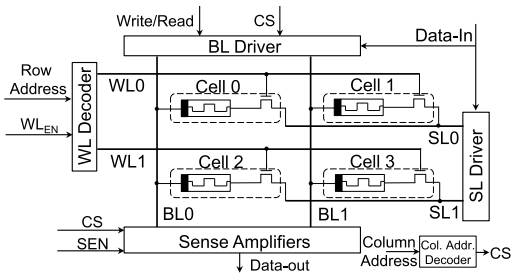


Fig. 4. Schematic of 1T–1R circuit architecture.

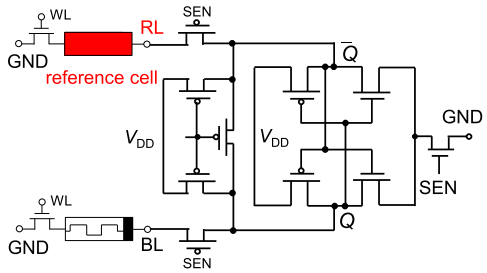


Fig. 5. SA circuit schematic [20].

in Fig. 5. The SA operates in two distinct phases, which are governed by the sense enable (SEN) signal. When SEN is "0," the output nodes Q and $\overline{Q}$ are initially pre-charged to VDD. Once SEN is set to "1," these nodes begin to discharge. During the sensing phase, the SA determines the cell's resistance level by comparing the discharge rate against that of a reference path. This comparison is performed by observing the behavior of the BL and the reference line (RL), each connected to their respective cells. Typically, the reference cell is programmed to a resistance value midway between the HRS and LRS states. The final voltages of discharged nodes Q and $\overline{Q}$ are interpreted as the output data.

III. Defect Characterizations of ID

This section explores the characteristics of both defect-free and ID-defective RRAM cells, based on results from silicon-level experiments. Beyond the representative observations reported in [16], this journal version further extends the characterization with multi-cycle, multi-device, and V_{stop}-dependent measurements, together with additional statistical analyses. A small subset of devices was found to exhibit normal SET behavior but failed to transition into the expected HRS during the RESET phase. This anomaly is attributed to the ID defect, which we identify as a primary factor contributing to incomplete RESET behavior and reduced HRS levels. To investigate this phenomenon, we present comparative measurements between a typical defect-free device and one exhibiting ID-defective behavior. The analysis highlights key differences in electrical performance and switching reliability. Finally, a brief summary is provided, outlining the defect characteristics and discussing possible underlying physical mechanisms.

A. Characterization

The electrical characteristics of a 7 × 7 1T–1R array, consisting of 49 BS RRAM devices, were measured across 936 RESET-SET cycles on a single wafer [15]. The device is HfO 2-based 1T1R array fabricated at ST Microelectronics

TABLE I

Occurrence Probability of ID (P_{ID}) in % and Maximal Duration Suffering From ID ($D_{\max}$), During 536 Cycles

		WL 0	WL 1	WL 2	WL 3	WL 4	WL 5	WL 6
BL 0	P_{ID}	4.41	0	0	0.74	15.44	0	0.74
	$D_{\max}$	1	0	0	1	3	0	1
BL 1	P_{ID}	0	1.47	0	1.47	1.47	0.74	0
	$D_{\max}$	0	1	0	1	1	1	0
BL 2	P_{ID}	0	0	0	0	0	1.47	0
	$D_{\max}$	0	0	0	0	0	1	0
BL 3	P_{ID}	0	9.56	0	0	13.24	11.03	20.59
	$D_{\max}$	0	2	0	0	4	1	3
BL 4	P_{ID}	0	0.74	0	0	0.74	0.74	8.82
	$D_{\max}$	0	1	0	0	1	1	1
BL 5	P_{ID}	0	2.94	2.94	0.74	0	18.38	5.15
	$D_{\max}$	0	1	1	1	0	3	1
BL 6	P_{ID}	4.41	0.74	0	0	0	0	0.74
	$D_{\max}$	1	1	0	0	0	0	1

130 nm technology. (BE/oxide/cap/TE) = (TiN/10 nm HfO 2/10 nm Ti/TiN) is the stack of the bipolar device. One ST Microelectronics high-voltage thick oxide transistor (W = 0.8 μm, L = 0.5 μm) is connected in series to regulate the current flowing through the device. The Keysight B1500 semiconductor parameter analyzer is connected to the measured 1T–1R device by a probe card, which is embedded in an 8-in wafer. A 1 ms DC staircase voltage sweep with a 20 mV step is applied across BL and SL of the measured device for the measurement configuration, and the current flowing through the device is measured. V_{SET}, V_{RESET}, R_{SET}, and R_{RESET} are four critical electrical parameters that demonstrate the device's switching behavior. From the measurement data, a device with a nominally defect-free switching is bipolar, where LRS is defined with $R_{\text{SET}} < 20$ kΩ and HRS with 100 kΩ < R_{RESET} < 1 MΩ. The remaining range [20, 100 kΩ] is defined as an undefined state ("U").

Upon examining the measurement data, it is evident that certain devices have a defective RESET process. Specifically, their resistance states remain at "U" regardless of the magnitude of the RESET voltage amplitude. The ID defect is characterized by comparing the typical measured 1T–1R log *(I)*–*V* and log *(R)*–*V* curves of defect-free and defective devices in the RESET process, as illustrated in Fig. 6(a) and (b). V_{TE} is applied in a sweeping motion from 0 to −1.8 V (①,②) and back to 0 V (③). The gradual RESET process with a significant current fluctuation is observed from our measurements, which can be explained by the thermodynamic process of the migration of Vo [19]. The RESET switch in the defect-free device starts at −0.7 V with a constant LRS and terminates at a very low current, approximately 20 μA. An evident transition is also observed at −0.7 V during the RESET switching of a defective device. Nevertheless, this transition fails at ② and remains in the "U" state. The current through the device gradually decreases as the RESET voltage decreases further, but it remains greater than the typical RESET current (approximately 50 μA). The HRS of both devices remains nearly constant (③) as the applied negative voltage returns to 0 V. The following SET processes of defective devices are consistent with the defect-free devices.

Next, we characterize the ID defect in multiple RESET-SET cycles. In the initial cycles, devices exhibit erratic resistance states, a phenomenon also reported in [21]. Thus, we skip the initial cycles to obtain stable measurements. Table I summarizes the occurrence probability (P_{ID}) of the ID defect in the measured devices (using the WL and BL to indicate them). The table lists the percentage of cycles

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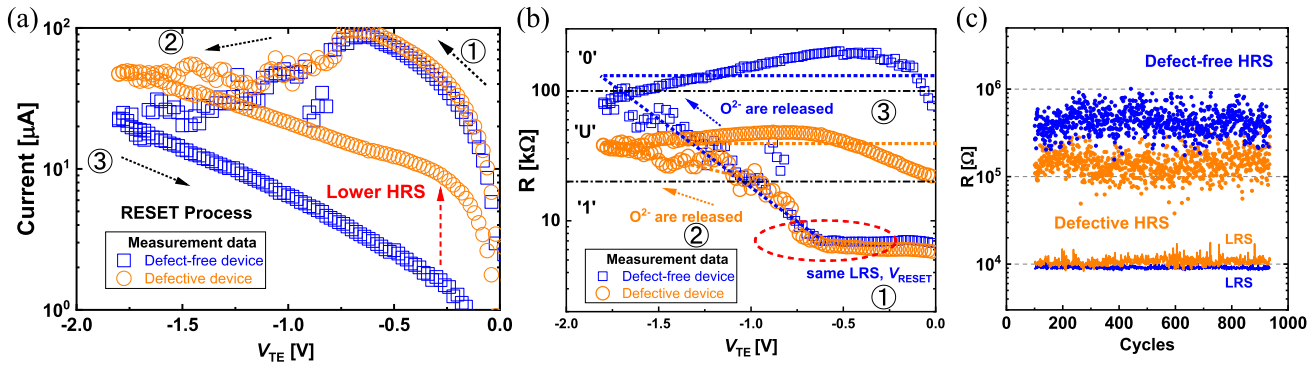


Fig. 6. Comparison of electrical behavior between defect-free (WL = 5, BL = 0) and defective (WL = 5, BL = 3) devices, adapted from [16]. (a) Measured current–voltage characteristics. (b) Logarithmic resistance–voltage curves. (c) Statistical distribution of measured R_{RESET} and R_{SET} across 836 cycles.

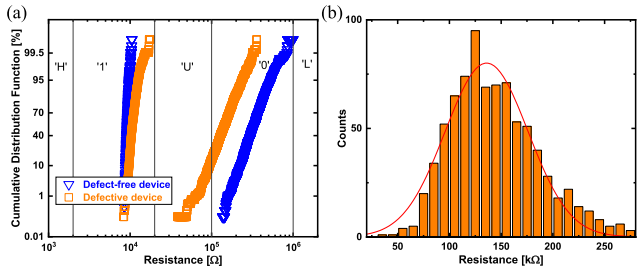


Fig. 7. Resistance distribution. (a) Measured R_{RESET} and R_{SET} of defect-free and defective devices. (b) Histogram of measured R_{RESET} distribution.

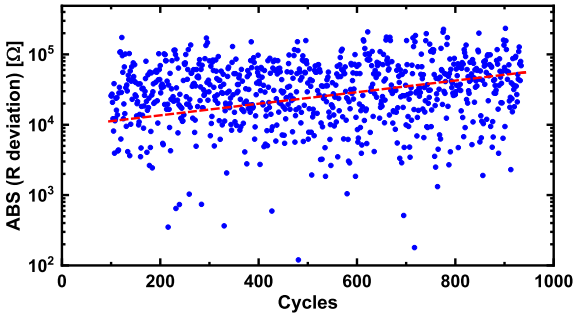


Fig. 8. $|R_{\mathrm{RESET}}|$ deviation of the defective device as cycle increases.

in which ID occurs, given a total of 536 cycles after stabilization. Besides, the table counts the maximal duration ($D_{\max}$) of the undesired "U" state, expressing the maximal cycle the ID defect can last in 536 cycles for each device. For example, if the ID first occurs in cycles 100, 101, and 102, and later in cycle 110, then $P_{\mathrm{ID}} = 4/536 = 0.74\%$ and $D_{\max} = 3$ cycles. The table indicates that the ID defect is present in 25 devices, with a maximum duration of four cycles and a probability of up to 20.59% of the cycles. Additionally, the ON/OFF resistance window is illustrated in Fig. 6(c) as a function of cycles for defect-free (WL = 5, BL = 0) and defective devices (WL = 5, BL = 3). This defective device only exhibits erratic resistance states in the first 100 cycles and is selected to analyze the ID defect in this article. 836 cycles per device that skip the first hundred have been collected. Following the initial few cycles, the resistance values exhibit minimal fluctuations. Fig. 7(a) shows the cumulative distributions of resistance for the defect-free and defective RRAM devices. The HRS distribution exhibits a more pronounced spread compared to the LRS, a finding that has also been reported in other articles [22]. Fig. 7(b) shows the histogram of defective measured R_{RESET} distribution, which follows the normal distribution. From Fig. 7, 14% of RESET-SET cycles demonstrate the ID-defective HRS degradation. Hence, the defect displays *intermittent* behavior, which poses a significant concern for RRAM devices. Fig. 8 shows the correlation between the absolute value of R_{RESET} deviation and the increase in the number of cycles, plotted on a logarithmic scale. Again, we skip the first 100 cycles. The Pearson correlation coefficient of our 835 R_{RESET} deviation data is 0.162 (a Pearson correlation of 0 indicates no correlation), indicating a weak positive correlation coefficient. The p-value is $2.4 \cdot 10^{-6} < 0.05$, indicating statistical significance. The red dotted line shows that the deviation increases as the cycles increase. This correlation indicates that the ID defect is not only at time 0 due to the imperfect fabrication but also becomes stronger as the cycles increase. Hence, the ID defect probably raises concerns about reliability since the ID-defective device wears out and is irrecoverable.

Since both defective and defect-free devices show proper SET switching in the measurement data, we focus on the RESET behavior in the rest of the article.

B. Relevant Research and Underlying Physical Explanation

The concept of "ion depletion" was introduced by Chen et al. [23] to characterize the RRAM endurance degradation phenomenon that occurs as a result of a reduction in HRS. The irreversible switching behavior observed after 10^5 cycles was the physical mechanism of this RESET failure. In 2012, the impact of the SET/RESET pulse on device reliability was examined [24]. It was asserted that the use of overly strong SET pulses induces an excessive quantity of OV at the interface, resulting in HRS failure after 10^6 cycles. Following that, these two earlier investigations demonstrated that the voltage amplitude, rather than the stress duration, has a substantial impact on the O^{2-} drift. In 2015, the thin oxygen-scavenging metal layer was argued to fail to form an Ohmic contact by Schönhals et al. [25]. This failure occurs when the capping layer is unable to release a sufficient amount of O^{2-} to recombine the OV in the RESET process. In 2017, the HRS decrease was experimentally studied with the creation of rougher and thicker CFs following 10^4 switching cycles [26]. However, they all neglected to observe the HRS reduction caused by device defects during the initial hundreds of cycles, resulting in experimental results that were exclusively focused on endurance failures. In addition, they failed to establish a

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circuit-level defect model that would describe the degradation behavior of the HRS.

As discussed in Section II, the BS mechanism is governed by the movement of O^{2-}, which leads to the formation and rupture of CFs composed of OVs. This process is inherently stochastic in nature [18], [19]. During the SET phase, OVs are introduced into the oxide layer, while O^{2-} drifts toward the titanium capping layer, accumulating at the interface between Ti and HfO_2 [18], [19]. In the RESET stage, the CFs rupture near this interface as O^{2-} migrates back into the oxide and subsequently recombines with OVs under reverse bias conditions [18], [19]. Notably, both defect-free and ID-defective devices exhibit a nearly stable LRS, as shown in Fig. 6(b), even after multiple switching cycles. It suggests that the SET process generates an equal quantity of O^{2-}. The O^{2-} stored in the capping layer is necessary for the recombination of OV during the RESET process [18]. However, the oxygen reservoir of defective devices is depleted of O^{2-}. Only a limited amount O^{2-} can be released back to recombine the OV, resulting in an insufficient RESET, and hence a smaller resistance window as well as the reduced HRS. It is important to note that defect-free devices exhibit a slight decrease in HRS at low voltages (less than −1.5 V) in Fig. 6(b). This phenomenon can be attributed to the effect of tunneling leakage currents [19]. Conversely, defective devices continue to release a small fraction of insufficient O^{2-} at high voltages in order to recombine the CF.

As indicated by the measurement data presented above, ID is the likely cause of the defective RESET switching. The observed behavior is consistent with interface-related imperfections that increase oxygen trapping, thereby reducing the recombination rate between inadequate O^{2-} and OV [23], [24], [26]. Hence, the reduced recovery of OV due to inadequate nonlattice O^{2-} stored in the capping layer induces lower HRS. This interpretation is supported by prior device-level literature and by the consistency between those reports and our silicon observations. Since the present work does not include direct materials characterization of defective interfaces, the mechanism should be understood as a plausible physical explanation used to motivate the circuit-level defect model, rather than as a definitive materials-level verification. Fig. 9 graphically depicts the degradation mechanism of the HRS and four potential resistance states of the device during forming, RESET, and SET processes: 1) R_{fresh}, pristine RRAM devices with minimal OV before forming, have an extremely high initial resistance state [10]; 2) R_{SET}, O^{2-} and OV are generated in SET or forming process; 3) R_{RESET}, regular recombination between O^{2-} and OV results in the nominal HRS during the RESET of defect-free devices; and 4) R_{RESET}(defective), in the RESET of defective devices, less recombination of OV due to physical imperfections. As a result, the resistance values are as follows: $R_{\text{fresh}} > R_{\text{RESET}} > R_{\text{RESET}}(\text{defective}) > R_{\text{SET}}$.

To better investigate the physical reason for the defect, we performed weak RESET (sweep the V_{stop} at −1 V) and compared the measurements with those of regular RESET (V_{stop} at −1.8 V), as shown in Fig. 10. For each cycle, the measurements are obtained as follows: regular RESET sweep, regular SET sweep, and weak RESET sweep. Fig. 10(a) shows that as the voltage decreases from −1 to −1.8 V, the current slightly decreases since more recombination between O^{2-} and OV (i.e., higher R_{RESET}), which implies that the defect is affected by applied voltage. In Fig. 10(b), the R_{RESET} remains at a lower value at V_{stop} of −1 V than V_{stop} of −1.8 V, and the nearly constant R_{RESET} (V_{TE} from −1 to 0 V) shows the defect is permanent once it occurs in the cycle.

C. Related Fabrication Processes

The imperfections of the RRAM process have a significant impact on the test methods for its design. The RRAM defects are associated with its manufacturing process, and the defects that are introduced during each stage of the manufacturing process are unique. The general manufacturing process is illustrated in Fig. 11 [10], [27]. Transistors are initially assembled on the wafer in the FEOL, which is equivalent to conventional CMOS technology. Then, the metal layers are deposited in the BEOL. Ultimately, the CF is generated by employing a high forming voltage.

In this article, we assume that the following imprecise fabrication processes (represented in red font in Fig. 11) are associated with the characterized ID defect. These procedures may impact the interface imperfections, thereby affecting the depletion of generated O^{2-}.

1) Thickness Variations of Deposition: The capping layer is deposited at varying thicknesses. The stable BS is favored by the thicker capping layer due to its increased oxygen affinity and decreasing work function [25]. Conversely, a thin capping layer captures a significant quantity of O^{2-}, making it challenging to fill the CF, which denotes a blocking contact formed at the interface [25]. The optimization of the proper barrier height at the interface between the cap and oxide is also influenced by the oxide layer [18]. Enhanced stability of RESET has been observed in thicker oxide [18], [28].

2) Annealing Process: An appropriate annealing treatment may enhance the crystalline quality of the oxide bulk and raise the oxygen concentration in the capping layer [27], [29]. The switching performance of RRAM is shown to be correlated with variations in the concentration of hydroxyl groups [30]. Substantial dependency on annealing temperature is seen at HRS, as reported in [30]. The annealing temperature is also a determining factor in the surface roughness [30], [31], [32]. Therefore, the presence of nonuniform or unsuitable annealing temperatures might impact the interface activity, resulting in HRS degradation.

Considering the variability of the manufacturing process and the unpredictable nature of CF dissolving [22], the ID defect is not present on every device and every cycle (intermittent).

IV. DA Defect Modeling of ID

The structural RRAM test development method has three steps: defect modeling, fault modeling, and test development [8], [15]. This systematic approach relies on precise defect and fault modeling to provide superior test methods. Traditionally, RRAM defects are modeled as linear resistors (e.g., an open can occur owing to a poorly located contact and be modeled as an increased series resistance) that are linked in either parallel or series with the device to represent bridges, shorts, and opens [11], [12], [13]. Unfortunately, linear resistor models cannot properly describe the faulty behavior within the defective device itself [15]. For example, the ID defect is inside the device and causes a decrease of HRS in RESET. Thus, the defect only sensitizes specific faults according to the applied voltage, exhibiting the nonlinearity. Moreover, unique defects can be intermittent and are not guaranteed to occur in every cycle, which is insufficient to be modeled by linear resistors. To overcome the limitations, we propose the systematic DAT

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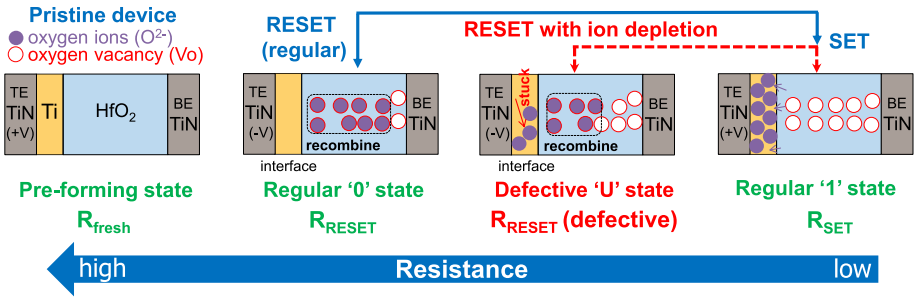


Fig. 9. Diagram depicting the ID mechanism involved in the RESET phase, adapted from [16].

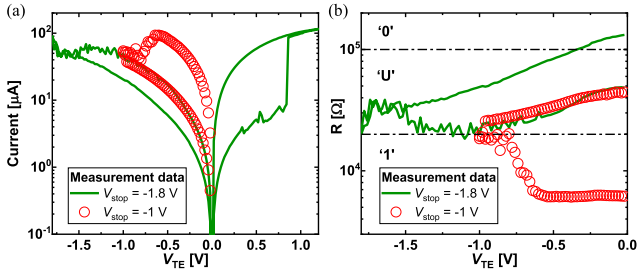


Fig. 10. Regular and weak RESET of the defective device with different V_{stop}. (a) Measured I–V characteristics plotted with a logarithmic scale on the y-axis. (b) Measured R–V response using the same log-scale representation.

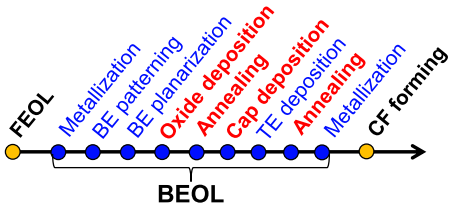


Fig. 11. Flow of RRAM manufacturing process [10], [27], adapted from [16].

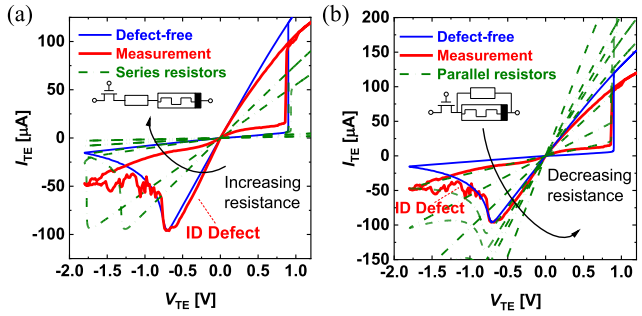


Fig. 12. Resistive defect models based on linear elements, adapted from [16]. (a) Series connection. (b) Parallel connection.

approach to accurately model defects/faults and develop tests for defects inside the device. Next, we will first demonstrate the inadequacy of linear resistors in effectively representing the ID defect. Afterward, we use the DA method to analyze the identified ID defect and develop an accurate defect model capable of describing its behavior.

A. Conventional Resistor Defect Models

The linear resistors are used in RRAM defect modeling by connecting them in either series or parallel with the device, as shown in Fig. 12. Varying resistance values are used in each of these linear defects to depict the dimensions and strength of the physical defect. When the series ohmic resistance increases or the parallel ohmic resistance decreases, it means that there are stronger defects and the faulty behavior is more severe. Fig. 12(a) and (b) depicts the behavior of the defective device under different defect strengths, namely the resistance of resistors. The red line represents the measurement of the ID-defective device. The electrical characteristics of the ID-defective RRAM device, such as R_{SET}, R_{RESET}, V_{SET}, and V_{RESET}, are clearly influenced by different strengths of resistive defects. The parallel resistor may also cause the same behavior of R_{RESET} degradation as the ID-defective device [see the green dotted line in Fig. 12(b)]. However, it is unable to be fit with other electrical parameters such as V_{RESET} and R_{SET}; hence, it cannot accurately model the ID defect. If the linear resistor defect significantly affects the device, it may potentially result in the failure to transition between HRS and LRS states. Clearly, neither of these two linear defect models can accurately describe the ID. Therefore, a more comprehensive defect modeling approach is necessary for accurately capturing the state drift in the RRAM RESET performance.

B. DA Defect Modeling

In this section, we apply a systematic DA approach to model ID defects with circuit-level fidelity. By leveraging a physics-driven defect-free model together with silicon measurement data from defective devices, the DAT approach produces a parameterized compact model that is both physically consistent and directly usable for fault/test simulation. The proposed DA defect modeling framework consists of three main stages: 1) identification and modeling of physical defects; 2) electrical representation of defective devices; and 3) parameter tuning and model calibration. The framework starts from a physics-driven baseline model and yields a parameterized defective-device representation tailored to the observed faulty behavior, while maintaining consistency with the defect-free device behavior. In the next step, we apply this framework to construct a physics-based model targeting ID defects. As a starting point, we analyze how ID influences the local concentration of O^{2-} within defective devices. Following this, the electrical parameters of the RRAM, such as V_{RESET} and R_{RESET}, are used to map its impact. Finally, the measurements are employed to calibrate the ID-defective RRAM compact model. Compared with our prior conference version ([16]), this journal extension further incorporates long-sequence measurements to calibrate and model intermittency, which is essential for accurate multi-cycle fault/test simulations.

1) Physical Defect Analysis and Modeling: The defect physical mechanism must be used as the foundation for the development of the ID defect model in order to assess the

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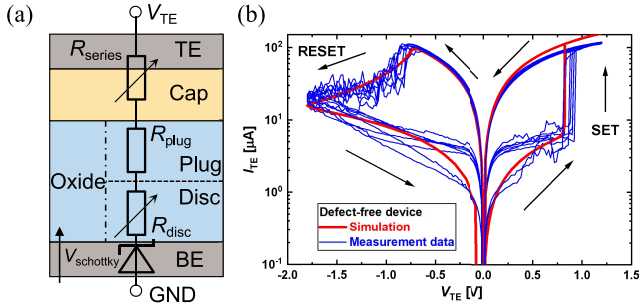


Fig. 13. Verilog-A compact modeling and simulation of a defect-free device, adapted from [16]. (a) Equivalent circuit of the JART VCM v1b model [33]. (b) Log-scale fitting result for the defect-free device.

effects of each (key) technology parameter of the device. In Section III, we characterize and analyze the ID defect, which is caused by insufficient O^{2-} available to recombine OVs in the bulk oxide. As a result, technology-dependent parameters that affect the O^{2-} availability (and thus OV recombination during RESET) deviate from their ideal values and lead to defective behavior. The physics-based HfO_2 RRAM model, JART VCM v1b, from [33], is employed to accurately model this defect. The compact model is intended to simulate the change of OV in the oxide in a valence change mechanism (VCM)-based device. The equivalent circuit diagram of the compact RRAM model is depicted in Fig. 13(a). This diagram comprises a Schottky-like contact (V_{schottky}), two filament resistances (R_{plug} and R_{disk}), and a series resistance (R_{series}) [33]. The oxide is divided into the disk region (where switching is modeled) and the plug region (conductive region with an abundant vacancy supply). Both SET and RESET are described by ionic migration of OVs, which modulates the Schottky barrier and thus the device conductivity [33]. The OV concentration is represented by N_{disk}, and the built-in limiting parameters $N_{\text{disk,min}}$ and $N_{\text{disk,max}}$ constrain N_{disk} within a physically meaningful range. In the presence of an ID defect, the OV recombination during RESET is restricted due to insufficient O^{2-}, resulting in a larger amount of residual OVs after RESET and thus a degraded HRS (undesired "U" state). To capture this behavior in a circuit-usable manner, we introduce a cycle-resolved residual disk concentration $N_{\text{disk,remain}}$ to represent the remaining OV concentration during RESET, which directly determines the measured R_{RESET} in that cycle. The final disk concentration at the end of RESET is therefore set as

$$N_{\text{disk}} = \max\left(N_{\text{disk,min}}, N_{\text{disk,remain}}\right) \tag{1}$$

i.e., when $N_{\text{disk,remain}} < N_{\text{disk,min}}$, it is clamped to the built-in lower bound $N_{\text{disk,min}}$ to preserve the physical constraints of the baseline compact model.

2) Electrical Defect Modeling: Once the physical defect analysis is completed, the impacted physical parameters (e.g., the OV concentration) are integrated into the electrical parameters, including V_{RESET}, R_{RESET} and I_{TE}. JART VCM v1b is a compact model that is written in Verilog-A and can be seamlessly integrated into the circuit-level (e.g., SPICE simulator) simulation. The model is capable of analyzing the impact of insufficient O^{2-} recombination on the switching electrical behavior (e.g., current, resistance) in the presence of the modeled defect by utilizing the disk-region vacancy concentration variables (e.g., N_{disk}, together with $N_{\text{disk,remain}}$ and the built-in bound $N_{\text{disk,min}}$) to capture defective switching behavior. The temporal evolution of N_{disk} is presented in the defect-free model as [33]

$$\frac{\mathrm{d}N_{\text{disk}}}{\mathrm{d}t} = \frac{I_{\text{ion}}}{zVo \cdot e \cdot A \cdot l_{\text{det}}}. \tag{2}$$

Here, the cross section and length of the filament are denoted by A and l_{det}, respectively. The ionic current in the device is denoted by I_{ion} and is calculated by the recommendations of Genreith-Schriever [34]. Thus, the ionic current alteration is directly proportional to the OV concentration (N_{disk}) and is equal to zero when either $N_{\text{disk,max}}$ or $N_{\text{disk,min}}$ is attained [33]. All other baseline parameters are listed in Table II. Therefore, the electrical behavior of the defective device switching, which includes current variations, can be examined by connecting it to N_{disk} using model simulations.

TABLE II
MODEL PARAMETERS

Symbol	Value	Symbol	Value
T_0	0.293 K	ν_0	$2 \cdot 10^{13}$ Hz
ϵ_s	11	ΔW_A	1.35 eV
$\epsilon_{\phi_{Bn0}}$	2.5	R_{th0}	$15.72 \cdot 10^6$ K·W^{-1}
ϕ_{Bn0}	0.18 eV	r_{det}	45 nm
ϕ_n	0.1 eV	l_{cell}	3 nm
μ_{n0}	$4 \cdot 10^{-6}$ m^2/(Vs)	l_{det}	0.45 nm
$N_{disc,max}$	$6.5 \cdot 10^{25}$ m^{-3}	$R_{theff,scaling}$	0.31
$N_{disc,min}$	$5 \cdot 10^{23}$ m^{-3}	$R_{series,ICL}$	650 Ω
N_{init}	$5 \cdot 10^{23}$ m^{-3}	R_0	1750 Ω
N_{plug}	$6.5 \cdot 10^{25}$ m^{-3}	$R_{th,line}$	90 471.5 W·K^{-1}
a	0.25 nm	α_{line}	$3.92 \cdot 10^{-3}$ K^{-1}

a) Baseline id-defect modeling using a representative defective cycle [16]: In this step, we first construct the baseline ID-defective compact model by calibrating it to a representative cycle in which the ID defect is observed. The key electrical effect of ID defects is an abnormally high remaining OV concentration after RESET, which we represent by $N_{\text{disk,remain}}$ and (1). To account for the voltage dependence, we parameterize $N_{\text{disk,remain}}$ as a voltage-dependent function motivated by the field-enhanced ionic hopping mechanism coupled with trap-assisted tunneling (TAT), exhibiting exponential voltage dependence [19], [33]

$$N_{\text{disk,remain}} = \exp\left[-\left(\frac{-V_{\text{TE}}}{p_1}\right)^{p_2}\right], \quad (V_{\text{TE}} < -1\ \text{V}). \tag{3}$$

Here, p_1 and p_2 function as fitting parameters. Equation (3) provides the voltage-dependent mapping of $N_{\text{disk,remain}}$ (here applied for $V_{\text{TE}} < -1$ V). The physical lower bound is enforced by (1), i.e., if the computed $N_{\text{disk,remain}}$ falls below $N_{\text{disk,min}}$, it is clamped to $N_{\text{disk,min}}$.

b) Journal extension: cycle-level intermittency modeling: While the baseline calibration captures the defect behavior within a representative defective cycle, multi-cycle measurements reveal that the ID-induced "U" state is intermittent across cycles and its occurrence probability is below 100%. To characterize this intermittent behavior for circuit-level simulation, we analyze a total of 836 RESET-SET cycles of the defective device (WL = 5, BL = 3) after skipping the first 100 unstable cycles. We compute the occurrence probability of the undesired "U" state over consecutive n cycles ($n = 1, 2, 3, 4$), denoted by P_{D1}-P_{D4}. Among the 836 cycles, P_{D1} = 117/836 = 14.00% of them are defective (e.g., in cycles 110, 210, and 263), P_{D2} = 29/(836-1) = 3.47% are sustained for two *consecutive* cycles (e.g., in cycles 107 and 108), P_{D3} = 7/(836-2) = 0.84% are sustained for three

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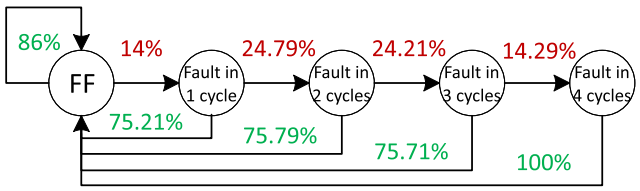


Fig. 14. State transition diagram showing probabilities of faulty "U" states over multiple cycles.

consecutive cycles (e.g., in cycles 348, 349, and 350), and P_{D4} = 1/(836-3) = 0.12% are sustained for four *consecutive* cycles. The maximal duration of the undesired "U" state is four cycles and only occurs once, starting in cycle 763.

Next, we conduct the correlation analysis of consecutive cycles for the defective device. Assuming the undesired "U" state occurring in each cycle are independent events from each other, the occurrence probability of the defect in two consecutive cycles is $P_2 = P_{D1}^2 = 1.96\%$, which is smaller than the measured P_{D2} (3.47%). Similarly, $P_3 = P_{D1}^3 = 0.27\% < P_{D3}$ and $P_4 = P_{D1}^4 = 0.04\% < P_{D4}$. Consequently, there is a correlation between each cycle and the occurrence of undesired "U" states. We can use the formula of conditional probability. First, we define "the second cycle is defective" as event B, "the third cycle is defective" as event C, and "the fourth cycle is defective" as event D. Then, the conditional probability that the second cycle is defective (event B) given that the first cycle has already been defective (event A) is: $P(B|A) = P(A \cap B)/P(A) = P_{D2}/P_{D1} = 24.79\%$. Following the same formula, we can obtain $P(C|(A \cap B)) = P_{D3}/P_{D2} = 24.21\%$, and $P(D|(A \cap B \cap C)) = P_{D4}/P_{D3} = 14.29\%$. Fig. 14 represents a state transition diagram, illustrating the statistical probability associated with the faulty "U" states occurring over multiple cycles in a system. Each state corresponds to a specific number of fault cycles (e.g., "Fault in 1 cycle"), with transition probabilities indicating the statistical likelihood of moving to the next state or returning to a fault-free ("FF") state. For example, the diagram starts with an initial state, labeled "FF" with a transition probability of 14% leading to the "Fault in 1 cycle" state, indicating that there is a 14% chance of a fault occurring in the first cycle. Subsequent transitions between states show the probability of faults continuing across additional cycles, with 24.79% leading to a fault in the second cycle, 24.21% leading to a fault in the third cycle, and 14.29% leading to a fault in the fourth cycle. Red percentages represent the chances of faults continuing, while green percentages show the likelihood of recovery or remaining fault-free. For instance, from the initial state "FF," there is an 86% chance of returning to the FF condition after one cycle and a 75.21% chance after two cycles. Finally, once a fault occurs in all four cycles, it will 100% recover to the "FF" state since the maximal duration of the defect is four cycles based on the measurements.

Implementation in the Compact Model: We incorporate intermittency as a *cycle-level* state-transition (Markov) activation layer in the Verilog-A compact model (Fig. 14). At each RESET-SET cycle, a random number is used to sample whether the ID defect is activated according to the transition probabilities extracted from measurements. If activated, the cycle-dependent defect strength is modeled by updating $N_{disk,remain}$ [thus N_{disk} via (1)]; otherwise, the model follows defect-free behavior. The state depth is limited to four cycles because the maximum observed consecutive faulty duration is four cycles in measurements.

Algorithmically, the implementation proceeds as follows: 1) maintain a cycle/state counter; 2) determine the activation probability based on the current state (i.e., fault occurrences in previous cycles) following Fig. 14; 3) if activated, update $N_{disk,remain}$ to reflect the measured cycle-dependent defect strength [while enforcing the physical lower bound via (1)]; and 4) update the state and counter; the counter is reset after it reaches four cycles.

3) Fitting and Model Optimization: MATLAB R2021a is employed to perform the fitting in order to match the I-V measurements from Section III. The fitting procedure is comprised of the subsequent two steps: 1) the fitting of defect-free device behavior and 2) the fitting of the defective device behavior using defective parameter $N_{disk,remain}$.

C. Step 1: Defect-Free Calibration

The defect-free measurement data were calibrated using the JART VCM v1b model, with the fit parameter values displayed in Table II. In the simulation, the RRAM model is connected in series with a transistor of identical dimensions to those used for device characterization. The voltage (V_{TE}) is ramped from 0 to −1.8 V, and back to 0 V for RESET; from 0 V, then to 1.2 V, and back to 0 V for SET. The fitting result of the BS device model simulation and the measurements of the defect-free device in various RESET-SET cycles are illustrated in Fig. 13(b). The model exhibits BS behavior, which is consistent with the measurements.

D. Step 2: ID-Defective Calibration

1) Baseline Calibration Using a Representative Defective Cycle [16]: We calibrate the measurements for the ID-defective device. All defect-free parameters are kept unchanged (Table II); only defect-related parameters (e.g., p_1, p_2 for $N_{disk,remain}$, and intermittency parameters) are calibrated from defective measurements. We extract the mapping parameters p_1 and p_2 in (3) using least-squares fitting in MathWorks's MATLAB R2021a, yielding $p_1 = 0.0611$ and $p_2 = 0.4209$. It demonstrates that a smaller value of $N_{disk,remain}$ is induced by lower negative RESET voltages (while it is physically bounded by the built-in lower limit $N_{disk,min}$). This is in accordance with the actual RRAM mechanism observed in [23]. Fig. 15(a) illustrates the simulated *I–V* curves, while Fig. 15(b) compares the fitting results for both defect-free and defective devices through the simulated R–V curves under the RESET/SET voltage sweep. First, both devices exhibit comparable LRS behavior, increasing at an equivalent rate as the RESET voltage decreases (①). Then, the defective device encounters a delayed increase in resistance, which is indicative of an anomalous RESET (②). The R_{RESET} is defective and remains in an intermediate state (③,④). However, it decreases in a normal manner with the positive SET voltage (⑤) and transitions to a normal LRS (⑥). The simulated HRS of the model at the beginning of SET is also greater than the HRS at RESET, as illustrated in Fig. 15(b) (④). This is elucidated by the fact that the Schottky contact at the BE/oxide interface is modeled as a diode in the RRAM model. As a result, its behavior can be divided into two conduction modes: forward direction when a negative RESET voltage is applied, and reverse direction under a positive SET voltage [33]. The diode's potential barrier corresponds to the difference between the oxide's electron affinity and the work function of the BE [33]. The SET process, particularly in the HRS, results in a

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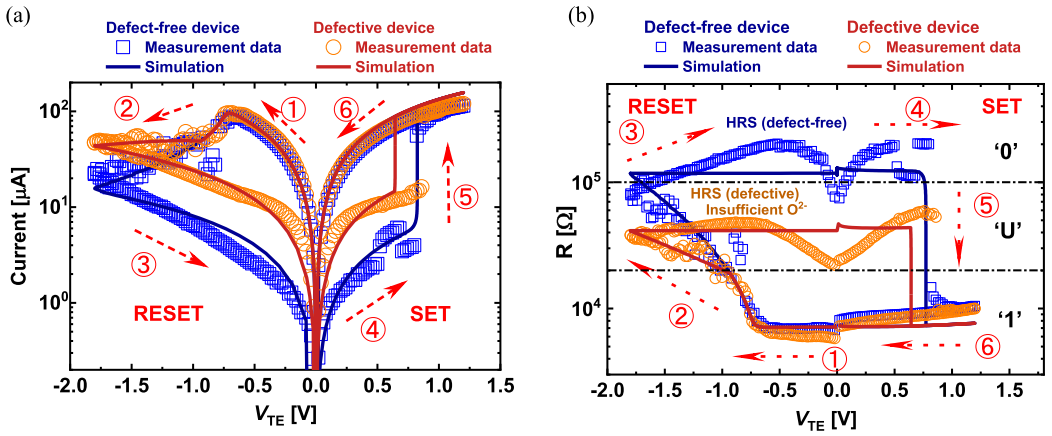


Fig. 15. Comparison between simulated and measured results for defect-free (WL = 5, BL = 0) and defective (WL = 5, BL = 3) devices, adapted from [16]. (a) *I–V* characteristics and (b) *R–V* characteristics.

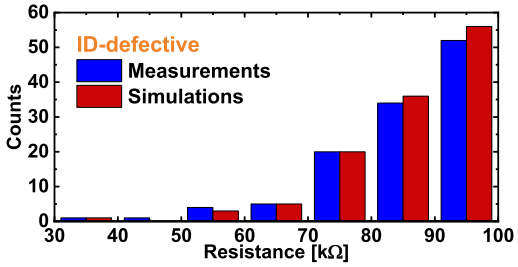


Fig. 16. Histogram of defective R_{RESET} distributions: measurements versus simulations.

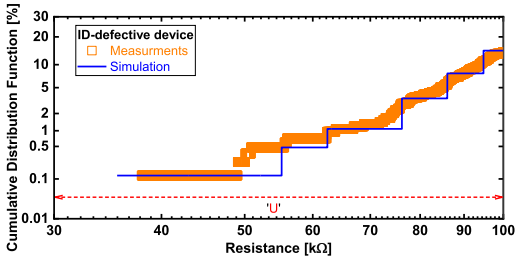


Fig. 17. Cumulative probability of defective R_{RESET} distributions: measurements versus simulations.

higher device resistance and a small Schottky current due to the application of various electronic conduction mechanisms. The measurements are accurately simulated by the model, with the exception of the defective device's V_{SET} reduction (⑤). This behavior can be attributed to the inclusion of initial resistance state–dependent thermoelectric interactions in the model during the SET phase, which leads to reduced transition delay times when the initial HRS is lower [33]. Additionally, the final LRS is not dependent on the initial state; rather, it is based on the applied voltage amplitude, as demonstrated by both the model simulation and measurements [33]. Therefore, in the subsequent RESET cycle, both ID-defective and defect-free devices keep the standard LRS. The model is capable of precisely describing the ID-defective RRAM device in a circuit simulator, as evidenced by the fitting results. Finally, the calibrated Verilog-A ID-defective RRAM compact model is the result of DA defect modeling. The fitting output indicates that the model is able to accurately describe the ID-defective RRAM device in a circuit simulator.

2) Journal Extension: Cycle-Level Intermittency Modeling: The above calibration reproduces the switching trajectory and defect strength within a representative defective cycle. To capture the intermittent behavior and calibrate the model with the measurements, we implement the cycle-level state-transition activation mechanism described above (Fig. 14) in the Verilog-A model and run 836 consecutive RESET-SET cycles, recording R_{RESET} after each cycle. Fig. 16 illustrates that the fit model is capable of accurately describing the intermittent behavior as well as varying defect strengths. Furthermore, Fig. 17 shows the cumulative distributions of faulty resistance for the defective RRAM devices and the simulation results. Note that we only show measurements and simulation results that exhibit ID-defective "U" states during cycles. Finally, the developed ID-defective model is compatible with circuit-level simulation, consistent with measurements, and significant for DfT/test evaluation and reliability analysis.

V. DA Fault Modeling of ID

The second phase of the DAT approach involves DA fault modeling, incorporating two key features: 1) definition of the fault space and 2) analysis of the fault. Building on [16], the present work further extends the fault modeling by incorporating newly defined fault behaviors arising from the richer defect characteristics identified in this journal version. First, we establish and categorize the fault space. Then, the fault analysis will be conducted using the electrical models to simulate the circuit.

A. Fault Space Definition and Classification

A fault space is the specified group of all potential modeled faults that may manifest in the circuit. The fault primitive (FP) notation is a systematic approach that can be used to describe all faults that result in incorrect logical behaviors: ⟨S/F/R⟩ [8]. Here, the sensitizing sequences of the cell are denoted by S. The stored value in the cell after the application of sensitizing S is denoted by F. F indicates the final stored value in the cell once the sensitizing S has been applied. The read output of the circuit is denoted by R, where $\mathrm{R} \in \{0, 1, ?, -\}$. Specifically, ? represents a random read outcome (e.g., the SA voltage is an intermediate value as a result of the sensing and reference currents being too near), and − indicates that the most recent operation conducted in the cell was not r.

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For instance, ⟨0r0/U/1⟩ represents a 0r0 operation performed on an HRS cell (S = 0r0), where the cell switches to an incorrect undefined state (F = U), and the read output returns "1" (R = 1) rather than the expected "0." For instance, the 0r0 operation is applied to an LRS cell (S = 1r1). The cell is then flipped to a faulty 'U state (F = U), resulting in a read output of "0" (R = 0) instead of the anticipated value of "1." This fault can be denoted as ⟨1r1/U/0⟩.

There are two types of faults: *static* and *dynamic*. Static faults can be sensitized by a single operation, while dynamic faults necessitate multiple operations to be sensitized. Faults can also be defined as *strong* and *weak* faults. An FP can only present strong faults; weak faults are parametric faults and do not cause any functional errors, e.g., a reduced BL voltage during a write operation. *easy-to-detect (EtD)* faults are a particular sort of strong faults that may be properly guaranteed to be sensitized and detectable by normal memory operations. *strong/weak hard-to-detect (sHtD/wHtD)* faults refer to strong faults devoid of predictable behavior (e.g., random read outputs), as well as weak faults.

B. Fault Analysis

1) Simulation Setup: This step is derived from the simulation of the electrical model constructed in Section IV. The simulation of the ID effect is conducted using Cadence Specter, implemented with the TSMC-40 nm transistor library and the RRAM compact model from [33]. The structure consists of a 1T–1R cell (with identical dimensions as the devices used for characterization) and the required circuitry to provide the three control lines (BL, SL, and WL) with the appropriate voltages. Standard voltage-based SA is used for reading purposes [20]. Two experiments are conducted for the purpose of fault analysis. The first experiment is constructed to validate faults with different strengths of ID defects. The injection of ID defects is achieved by replacing the defect-free RRAM model with the model of the ID-defective RRAM device developed in Section IV. Various defect strengths of $N_{\text{disk,remain}}$ are modified within the range of $0.005 \cdot 10^{26}$ m−3 to $0.065 \cdot 10^{26}\,\text{m}^{-3}$ to guarantee accurate model functioning and adherence to realistic physical constraints [33]. Consistent with the measurement setup, the voltage in the simulation sweeps via SL from 0 to 1.8 V back to 0 V (in RESET hysteresis) to sensitize the fault. In this work, the sensitizing operation for the ID defect is 1w0 (RESET), and the analysis mainly focuses on the static fault manifestations ⟨1w0/1/−⟩ and ⟨1w0/U/−⟩, as well as their intermittent cases. To determine the faulty behavior in the presence of the modeled defect, the simulation results are evaluated for the ultimate reached resistance of the defective devices (i.e., R_{RESET} after RESET operation). For example, F = U if the final R_{RESET} is outside of the HRS boundary (i.e., [100 kΩ, 1 MΩ]). The second experiment is established to validate the fault space when a linear resistor is present, either in series (R_s) or in parallel (R_p), with a device that is defect-free. The resistor defect sweeps from 1 Ω to 100 MΩ in strength.

2) Fault Modeling and Results: The simulation results for varying defect strengths are shown in Table III. In this analysis, a fault is classified as static if it can be sensitized and observed by the single operation 1w0; by contrast, a fault would be classified as dynamic if multiple consecutive operations or operation-history dependence were required before the faulty behavior becomes observable. Depending on the defect strengths, the table shows both EtD (⟨1w0/1/−⟩) and sHtD (⟨1w0/U/−⟩) faults. More faults are sensitized as $N_{\text{disk,remain}}$ increases. This identifies $N_{\text{disk,remain}}$ as the key defect-related parameter in the fault analysis, since it determines whether the RESET operation leaves the cell in the undesired "U" state. While EtD faults are sensitized for $N_{\text{disk,remain}}$ above $0.042 \cdot 10^{26}\,\text{m}^{-3}$, sHtD faults are sensitized for $N_{\text{disk,remain}}$ between $0.006 \cdot 10^{26}\,\text{m}^{-3}$ and $0.0415 \cdot 10^{26}\,\text{m}^{-3}$. Considering the defective measurement data shown in Fig. 15, $N_{\text{disk,remain}} = 0.016 \cdot 10^{26}\,m^{-3}$ (bold in the table) is calibrated in this case. Greater space for OVs to be recombined in the disk region is given by higher $N_{\text{disk,remain}}$, which increases the likelihood of undesired RESET failure in the device. The concentration of OV lowers as more O^{2-} are attracted toward the oxide bulk to recombine with it as the decrease in supplied negative RESET voltage. However, ID-defective devices are unable to release a sufficient amount of O^{2-} back into the oxide bulk, which raises the final OV concentration while lowering the R_{RESET}. As a result, faults can be sensitized at these voltages. Greater $N_{\text{disk,remain}}$ indicates a higher defect strength and more O^{2-} depletion (inadequacy).

TABLE III
ION DEPLETION-INDUCED FAULT MODEL VALIDATIONS

$N_{\text{disc,remain}}$ [$10^{26}\,\text{m}^{-3}$]	R_{RESET} [kΩ]	Fault	Type
0.065	15.21	⟨1w0/1/−⟩	EtD
0.05	17.76	⟨1w0/1/−⟩	
0.0415	20.03	⟨1w0/U/−⟩	sHtD
0.035	22.51	⟨1w0/U/−⟩	
0.016	41.34	⟨1w0/U/−⟩	
0.0113	55.55	⟨1w0/U/−⟩	
0.0077	78.57	⟨1w0/U/−⟩	
0.006	99.64	⟨1w0/U/−⟩	
0.005	118.42	Fault free	

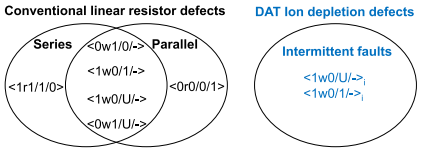


Fig. 18. Static faults.

The static faults that are sensitized using the DAT as well as the traditional approach (linear resistor model) are then compared; these are shown in Fig. 18. The figure illustrates the distinctions between the two approaches. Due to the intermittent behavior, ID will only sensitize intermittent faults, as shown in the right circle. We denote the corresponding FP as ⟨1w0/1/−⟩$_i$ and ⟨1w0/U/−⟩$_i$, where the subscript i indicates the intermittent case. Clearly, conventional defect models based on either series or parallel resistors fail to capture the realistic faults sensitized by ID. Additionally, we are able to distinguish and diagnose ID defects from linear resistor defects due to the comparison result.

VI. DAT DEVELOPMENT

The final stage of the DAT approach is to provide effective test solutions addressing the validated RESET faults in Section V. Compared with [16], this journal version further strengthens the test design by validating the previously proposed test method under variation and by additionally proposing and evaluating a DfT strategy. First, we discuss the

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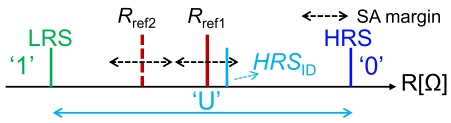


Fig. 19. Resistances for faulty RRAM state adapted from [16].

test generations for ID defects. Next, we provide a concise overview comparing different RRAM defects.

A. Test Generation

Table III illustrates how the ID defect could result in EtD and sHtd faults when the RESET procedure is performed. The March algorithm below is one straightforward test solution

March-ID = {⇕ (w1); ⇕ (w0, r0)}.

Here, "⇕" denotes an irrelevant addressing direction. The first march element sets all memory cells to state "1," with w0 indicating a RESET operation, and r0 signifying a read 0 operation for fault detection. This test algorithm ensures the detection of EtD faults, i.e., $N_{\text{disk,remain}} > 0.0415 \cdot 10^{26}\,\text{m}^{-3}$ in our simulation. However, due to the *intermittent* nature of the ID, the proposed test algorithm detects the fault *probabilistically*. Hence, multiple iterations of 1w0 (for sensitization) and read (for detection) are needed to improve the probability of detection. Assuming the ID defect occurs with probability P_{ID}, then the detection probability can be expressed as: $P_{\text{d}} = 1-(1-P_{\text{ID}})^k$, k indicates the repetition time of the applied sequence. In our case of $P_{\text{ID}} = 14\%$, $k = 31$ is necessary to achieve over 99% fault coverage.

However, this March algorithm does not satisfy the fault coverage requirement for sHtD faults in the "U" state, which can lead to random read outputs. Therefore, DfT schemes specifically targeting these sHtD faults should be employed.

It is possible to include different References in the SA so that it can distinguish resistance states between "U"/"1" or "U"/"0" instead of distinguishing only the regular "0"/"1" [35]. For example, Singh et al. [35] introduce a DfT scheme utilizing multiple references in the SA during a single read to execute a logic NOR operation to determine RRAM device resistance [35]. However, this approach requires a significant area overhead and does not account for process variations. In this article, we propose two low-cost re-configurable DfT schemes by modifying the references in SA to detect the intermediate HRS of ID-defective devices. Fig. 19 demonstrates the DfT concept involving various references to identify the "U" state in ID-defective devices. R_{ref1} is set to (HRS + LRS)/2 for the defect-free device. R_{RESET} of the ID-defective device is referred to as HRS_{ID}, which is near R_{ref1} (within the SA margin) and cannot be reliably distinguished as logic "0." To detect this faulty state, the reference can be set to R_{ref2} of $(HRS_{\text{ID}} + \text{LRS})/2$ for the ID-defective device.

Next, we implement a 2×2 RRAM array circuit shown in Fig. 4 with read circuits and proposed write drivers to validate the following two DfT schemes. The proposed DfT schemes are validated in this work at the circuit level, using a silicon-calibrated defect-aware compact model together with the TSMC 40 nm industrial transistor library and variation-aware simulations. Note that here we evaluate the DfTs considering process variations but assuming that the ID defect occurs (not intermittent) to verify the detection capability.

1) Reference Tunable Scheme: The first scheme is an adaptable DfT method featuring a tunable reference design that

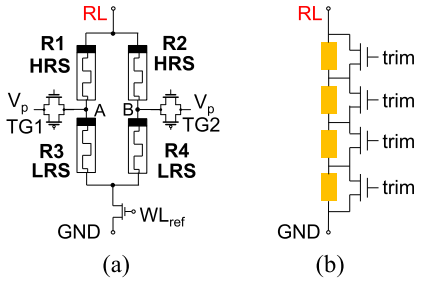


Fig. 20. Reference resistance for DfT schemes. (a) Programmable reference cells. (b) Controllable reference trimming.

remains compatible with standard read operations. The tunable reference cells comprise two series RRAM devices, paralleled by another two RRAM devices in series, with additional two transmission gates (TG1, TG2), as shown in Fig. 20(a). Each branch incorporates one RRAM device set to an LRS and the other to an HRS, such that the equivalent resistance of the parallel configuration lies between the two programmed values. Two transmission gates (TG1 and TG2) are used to selectively apply voltage pulses (i.e., V_{P}) to nodes A and B, enabling programmable control over the reference resistances. For example, activating TG1 applies the programming voltage V_{P} to node A, allowing fine-tuning of R1. To implement and evaluate the DfT scheme, an RRAM circuit including 2×2 1T-1R cells and SA (using TSMC transistor model and compact RRAM model [33]) shown in Fig. 4 is built.

First, the defect-free circuit is validated. Under a 1w0 operation, a 1.8 V RESET voltage is applied to the SL, with the BL grounded, transitioning the resistance state from LRS to HRS. The FF HRS can then be read correctly by the used SA, with $R_{\text{ref1}} = 61.13\,\text{k}\Omega$. Next, we replace the defect-free cell with the ID-defective device model, including variations. After applying the same 1w0r0 operation, the faulty HRS (with the strength of $N_{\text{disk,remain}} = 0.01 \cdot 10^{26}\,\text{m}^{-3}$) is incorrectly read because the BL/RL voltage difference ($\Delta V = V_{\text{BL}} - V_{\text{RL}}$) remains below the SA margin (ΔV_{min}). By tuning the original HRS in the reference cell to the HRS_{ID} (i.e., $R_{\text{ref2}} = 32.81\,\text{k}\Omega$), the faulty HRS_{ID} can be correctly distinguished from the LRS by the readout value. Furthermore, we perform a sensitivity analysis to study the influence of process variation of both transistors and RRAM devices. For the transistor variations, we use the variation models that include the statistical mismatch from the TSMC 40 nm model library. For RRAM device variations, we set up the models as described in [36]. We incorporate both device-to-device (D2D) (from a truncated Gaussian distribution) and cycle-to-cycle (C2C) (change the variable parameters with confined step size, whose maximum is chosen to be 10% of the current value) variations of the RRAM cells (including the reference cell). Using R_{ref1} in 5000 MC simulations, only 33.9% of read operations correctly detect the injected ID defect. In contrast, switching to the DfT scheme with the trimmed reference R_{ref2} results in a dramatic improvement: 99.34% of simulations produce correct "0" outputs. These results validate the effectiveness of the first DfT scheme, demonstrating its ability to accurately detect ID defects while maintaining high resilience to process variation.

2) Reference Trimming Scheme: Although the first circuit proposed is validated for the ID defect, precisely controlling the programming of the RRAM-based reference resistor is challenging. To address this limitation, we propose a second

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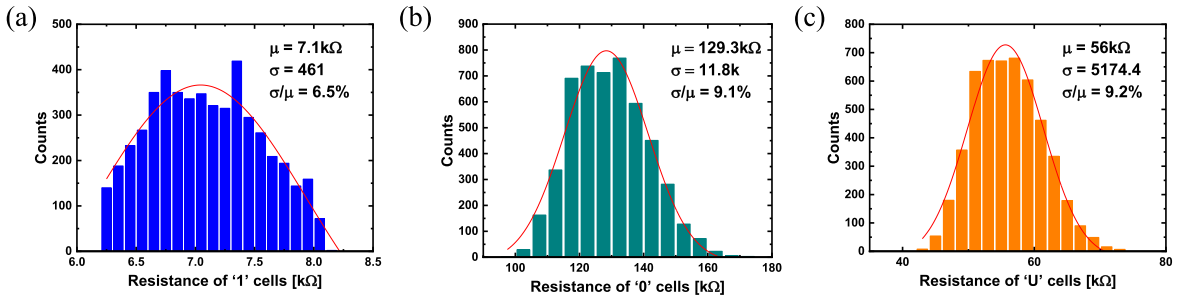


Fig. 21. Histograms of the RRAM resistance distribution under variations. (a) Resistance of "1" cell (defect-free). (b) Resistance of "0" cell (defect-free). (c) Resistance of "U" cell (ID-defective).

scheme that incorporates tunable resistors to adjust the reference resistance. This is implemented by connecting multiple resistors in series, each of which can be selectively bypassed, as illustrated in Fig. 20(b). We use the minimal size (width= 400 nm, length = 270 nm) of the TSMC 40 nm library as the minimal resistor. It has an equivalent resistance of around 4 kΩ and is guaranteed to operate in the linear region. By controlling trim settings, the reference resistance can be configured as $R_{\text{ref2}} = 40$ kΩ (enable ten transistors, design for defective "U" cells), and $R_{\text{ref1}} = 60$ kΩ (enable 15 transistors, design for defect-free cells).

To demonstrate the effectiveness of this trimming-based design, we inject an ID defect with a strength of $N_{\text{disk,remain}} = 0.01 \cdot 10^{26}\,\text{m}^{-3}$. Under this condition, the SA using R_{ref1} incorrectly returns a logic "1," while the SA using the trimming R_{ref2} correctly returns a logic "0." We further evaluate the robustness of the scheme under RRAM variation and process variation through Monte Carlo (MC) simulations. Fig. 21(a)–(c) shows histograms for the LRS, HRS cells of the defect-free circuit, and the defective "U" cells, for 5000 MC simulations. The mean values are 7.1 kΩ of "1" cells, 129.3 kΩ of "0" cells, and 56 kΩ of "U" cells, all within the specification. Besides, the coefficient of variations (CV, σ/μ) are 6.5%, 9.1%, and 9.2% for "1" cells, "0" cells, and "U" cells, respectively. In statistics, a lower CV indicates more uniformity in the data, which is consistent with the physics of RRAMs [22]. Upon validation of read operations under the process variation in the defect-free case, 100% of the 10 000 iterations (5000 read "0" and 5000 read "1") result in the correct read outputs with $R_{\text{ref1}} = 60$ kΩ. When the cell is defective in "U" state, 2191/5000 iterations return to incorrect "1" read outputs with $R_{\text{ref1}} = 60$ kΩ. After the reference trimming is set to $R_{\text{ref2}} = 40$ kΩ, 100% of the 5000 iterations return to correct "0" read outputs, although the ID-defect is injected. In summary, the results show that the proposed DfT is decently resilient against process variations.

To further reduce the test duration, dedicated DfTs are necessary, focusing on minimizing the occurrence of the ID defect by, e.g., operating the device at low temperatures below 293 K. This will lead to a slow migration of O^{2-} recombination [23], [33]. Then, the ID-defective device may fail to switch and stuck at "1" (during the RESET operation), being easily detected. A drawback of this approach is that extra cryogenic equipment is required, and the electrical behavior of the transistors is also affected at low temperatures. The approach may involve increasing device current during SET over-forming the device, leading to a higher OV concentration and reduced final RESET resistance in ID-defective devices [2], [15]. This can be achieved by boosting the BL or WL in test mode. However, the downside of this method is a lower R_{SET}, which increases energy consumption and write latency.

TABLE IV
FAULT ANALYSIS RESULTS FOR ID DEFECT

Defect/Fault	Faulty Behaviors	Fault Models (sHtD)
Over forming	Low R_{SET}/R_{RESET}, high V_{RESET}	⟨1w0/U/−⟩ ⟨0w1/H/−⟩
Under forming	High R_{SET}/R_{RESET}, low V_{RESET}	⟨1w1/U/−⟩ ⟨1w0/L/−⟩
IUSF	Intermittent, high R_{SET}	⟨0w1/U/−⟩
ID	Low R_{RESET}, normal R_{SET}/V_{RESET}	⟨1w0/U/−⟩
Over RESET	High R_{RESET}, high V_{SET}	⟨1w0/L/−⟩

B. Diagnosis of Unique RRAM Defects

Using characterized defect features to diagnose the causes of detected faults is consistent with the broader DA diagnosis methodology, which extends DAT from defect detection to defect diagnosis by exploiting defect-specific distinctive features [37]. Accordingly, the following comparison is not intended as an exhaustive survey of all RRAM defects, but rather as an illustration of how ID defects can be distinguished from other representative defect classes within a more general diagnosis framework. There have been reports of many RRAM defects and unique faults, e.g., over-, under-forming, and IUSF [15], [38]. Several of these defects can trigger similar undefined state faults. Identifying the specific characteristics behind similar faulty behaviors is essential for developing effective test strategies. To this end, we summarize (see Table IV) various defect types, including the ID defect, over and under-forming, IUSF, and over RESET, categorized by their underlying physical mechanisms [15], [38]. Over and under-forming defects may occur due to instability in the external tester channels conducting the forming process and the inherent device-to-device variation. When this occurs, the forming current deviates from the nominal value. Although both forming and ID defects can induce an undefined state fault, an under-forming defect causes both R_{RESET} and R_{SET} stuck at the undefined state, whereas an ID-defective device still maintains R_{SET} in "1" state. Thus, comparing R_{SET} alone is sufficient for diagnosing these two defects. IUSF causes the RRAM device to intermittently transition from BS to CS during the SET process, introducing undefined state faults, and it appears with a certain probability [15]. Accordingly, the 0w1 (SET) operation can be used to diagnose these defects. Meanwhile, Over RESET intermittently switches the device into an extremely HRS during the RESET phase, exceeding the HRS threshold; hence, the 1w0 (RESET) operation can identify these defects. We can conclude that although other RRAM defects potentially sensitize undefined state faults, additional behaviors allow us to distinguish them from ID

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defects. While the present article focuses on the ID defect for detailed DAT validation, the same diagnosis principle can, in principle, be extended to additional emerging defect classes, such as thermally induced defects, once their distinguishing electrical signatures are characterized.

VII. Conclusion

This article demonstrates that the DAT approach enables silicon-grounded characterization, modeling, and test/DfT validation of unique RRAM defects. As RRAM technologies continue to scale, more emerging defect mechanisms are expected, requiring stronger defect, fault modeling, test solutions, and diagnosis. The proposed framework therefore provides a practical basis for future extensions to other emerging RRAM defects. While the present work validates the proposed DfT schemes through variation-aware circuit-level simulations based on silicon-calibrated models, full hardware implementation and silicon test-chip validation remain important directions for future work.

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During the preparation of this article, the authors used ChatGPT to enhance its academic clarity while strictly preserving the original content without AI-generated writing. After using this tool, they reviewed and edited the content and took full responsibility for any errors or oversights.

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