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Citation (APA)
Undseth, B., Meggiato, N., Wu, Y. H., Katiraee-Far, S. R., Tryputen, L., de Snoo, S. L., Degli Esposti, D., Scappucci, G., Greplová, E., & Vandersypen, L. M. K. (2026). Weight-four parity checks in a spin-shuttling architecture. *Nature*, *655*(8125), 1160-1166. https://doi.org/10.1038/s41586-026-10766-3

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Article

Weight-four parity checks in a spin-shuttling architecture

https://doi.org/10.1038/s41586-026-10766-3

Received: 30 January 2026

Accepted: 4 June 2026

Published online: 29 July 2026

Open access

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Recent advances in coherent spin shuttling have made sparse semiconductor spin-qubit arrays an appealing solid-state platform to realize quantum processors[1–7]. The dynamic and long-range connectivity enabled by shuttling is also essential for many quantum error-correction schemes[8–10]. Here we demonstrate a silicon spin-qubit device comprising a shuttling bus for coherently transporting qubits that can interact at four isolated locations that we call bus stops. We dynamically populate the array and tune all single- and two-qubit operations using shuttling and quantum non-demolition spin measurements, without access to charge sensing in most of the device. We achieve universal control of the effective five-qubit processor and select the connectivity required to form a surface-code stabilizer plaquette that supports X- and Z-type parity checks up to weight four. We use the parity checks to generate multi-qubit entanglement between all qubit combinations in the array and report the genuine entanglement of a five-qubit Greenberger–Horne–Zeilinger state, constituting one of the largest such states constructed with gate-defined semiconductor spins. The protocols developed here lay the groundwork for modular calibration and operation of sparse spin-qubit arrays, and we highlight the feasibility of near-term quantum error-correction experiments with mobile spin qubits.

For semiconductor-based spin qubits to be a viable platform for fault-tolerant quantum computing, their physical advantages, including their small size, long coherence times and high-fidelity operations[11], must be compatible with quantum error correction (QEC). Although previous demonstrations of phase-flip codes with spin qubits have made use of Toffoli-like primitives to implement conditional correction operations[12,13], large-scale deployment of QEC requires the repeated extraction of stabilizer measurements to infer error syndromes in both space and time. A well-established error-correction benchmark, the surface code, uses weight-four X- and Z-type parity checks to achieve quantum memories with reasonable error thresholds[14]. Such operations require an ancillary qubit to interact with four data qubits, and the former must be measured without destroying the quantum state of the latter. This connectivity is challenging to realize in densely populated quantum-dot arrays owing to crosstalk and the co-integration of readout, but spin shuttling in sparsely occupied arrays has long been recognized as a path forward[15].

The performance of semiconductor-based spin shuttling has progressed rapidly in recent years owing to improvements in material uniformity and control techniques[1–7,16–19]. More recently, spin shuttling has also been used as a means of material characterization[20], qubit characterization[21] and implementing logical gates[22,23]. These advancements have maintained substantial interest in sparse spin-qubit architectures for fault-tolerant quantum information processing where the physical movement of spins enables the coupling of qubits at distances far greater than kinetic exchange or capacitive coupling and allows for the dynamic reconfiguration of qubit connectivity[9,10,15,24–27].

Qubit shuttling in other quantum computing platforms, such as trapped-ion systems[28] and neutral-atom systems[29], enables zoned architectures and permits beyond-planar connectivity that is relevant for QEC codes with higher encoding rates[8]. For semiconductor-based spins in particular, the additional separation between shuttled qubits in sparse arrays offers advantages beyond higher connectivity. First, residual exchange between adjacent spins can be effectively eliminated during idling, greatly reducing the potential for entangling crosstalk[30]. Second, a lower qubit density eases the routing and localization of control signals, which consequently reduces the calibration overhead required to mitigate capacitive crosstalk[31]. Finally, spin-qubit readout becomes more flexible as the co-integration of charge sensing can require charge reservoirs, direct current (DC) current paths[32] or radio-frequency (RF) resonators[33] that are bulkier than the individual qubits. However, to realize these advantages of sparser architectures, coherent spin shuttling must be integrated within a multi-qubit setting while maintaining universal control and efficient measurement[34–39].

In this work, we commission a sparse five-qubit array in silicon that leverages spin shuttling to enable long-range connectivity. In contrast to previous demonstrations with semiconductor spins, we characterize the array and tune logical control using shuttling in the absence of direct charge sensing. The resulting protocol allows for modular calibration and optimization, and it illustrates a viable alternative to

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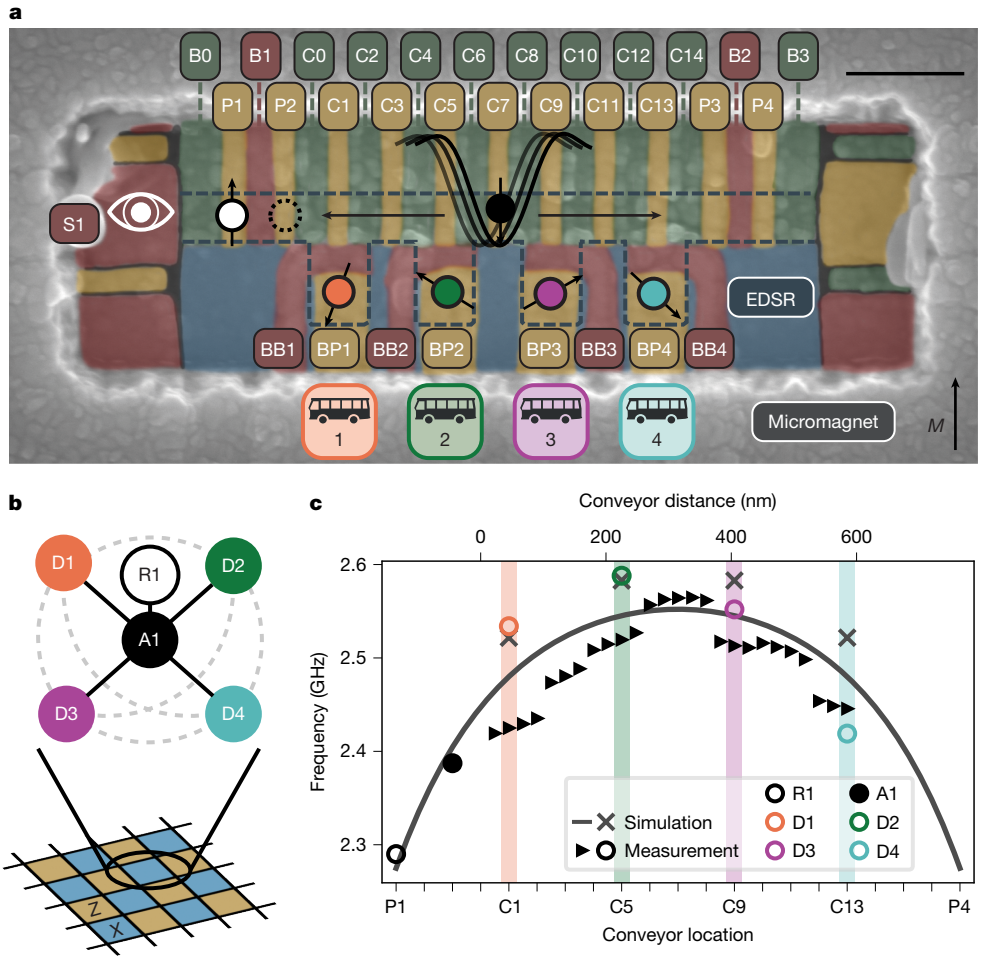

Fig. 1 | Device concept and shuttling bus. a, False-coloured scanning electron microscope image of a device nominally identical to that used in the experiments. Four metallization layers (from bottom to top: blue, red, yellow, green) are used to define a SET charge sensor (S1), the readout zone (B0–P2), the shuttling bus (C0–C14) and four bus stops (BP1–BP4). The readout zone on the right side of the device (P3–B3) is functional but unused, and no electrons are accumulated beneath P3 or P4. A cobalt micromagnet (grey) with residual magnetization *M* provides an inhomogeneous magnetic field profile to define and operate the qubits. No external magnetic field is present. The coloured spins correspond to the qubit labels in **b**. **b**, The qubit connectivity graph enabled by the shuttling bus. The solid lines indicate connections used in this work, whereby the shuttled ancilla qubit (A1) may interact with the four data qubits (D1–D4) as well as the readout ancilla (R1). This connectivity forms a surface-code stabilizer plaquette within a larger architecture. The dashed lines indicate connections that are physically available but unused in this work. **c**, The simulated and measured Larmor frequency profile along the shuttling bus axis. Analogous values for a spin localized under the bus-stop plungers (BP1–BP4) are plotted at the adjacent shuttling bus gates (C1–C13) and highlighted by the respective colours depicted in **a**. Scale bar, 200 nm (**a**).

the challenges of experimentally realizing dense qubit arrays. After outlining the measurement framework used to initialize and readout the multi-qubit state of the device, we benchmark the quantum processor and report the successful implementation of parity checks up to weight four as well as the creation of genuine entanglement between all qubit combinations in the array. These results highlight both the feasibility and the architectural benefits of incorporating shuttling into semiconductor quantum processors.

The sparse array, as shown in Fig. 1a, is electrostatically defined in the isotopically purified quantum well of a ^{28}Si/SiGe heterostructure ('Device fabrication' in Methods) and consists of three zones: a readout zone, a spin-shuttling bus and an adjacent row of quantum dots that we refer to as bus stops. At constant DC voltages, only the quantum dots formed under gates P1 and P2 are populated with 3 and 1 electrons, respectively, to form a qubit readout pair using parity-mode Pauli spin blockade (PSB) for spin-to-charge conversion ('Ancilla readout' in Methods). The adjacent sensor S1 is a single-electron transistor (SET) connected to an off-chip tank circuit such that RF reflectometry may be used to probe the charge state of the readout pair. The spin qubit R1, kept constantly below gate P1, is only used as a readout ancilla in this work, although it is fully controllable. The qubit A1, initialized below gate P2, functions as a mobile ancilla with which to characterize the sparse array and connect the qubits within it.

The overlapping gates C0–C14 in the top row of the array define the shuttling bus in the channel between the screening gates. The bottom row defines the bus stops with four individual plunger gates BP1–BP4 to accumulate four spin qubits, respectively D1–D4, and four adjacent barrier gates BB1–BB4 to control the tunnel couplings to the bus. The resulting connectivity graph, shown in Fig. 1b, corresponds to a weight-four stabilizer plaquette where each data qubit may directly interact with the ancilla qubit by coherently shuttling the latter to a position adjacent to the data qubit bus stop. The data qubits could also be shuttled and interact directly with one another for effective all-to-all connectivity[24], but we do not make use of these couplings in this work. It has been shown that extending such a bilinear architecture is conceptually sufficient to support the surface code[40], while the addition of more shuttling channels increases the architectural flexibility further[9].

The gate stack consists of four metallization layers and an on-chip micromagnet ('Device fabrication' in Methods). The bottom screening gate is used as a microwave antenna for driving resonant single-qubit

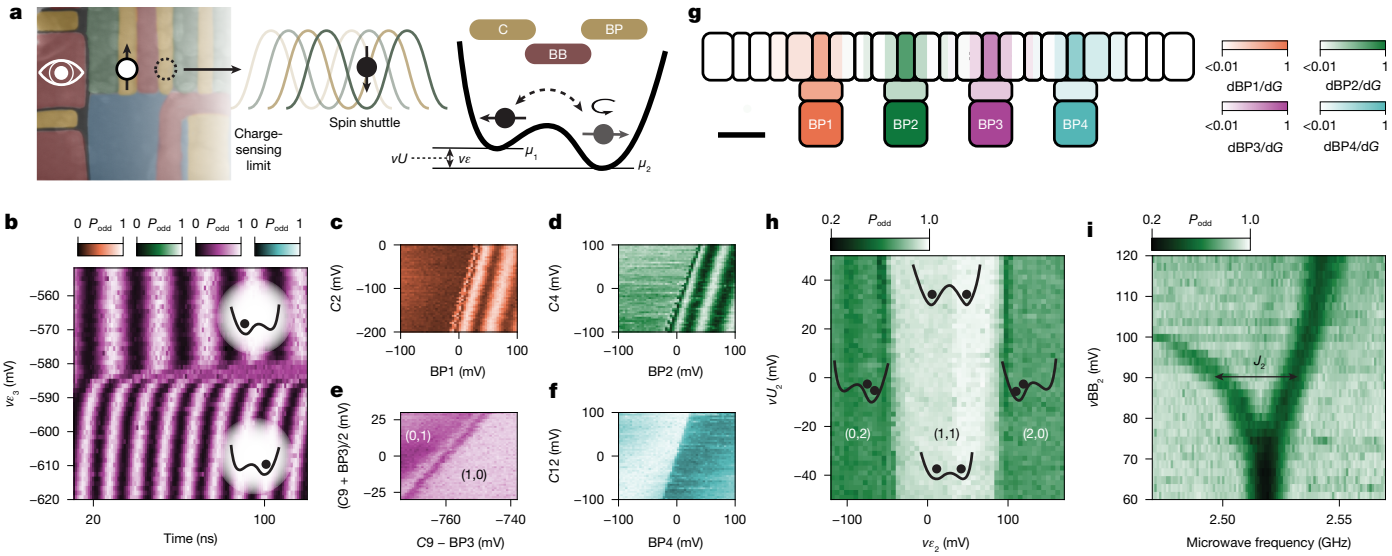

Fig. 2 | Remote-tuning protocols. a, Illustration of the remote-tuning concept. The sensor has a limited charge-sensing range and is therefore only used for qubit measurement of the ancilla spin. To probe control of the bus stops with chemical potentials μ_1 and μ_2, the ancilla is shuttled beyond the charge-sensing range, and spin physics is used to calibrate the virtual detuning $v\epsilon \propto \mu_1 - \mu_2$ and average chemical potential $vU \propto (\mu_1 + \mu_2)/2$ for all four effective double-dot systems formed at the bus stops ('Single-spin remote tuning' in Methods). **b**, An example of a Ramsey tunnelling experiment at bus stop 3. Coherent tunnelling of the ancilla spin from the shuttling bus to the bus stop is recognized by the abrupt change in Larmor precession frequency. Colour bars are shared with **c**–**f**. **c**–**f**, Examples of charge transitions identified via Ramsey tunnelling experiments for bus stops 1 (**c**), 2 (**d**), 3 (**e**) and 4 (**f**) with wait times on the order of tens of nanoseconds. The interdot charge transition between the shuttling bus and bus stop 3, which may be used to infer control of $v\epsilon$ and vU, is shown in **e**, whereas the other scans are used to extract other virtual gate matrix elements. **g**, Crosstalk heatmap of the influence of all individual gate voltages G with respect to the interdot charge transition between the bus and each bus stop extracted from scans analogous to those in **c**–**f** (Supplementary Fig. 6). Detectable crosstalk to multiple bus stops is indicated by split colouring. **h**, An effective two-electron charge stability diagram of the isolated double-dot system formed at bus stop 2 identified from the returned polarization of a shuttled spin. **i**, Detection of the exchange interaction strength J_2 between a shuttled spin and a mixed spin state in bus stop 2 obtained by applying microwave bursts at the charge-symmetry point as determined from **h**. See Extended Data Fig. 1 for analogous calibrations of all four bus stops. Scale bar, 100 nm (**g**).

gates and conditional rotations (CROT) via electric-dipole spin resonance (EDSR)[11]. Each labelled finger gate is controlled individually, although the experiments presented here are conceptually compatible with shared control of the shuttling bus[3,7].

The on-chip cobalt micromagnet is used to engineer the spin Hamiltonian of the array (Supplementary Note 2). After magnetizing the micromagnet in an external field of 1 T, the external field is turned off so that only the micromagnet remanence field remains. Figure 1c shows the simulated parabolic trend in Larmor frequencies of spins located along the bus axis along with the estimated Larmor frequencies of spins localized in the adjacent bus stops. These frequencies are experimentally probed by shuttling the ancilla spin prepared in a superposition with a resonant burst and measuring the relative change in Larmor precession. We use a four-phase travelling-wave potential to propagate spins through the bus[5,7,41], at a speed of 1.8 m s^{-1} ('Conveyor-mode shuttling' in Methods). The sudden steps in the measured trend indicate confinement potential roughness[42]. The shuttling operation is adiabatic, and the effective unitary acting on the spin is a phase pickup that can be calibrated explicitly or negated using a spin echo.

The conventional method of tuning spin-qubit arrays begins with using a charge sensor to tune quantum dots into known charge states, followed by using spin physics to calibrate and refine qubit interactions. In this device, direct charge sensing with S1 is possible only up to bus stop 1, so we pioneer a remote-tuning procedure that allows us to populate and virtualize control of the distant bus stops as well as tune single- and two-qubit operations without local charge sensing. Figure 2a provides a conceptual illustration where a spin is placed in a superposition and shuttled to a bus stop out of charge-sensing range. After pulsing the effective double-dot system to a particular balance of chemical potentials, the phase of the resulting superposition will depend on whether coherent tunnelling between dots occurred. This phase is measured by shuttling the spin back to the readout zone. Figure 2b depicts an instance of this tunnelling, similar to measurements performed in silicon metal-oxide-semiconductor and Ge/SiGe spin qubits while in the range of charge sensing[2,4].

By fixing the time of free evolution, single-electron charge stability diagrams are reconstructed from the shuttled spin phase as in Fig. 2c–f for all four bus stops. On the basis of the slope of the interdot transition, the relative capacitive coupling between all gates and the bus-stop quantum dot can be inferred and compensated through gate virtualization ('Single-spin remote tuning' in Methods). Figure 2g illustrates a heatmap of all such electrostatic crosstalk and highlights one of the benefits of increased dot separation. Although a few intermediate gates in the shuttling bus have a weak effect on two bus stops, the charge transition to each bus stop can be treated as effectively independent, allowing modular charge tuning of the array. Virtualization of the gates in the shuttling bus with respect to the bus-stop plungers prevents the occurrence of unintended electron transitions to the bus stops during shuttling. However, the bus-stop plunger gates are not virtualized with respect to the gates of the shuttling bus. We therefore expect the electrostatic potential in the shuttling channel to change when gate voltages are pulsed to accumulate data qubits, and we use two different conveyor definitions for charge loading and multi-qubit operation to account for this ('Conveyor-mode shuttling' in Methods).

After a spin has shuttled through the bus and tunnelled into a bus stop, we can load a new spin into the array on-demand from the sensor S1, which doubles as an electron reservoir, in approximately 10 μs ('Spin reloading' in Methods). To calibrate two-qubit logic between the ancilla qubit in the bus and a data qubit in a bus stop, the correct electrostatic balance in the effective double-dot system must be ensured. To do this, we initialize the ancilla to $|\downarrow\rangle$ after loading the bus stop with a mixed spin state. The ancilla spin is shuttled to be adjacent to the bus stop for

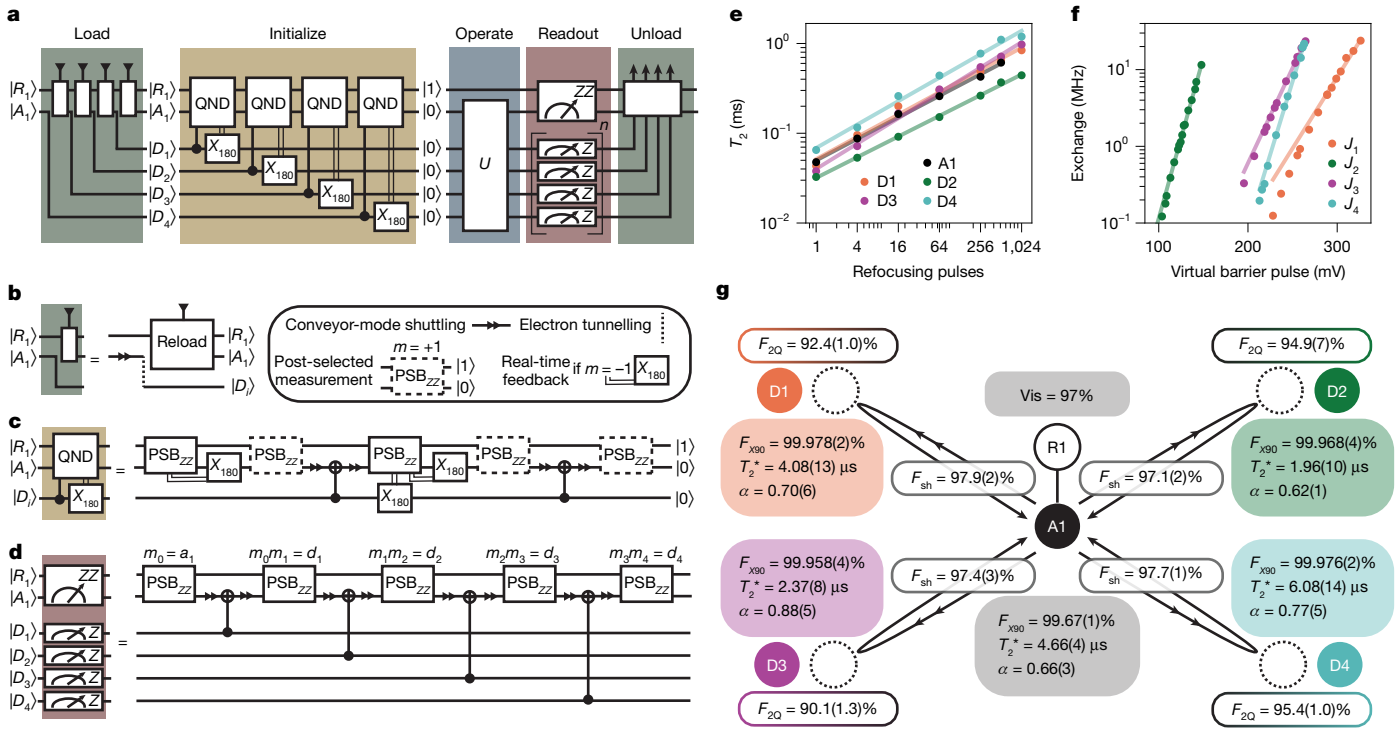

Fig. 3 | QND measurement framework and quantum processing unit characterization. a, Schematic showing the overall protocol for loading, initializing, measuring and unloading the sparse array when used as a quantum processor. **b**, Building block of the loading protocol. The ancilla qubit is shuttled along the bus, tunnels into the selected bus stop and is relabelled as a data qubit. A new ancilla is then reloaded from S1 as described in 'Spin reloading' in Methods. **c**, Building block of the initialization protocol. Two rounds of QND measurements are performed on the data qubit, with real-time feedback of the measured bit m used to correct the measured state of both the ancilla and data qubits. Post-selection is used to further boost the initialization fidelity by filtering certain error modes, such as infidelity in the CROT. A variable number of data qubits can be initialized in any order using this fixed building block at the expense of some redundancy, but this does not cause a meaningful performance bottleneck. **d**, Building block of the QND readout protocol. Extraction of the five-qubit computational-basis measurement bits a_1, d_1, d_2, d_3 and d_4 is elaborated in 'QND measurement' in Methods. **e**, Carr–Purcell–Meiboom–Gill (CPMG) coherence times T_2 measured for the ancilla qubit and four data qubits. Fits are according to an assumed $1/f^{\alpha}$ noise power spectral density ('Single-qubit characterization' in Methods). **f**, Exchange tunability of all four interactions between data qubits and the ancilla. Fits assume an exponential relation between barrier voltage and exchange. **g**, Overview of all benchmarked operations and qubit properties in the five-qubit processor ('Single-qubit characterization' and 'Two-qubit characterization' in Methods). The Ramsey coherence times T_2^* are averaged for about 25 min. The ancilla measurement fidelity is quantified by the visibility (Vis).

10 µs, and the polarization of the returned spin serves as a probe of whether tunnelling to or from the bus stop and subsequent spin mixing occurred. The resulting spin signal can be used to infer two-electron charge stability diagrams as shown in Fig. 2h. We note that such a method could form the basis for more rigorous spectroscopy of excited valley–orbital states far from local charge sensing as well.

After identifying the approximate symmetry point (where the virtual detuning $v\epsilon = 0$) of the two-electron charge state in each bus stop (Extended Data Fig. 1i–l), the exchange splitting is probed by modulating the bus-stop barrier gates to establish a suitable range for two-qubit interactions as shown in Fig. 2i. Exchange tunability on the order of 10 MHz is suitable for resonant-controlled rotations (CROT) and adiabatic controlled-phase (CZ) operations[11], both of which provide a universal entangling gate. Verifying the tunability of all four unique exchange interactions after sequentially loading all four bus stops confirms that the loaded spins are robust to the interleaved shuttling operations and suitable for calibrating quantum logic (Extended Data Fig. 1m–p).

To operate the sparse spin-qubit array as a five-qubit quantum processor, the protocol shown in Fig. 3a is used. First, all four data qubits are loaded into the bus stops in mixed states via shuttling the ancilla qubit and reloading as depicted in subcircuit Fig. 3b. After reloading the ancilla qubit for the final time, a quantum non-demolition (QND) protocol, expanded in Fig. 3c, is used to initialize both the ancilla and data qubits by measurement and using real-time feedback[39,43]. Direct initialization of the data qubits at the readout zone before shuttling is possible, but the QND protocol generally permits higher measurement fidelities owing to its repeatability. At the end of the initialization sequence, all spins are initialized in the ground state $|\downarrow\rangle \equiv |0\rangle$ with the exception of R1, which is initialized to $|\uparrow\rangle \equiv |1\rangle$. After universally controlling the spins with a combination of coherent shuttling, single-qubit EDSR and two-qubit exchange, they are measured using a generalized multi-qubit QND measurement, shown in Fig. 3d. The measurement yields up to five bits of information corresponding to the computational-basis measurement of the ancilla qubit and the four data qubits, and multiple rounds of QND measurement may be used to improve the readout fidelity of the data qubit states (Extended Data Fig. 2). After measurement, the pulsed gate voltages are returned to zero, and the bus-stop spins are unloaded before the next experimental cycle is initiated ('Spin reloading' in Methods). The dominant timescale is the 10 µs integration time associated with each PSB measurement, and the minimal duration of an experimental cycle is about 300 µs.

We use the QND measurement framework to calibrate and characterize all relevant operations for multi-qubit control using established methods ('Universal spin control' and 'Gate calibration protocols' in Methods). With dynamical decoupling, all qubits maintain coherence for hundreds of microseconds and show behaviour consistent with a $1/f^{\alpha}$ noise power spectral density as seen in Fig. 3e. We note that the data qubit coherence far exceeds the 10 µs readout time and permits

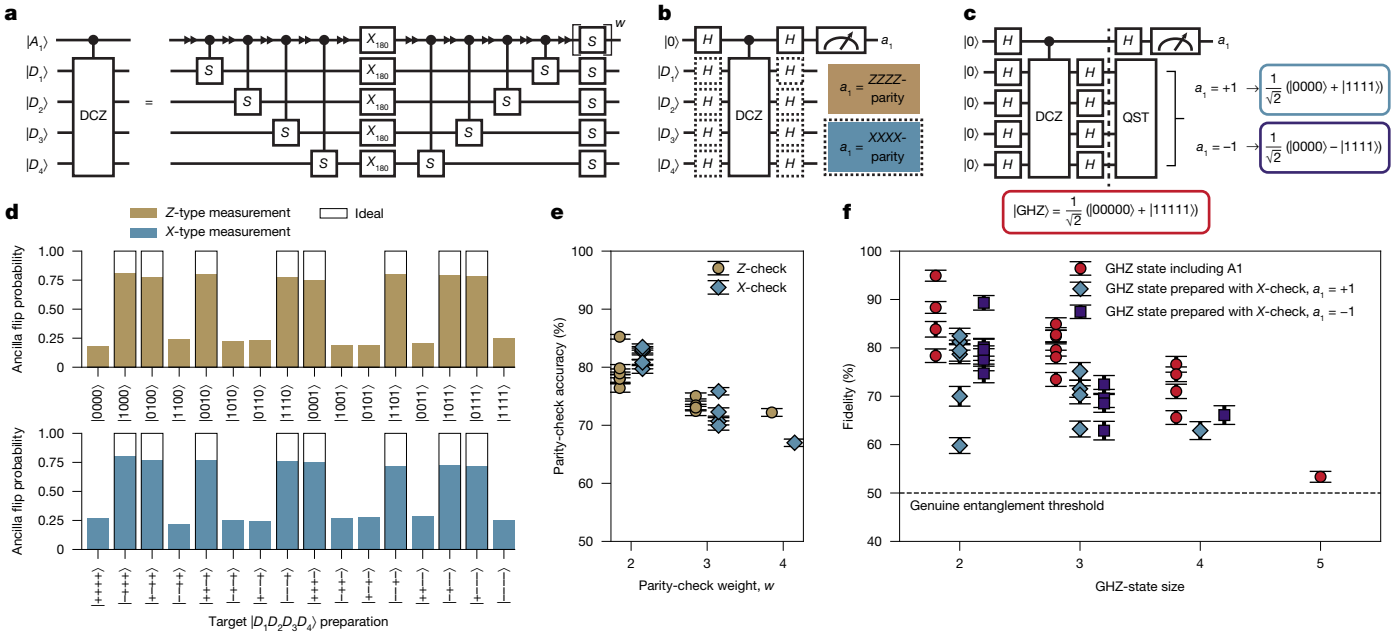

Fig. 4 | Benchmarking parity checks and multi-qubit entanglement. **a**, Quantum circuit depicting the multi-qubit DCZ used for coherent two-qubit operations. The circuit generalizes to any number w of data qubits by omitting or adding quantum wires of different data qubits. Single-qubit gates are parallelized pairwise when relevant, and the $2w$ S gates are applied virtually. **b**, Quantum circuit depicting a weight-four Z-type parity check utilizing the multi-qubit DCZ from **a**. The circuit generalizes to any number of data qubits by changing the weight w of the DCZ. An X-type check is performed with the inclusion of the dashed Hadamard gates. **c**, Quantum circuit depicting w-qubit GHZ-state generation using an X-type parity check. The dashed line indicates when the ancilla forms a $w+1$ qubit GHZ state with the data qubits, and the outcome of the ancilla measurement a_1 determines which of two GHZ states are realized in the data qubits. **d**, Outcomes of the weight-four Z-type (X-type) parity check obtained after preparing all Z-basis (X-basis) eigenstates of the data qubits. The black wireframes indicate the ideal result for each input state, and we estimate that data qubit initialization errors contribute a discrepancy of 2% in the observed ancilla outcome. **e**, The parity-check accuracy for all Z- and X-type parity checks of weights two to four, where error bars signify $\pm1\sigma$ as determined by Monte Carlo bootstrapping ('Parity-check analysis' in Methods). **f**, GHZ-state fidelities for all combinations of two or more qubits in the five-qubit processor (some overlap closely). State fidelities including the ancilla are calculated with respect to the GHZ state $\frac{1}{\sqrt{2}}(|0\rangle^{\otimes(w+1)} + |1\rangle^{\otimes(w+1)})$. For GHZ states initialized via a weight w parity check, the state fidelities are calculated with respect to $\frac{1}{\sqrt{2}}(|0\rangle^{\otimes w} \pm |1\rangle^{\otimes w})$. Error bars signify $\pm1\sigma$ as determined by Monte Carlo bootstrapping ('Quantum-state tomography' in Methods).

coherence-preserving mid-circuit measurements in this device[44]. Figure 3f illustrates the dynamic range of exchange tunability that is used to implement entangling two-qubit operations. Residual exchange between spins loaded in the bus stops is directly verified to be at least below 10 kHz, although it is probably much smaller, and therefore entangling crosstalk within the sparse array is negligible (Supplementary Fig. 11). We note that the residual exchange between data qubits and the ancilla is not relevant, as the ancilla never idles adjacent to any bus stop.

Figure 3g illustrates all benchmarks when the device is fully operational. Although the single-qubit fidelities F_{X90} are respectable when compared with the state of the art[34], we find that the two-qubit gate fidelities F_{2Q} are limited by incoherent noise in the exchange interaction strength (Extended Data Fig. 3). Previous demonstrations in two-qubit devices show that the technology is capable of two-qubit gate fidelities well over 99% (refs. 35–37,45,46). In Methods, we discuss multiple improvements, including modest device and set-up design changes as well as modifications to the gate stack, that should make such performance possible in our shuttling architecture.

We characterize the 1.2-µm round-trip shuttling path to have a single-qubit fidelity F_{sh} of 97.7(1)% with respect to an identity operation when the array is operated as a five-qubit processor. The largest error contribution is associated with the charge transition from below P2 to C0. We estimate the remaining infidelity to be consistent with dephasing and discuss the possible role of valley excitations further in 'Single-qubit characterization' in Methods. Although higher shuttling fidelity has been reported over a larger cumulative distance[5], our results demonstrate the longest coherent spin shuttle over a real distance in silicon. Although further refinement of the travelling-wave potential would probably enhance both the speed and fidelity of shuttling by reducing dephasing, the total error budget for operating all five qubits is dominated by the two-qubit interactions.

To demonstrate both phase-coherent two-qubit interactions and the utility of the shuttling-enabled connectivity across the full system, we demonstrate up to weight-four parity checks of the data qubits and five-qubit entanglement. A central consideration for operating multi-qubit registers with shuttling is that moved spins will accrue phase in the rotating frame in which they are being resonantly controlled. In this device, the ancilla qubit will pick up a phase as it travels in the inhomogeneous magnetic field. The data qubits, although stationary, also pick up a phase owing to the stray electric fields from the shuttling pulses coupling to the spins via the magnetic-field gradient. These phases depend on the shuttling path and the number of two-qubit interactions carried out on the way, and therefore may lead to a large overhead in the number of calibrated parameters.

To avoid this, we perform two-qubit logic using a decoupled CZ (DCZ) gate shown in Fig. 4a. In addition to decoupling low-frequency noise, the X_{180} gates also refocus the single-qubit phase pickups acquired during both shuttling and two-qubit gates provided the operation is symmetric. The pairs of native conditional S gates are implemented by adiabatically modulating the exchange interactions, which commute with the refocusing pulses, and enable a maximally entangling operation between the ancilla and any combination of the data qubits depending on which two-qubit interactions are enabled. The single-qubit operation on the ancilla has the highest quality when the spin is localized below gate P2, and therefore the implemented DCZ operation uses

two rounds of shuttling ('Single-qubit characterization' in Methods). However, this is not a fundamental requirement of the approach.

The parity of any multi-qubit Pauli operator acting on any subset of the data qubits can be extracted with the appropriate change in basis of the data qubits as shown in Fig. 4b. In our implementation, the shortest weight-four parity-check circuit has a duration of 4.84 µs. Figure 4c shows how a weight-w X-type parity check acting on an input state $|0\rangle^{\otimes w}$ is used to probabilistically generate maximally entangled w-qubit states that differ by a single-qubit Pauli operation. In the case of a weight-four parity check, one of the post-selected states is the logical state of a $[\![4, 1, 2]\!]$ surface code whereas the other state is outside of the code space. We can therefore benchmark the quality of the parity checks in two ways. First, we ensure that all eigenstates of Z- and X-type parity observables are detected and preserved properly. Second, we generate multi-qubit entanglement generated via the parity checks as a more stringent test of the parity-check performance.

Figure 4d shows the measured ancilla state when weight-four Z- and X-type parity checks act on all of the respective input eigenstates. Imperfections between the ideal ancilla outcome and the measured parity result from imperfect state preparation of ancilla and data qubits, finite ancilla measurement fidelity, finite ancilla shuttling fidelity, and finite single- and two-qubit gate fidelity. In addition, we measure the data qubit state after the parity check and calculate the parity-check accuracy as the probability that both the ancilla outcome is correct and the intended prepared state is observed. Figure 4e tabulates this parity-check accuracy for all data qubit combinations. The weight-four parity-check accuracy of 72.2(6)% (67.0(7)%) therefore establishes the quality with which the parity of the *ZZZZ* (*XXXX*) eigenbasis can be detected and conserved. These benchmarks are in reasonable agreement with the estimated accuracies of 70.5% and 70.0% (Methods). The primary difference between X- and Z-type checks is the larger number of single-qubit rotations required in the former case and the additional dephasing incurred while performing them. All other parity checks are shown in Extended Data Fig. 4. In Extended Data Fig. 5, we show an example of performing 35 repeated weight-two parity checks with a retention rate above 93%.

When benchmarking the check performance on eigenstates, the data qubits are ideally $|0\rangle$ or $|1\rangle$ throughout the DCZ operation and, owing to the long T_1 relaxation times of spin qubits, are robust to decoherence. The generation of entanglement is therefore a stronger test of the parity-check performance, as the quantum state of the system will be maximally sensitive to operational errors, including the error rates associated with spin shuttling and crosstalk. Figure 4f tabulates the Greenberger–Horne–Zeilinger (GHZ) state fidelities of all combinations of entangled states possible in the five-qubit processor. After accounting for measurement errors, the observed fidelities are comparable to the best multi-qubit entangled states generated with gate-defined semiconductor spins[39,47,48], and we observe genuine five-qubit entanglement ($F_{\mathrm{GHZ}} > 50\%$) in the platform. All reconstructed density matrices are shown in Extended Data Figs. 6–9 along with the estimated fidelities in the absence of initialization and readout error removal.

By post-selecting the state of the ancilla measurement, we probabilistically initialize the data qubits into the logical state of a $[\![4, 1, 2]\!]$ surface code with a state fidelity of 62.9(1.8)%. This central result highlights that our implementation of parity checks is suitable for more sophisticated QEC experiments. We note that this procedure requires five-qubit entanglement, and we demonstrate higher four-qubit GHZ-state fidelities up to 76.6(1.6)% with qubit combinations that include the ancilla. In Extended Data Fig. 10, we formulate a budget of all characterized error sources and conclude that the majority of the error originates from infidelity in the two-qubit exchange interactions. Dephasing during shuttling and idling constitutes about a quarter of the total error, and increasing the speed of shuttling is the most direct means to lower this contribution.

The incorporation of spin shuttling into a multi-qubit setting has implications for both how semiconductor spin-based quantum processors are operated and the level of performance they can achieve. We have shown that shuttling can be used to tune universal multi-qubit control without the need for local charge sensing throughout an array. The presented tuning protocols are only limited by the distance over which the shuttling operation maintains spin coherence. With high-fidelity shuttling already demonstrated over an effective 10 µm length scale[5], we expect that the approach presented here is sufficient to tune on the order of 100 qubits using a single charge sensor and ohmic contact in prototype industrial layouts[49] ('Single-spin remote tuning' in Methods). Owing to the lower degree of electrostatic crosstalk in sparse arrays, this calibration would be modular and scale linearly with the number of qubits in the worst case. The addition of more shuttling channels further increases architectural flexibility and will be essential to avoid a measurement bottleneck. In larger fault-tolerant architectures, this allows charge sensors to be located where they are optimal for ancilla measurements rather than being necessary for device tune-up.

Despite the finite fidelity of shuttling, we have shown that generating and preserving multi-qubit entanglement is not only versatile but also has been achieved over more spins than in past experiments. The connectivity enabled by shuttling allows QND parity-check measurements to be performed on flexible combinations of non-local data qubits. Importantly, the present device architecture is sufficient for realizing near-term QEC experiments with Loss–DiVincenzo spin qubits. As a concrete example, the error-detecting $[\![4, 2, 2]\!]$ rotated toric code, which was recently demonstrated with exchange-only spin qubits[50], could be implemented. The operational right side of the device could be used as a second mobile ancilla and readout zone, and mid-circuit measurements, which are possible in our device but not characterized in this work, would be necessary[44]. As detailed in Supplementary Note 3, we estimate that 20 rounds of error detection within the average coherence time of the physical data qubits could take place.

The present work illustrates how the mobility of semiconductor spin qubits can be used to realize all the essential ingredients for building logical qubits with physical operations that have all been individually demonstrated at fault-tolerant fidelities[5,35,37,38]. Beyond the present architecture, the non-planar connectivity possible in larger spin-shuttling devices would permit more exotic encodings as well. By combining the high fidelities and long coherence times that are now routinely demonstrated in industrially fabricated devices with the versatile and extensible control possible in sparse architectures, semiconductor spin qubits can be a powerful platform for large-scale quantum information processing.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-026-10766-3.

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Methods

Device fabrication

The device is fabricated on an isotopically purified ^{28}Si/SiGe heterostructure containing a 7-nm-thick strained quantum well[19], 30-nm SiGe buffer passivated with an amorphous silicon cap, and a 10-nm atomic layer deposition of insulating Al_2O_3. The heterostructure is nominally equal to that in previous studies where large average valley splitting in excess of 200 μeV (ref. 19) and high-fidelity shuttling[5] have been observed. The four proceeding Ti:Pd layers have thicknesses of 3:17 nm, 3:27 nm, 3:27 nm and 3:27 nm respectively and are each followed by 5-nm atomic layer deposition of Al_2O_3. Finally, a 3:150 nm Ti:Co micromagnet is evaporated. The gate layer order is selected (refer to Fig. 1a) to maximize the tunnel coupling tunability for two-qubit interactions between the ancilla and data qubits as well as the interaction between the PSB pair, as gates in higher layers typically exhibit lower lever arms to the buried quantum well[51].

Experimental set-up

The experiments were performed in an Oxford Instruments ProteoxMX dilution refrigerator where the mixing chamber temperature was held at 200 mK to mitigate heating effects[52]. A driven superconducting vector magnet was used to magnetize the on-chip micromagnet in a field of 1 T and is otherwise unpowered. The device was glued with GE varnish to a copper plate in direct thermal contact with the mixing chamber and was wirebonded to an in-house printed circuit board (PCB). We applied DC bias voltages supplied by battery-powered home-built voltage source modules (D5a) and generated baseband control and readout pulses with a Qblox Cluster equipped with eight 4-channel QCM arbitrary waveform generator (AWG) modules and a QRM module for RF reflectometry readout. DC channels were filtered with a combination of PI and RC filters with a nominal cut-off frequency of about 20 Hz. Alternating current (AC) channels were filtered by ferrite chokes, passed through UT85 stainless steel semi-rigid coaxial cables and attenuated by 20 dB at 4 K to balance thermalization and have a large dynamic range for baseband pulsing. The ±2.5 V output range of the AWG channels corresponded to a ±500 mV available range at the device. The DC and AC signals were combined through bias tees with a time constant of 100 ms. Two channels of a QCM module are used for IQ modulation of a Rohde & Schwarz SGS100A vector source. We set the local oscillator of the vector source to 2.27 GHz to ensure that all target qubit frequencies fall on the same sideband within the 400-MHz bandwidth of the QCM. The output power of the vector source was set to 6 dBm.

The RF tone for readout was generated by the QRM, attenuated by 40 dB at room temperature and 20 dB at 4 K, and the input and output signals passed through a MiniCircuits ZEDC-15-2B directional coupler at the mixing chamber stage. The input power was set to optimize the signal-to-noise ratio of charge sensing. The output signal was carried through a superconduting NbTi UT85 cable to a Cosmic Microwave Technologies CMT-BA1 cryogenic amplifier mounted at the 4 K stage, which provides approximately 30 dB of amplification. The signal was further amplified at room temperature with a home-built amplifier (standalone M2j), which provided an additional 45 dB of amplification before being filtered, digitized and demodulated by the QRM. The demodulated signal was digitally rotated to the in-phase component to make use of real-time feedback.

Initial device testing and tuning procedure

After cooling below 1 K, RF reflectometry was verified by finding the LC circuit resonances with a spectrum analyser. We then proceeded to verify DC transport through both SET structures as well as the conveyor channel. This is shown for the latter in Supplementary Fig. 4. Although the adjacent bus-stop gates cannot pinch off the channel entirely, their large effect on the conducted current is an indication that they operate normally, as shown in Supplementary Fig. 5. After verifying DC transport, we benefited from a complete thermal cycle to reset hysteresis before tuning up sensors with RF reflectometry.

The pinch-off voltages within the channel provide a first guideline for DC voltages that allow the device to be accessible by shuttling. We find that the channel gates in the same layer pinch off with reasonable uniformity around 1 V. To avoid unwanted static charge accumulation under the conveyor, we therefore set their preliminary DC voltages in the range of 700–800 mV. As the DC tests on the bus-stop gates do not provide such a quantitative guideline, we rely on electrostatic simulations to estimate the bus-stop gate voltages needed to create a balanced double-dot potential with the corresponding conveyor gate. We extract roughly a factor 1.5 and 1 for the bus-stop plunger and barrier, respectively, compared with the conveyor gate voltages. We therefore set the bus-stop plungers to 1,200 mV and the bus-stop barriers to 750 mV as a reasonable starting point to tune the array.

After verifying DC functionality, the device tune-up proceeds in the following sequence: (1) ancilla readout and control, (2) coarse conveyor-mode shuttling, (3) single-spin remote tuning and virtual gate matrix calibration, (4) spin reloading, (5) two-spin remote tuning and exchange detection, (6) optimization of coherent conveyor-mode shuttling, (7) CROT tuning and implementation of the QND measurement framework, and (8) single- and two-qubit gate calibration.

Ancilla readout

Charge sensing was achieved via an RF SET measurement. The 2D electron gas (2DEG) leads of each SET were accumulated according to the split-gate method, where the RF signal was capacitively coupled to the 2DEG via an accumulation gate to minimize series resistance and remove leakage pathways[53]. An LC tank circuit was formed with a NbTiN meandering superconducting nanowire with a nominal kinetic inductance on the order of a few microhenry, the series capacitance between the accumulation gate and the 2DEG, and the parasitic capacitance between the bond wires and the PCB ground plane, giving rise to a resonance frequency of 114.3 MHz.

Spin-to-charge conversion was achieved via parity-mode PSB. The Zeeman energy difference of about 100 MHz between the readout ancilla R1 and ancilla A1 lifts the blockade of the $|T_0\rangle$ spin triplet, resulting in an effective $Z \otimes Z$ observable for the qubit pair[54]. The (4, 0)–(3, 1) interdot charge transition was used such that R1 occupies the dot where the lowest valley–orbit shell is filled, increasing the energy required to lift the blockade. A charge stability diagram of this region can be seen in Supplementary Fig. 7b.

PSB was first tuned in isolation mode, where the tunnel barrier to the reservoir (S1) was completely closed, as this makes the visual characteristic easier to recognize during manual tuning with video-mode charge-state measurements while sweeping the respective plunger gates of the PSB pair. After initial identification of the qubit resonances, PSB was retuned with a finite reservoir coupling to allow for efficient qubit reloading.

The tunnel coupling between the quantum dots of the readout pair was pulsed to be on the order of several gigahertz such that the singlet state $|S(4, 0)\rangle$ evolves adiabatically to the $|\uparrow\downarrow\rangle$ spin state of the (3, 1) configuration with a 50-ns linear voltage ramp. This allows for the initialization of an unblockaded $|\uparrow\downarrow\rangle$ state via post-selection. Real-time feedback serves to enhance the fraction of post-selected measurement shots by flipping the state of A1 if blockade is detected during initialization. Although we conceptually identify the ancilla qubit as the single-spin A1 that is shuttled through the device, it is technically correct to attribute the qubit to the parity of the $|R_1\rangle \otimes |A_1\rangle$ spin state. The initialization and readout protocols of Fig. 3 only require PSB to be parity-preserving to function correctly.

After achieving reasonable readout visibility with manual tuning, the visibility of Rabi oscillations was used as a cost function for a CMA-ES optimizer to maximize the quality of initialization and readout[55]. The optimizer takes as parameters the voltage pulse amplitudes on all gates

immediately surrounding the double-quantum-dot system hosting the readout pair, as well as the durations of piecewise-linear voltage ramps defining the readout sequence. We routinely achieve ancilla qubit visibilities of about 97% with such an optimization, corresponding to initialization and readout error rates of about 1%, while using an integration time of 10 μs. The integration time is selected such that spin readout is stable over periods of at least 1 day without requiring more frequent recalibration. We note that similar performance can be achieved by shortening the integration time to as low as 5 μs at the expense of requiring more interleaved threshold calibrations. In the future, the optimal integration time must balance the quality of readout with the dephasing incurred by other spins during coherent mid-circuit measurements.

Conveyor-mode shuttling

To generate the travelling-wave potential for the shuttling bus, we make use of a four-phase conveyor-mode pulse template as in refs. 3,5,7,41. The goal is to generate a smooth moving-dot potential that minimizes the decoherence of a shuttled spin[42,56–59]. During conveyor operation, every participating virtual gate $v\mathrm{G} \in \{v\mathrm{C0}, \ldots v\mathrm{C12}, v\mathrm{U}_1, v\epsilon_1, \ldots, v\mathrm{U}_4, v\epsilon_4\}$ is assigned a voltage vG such that:

$$vG(t) = vG^{\mathrm{offset}} + vG^{\mathrm{amp}}\sin(2\pi f_{\mathrm{conv}}\, t - \phi_G), \quad (1)$$

where $\phi_G = m\pi/2$ for integer $m \in \{0,1,2,3\}$ such that every fourth virtual gate is in-phase. $v\mathrm{U}_{1-4}$ and $v\epsilon_{1-4}$ are used in place of vC1, vC5, vC9 and vC13 to avoid unwanted charge transitions at the bus stops during shuttling. All gate voltages oscillate with the conveyor frequency f_{conv}, and the constant offsets vG^{offset} and amplitudes vG^{amp} are unique to each individually controlled gate. The set of parameters $\{f_{\mathrm{conv}}, vG^{\mathrm{offset}}, vG^{\mathrm{amp}}\}$ constitutes a conveyor definition. The pulses are applied in addition to the constant DC bias voltages vG^{DC}.

All shuttling experiments begin with the ancilla A1 located below P2. A linear voltage ramp to $\{vG(0)\}$ pulls the charge below C0, and the travelling-wave potential minimum progresses by four gate lengths for every conveyor cycle of duration $t_{\mathrm{conv}} = 1/f_{\mathrm{conv}}$. The ancilla is therefore localized adjacent to bus stops 1–4 at $t/t_{\mathrm{conv}} = 0.25, 1.25, 2.25, 3.25$, respectively. When the conveyor voltages are held constant at a fixed time, additional gate voltage pulses (for example, for activating an exchange interaction) are applied in linear combination with the paused conveyor. The direction of the travelling-wave potential is reversed by flipping the sign of f_{conv} and adding a time-dependent offset to ensure that there is no sudden discontinuity in the conveyor. The charge returns from below C0 to below P2 by linearly ramping all conveyor voltages to zero.

Two conveyor definitions are used during the operation of the array. The first is a coarse-tuned conveyor that is used to shuttle uninitialized spins past unpopulated bus stops during loading and unloading. This is achieved by manually tuning $\{vG^{\mathrm{amp}}\}$ and, if necessary, the DC gate voltages, to ensure good charge shuttling fidelity. Coherent spin-shuttling fidelity is unimportant for this conveyor definition. The coarse conveyor is tuned by using adiabatic inversion to infer the movement of the spin in the inhomogeneous magnetic field.

The second conveyor definition is used when the bus stops are loaded with single electrons, and therefore the electrostatic landscape of the bus is different than during loading (which is ordered from bus stop 4 to bus stop 1 to avoid this issue). Here, coherent spin transfer is relevant, and we make use of CMA-ES optimization to fine-tune $\{vG^{\mathrm{offset}}, vG^{\mathrm{amp}}\}$. As a cost function, we use an echo-type experiment where the spin is shuttled ten times back and forth in total from P2 to C13[55]. The spin visibility serves as a proxy for the dephasing experienced during shuttling, making it an easy-to-evaluate cost function for optimization.

The Larmor frequencies along the optimized conveyor, as shown in Fig. 1c, are extracted by preparing the shuttled spin in superposition and observing the precession frequency after transporting the spin to various points along the array.

Single-spin remote tuning

After confirming the operation of the shuttling bus, the loading protocol of the bus stops can be tuned. For this, we leverage the availability of EDSR throughout the bus to perform Ramsey experiments with respect to various rotating frames, but we note that the strategy we use is compatible with not having single-spin control throughout the array. The minimum requirement is the ability to prepare a spin in a superposition state and shuttle it coherently.

During initial tuning, no gate virtualization has taken place beyond the readout zone, and the ability to load the bus stops is probed by applying a physical detuning pulse $\epsilon_i = Cj - \mathrm{BP}i$ where Cj is the voltage of the conveyor gate adjacent to bus stop i ($j = 1, 5, 9, 13$ for bus stops 1–4 respectively). Extended Data Fig. 1a–d shows the first convincing experimental signatures of bus-stop loading before any virtualization takes place. To verify that the bus stop is the most likely destination for the tunnelled electron, we repeat the loading experiments while pulsing negatively on the surrounding conveyor gates. This provides evidence that tunnelling is not taking place within the shuttling bus.

The Larmor frequency difference between the spin when localized in the bus and in the bus stop encodes information about its position in the phase of the spin state. For each bus stop, we select a free evolution time on the order of tens of nanoseconds to optimize contrast between the two cases, and we use this signal to virtualize control of the effective double-dot system as well as the surrounding conveyor gates. First, we focus on the gate voltage subspace consisting of the physical conveyor gate voltage Cj and physical bus-stop plunger gate voltage BPi. In the case of bus stop 1, these gates are already virtualized with respect to the readout zone, but not to each other, and the following procedure is the same regardless of any pre-existing virtualization.

We define unvirtualized detuning and average potential parameters ϵ_i, U_i that relate to voltages Cj, BPi as $(\epsilon_i, U_i)^{\mathrm{T}} = V(Cj, \mathrm{BP}i)^{\mathrm{T}}$ where:

$$V = \begin{pmatrix} 1 & -1 \\ 0.5 & 0.5 \end{pmatrix}. \quad (2)$$

We want to identify corresponding virtual gates vCj and vBPi, where $(vCj, v\mathrm{BP}i)^{\mathrm{T}} = M_i(vCj, \mathrm{BP}i)^{\mathrm{T}}$, such that the virtual detuning and average potential, defined as $(v\epsilon_i, U_i)^{\mathrm{T}} = V(vCj, v\mathrm{BP}i)^{\mathrm{T}}$, relate to the double-dot chemical potentials as sketched in Fig. 2a. Explicitly, this means $v\epsilon_i \propto \mu_{Cj} - \mu_{\mathrm{BP}i}$ and $vU_i \propto (\mu_{Cj} + \mu_{\mathrm{BP}i})/2$ where μ_{Cj} and $\mu_{\mathrm{BP}i}$ are the chemical potentials of the dots formed below gates Cj and BPi, respectively. An interdot charge transition to bus stop i should therefore only be modulated by $v\epsilon_i$.

The interdot charge transitions measured when sweeping the physical detuning and average potential parameters (Supplementary Fig. 6a) show a finite (positive) slope $\mathrm{d}\epsilon_i/\mathrm{d}U_i = \tan\theta_i$ from which it follows that $(v\epsilon_i, vU_i)^{\mathrm{T}} = R(\theta_i)(\epsilon_i, U_i)^{\mathrm{T}}$ where $R(\theta_i)$ is an anticlockwise rotation about the origin ($\epsilon_i = v\epsilon_i = 0$, $U_i = vU_i = 0$) by an angle θ_i. We therefore have $M_i = V^{-1}R(\theta_i)V$. Applying the elements of M_i to the total virtual gate matrix permits direct control over the virtual detuning and average potential.

To virtualize any other gate G with respect to each bus-stop plunger BPi, the same experiment definition is used where the slope $\mathrm{dBP}i/\mathrm{d}G$ of the interdot transition informs both the degree of influence of the gate voltage G on the chemical potential below gate BPi and therefore the virtual gate definition vG required to offset the effect (Supplementary Fig. 6b). The slope $\mathrm{dBP}i/dCj = (2 - \tan\theta_i)/(2 + \tan\theta_i)$. This provides all slopes plotted in the crosstalk heatmap of Fig. 2g.

Extended Data Fig. 1e–h shows the loading experiments repeated after gate virtualization has taken place. In certain cases, the tunnel coupling between the bus and bus-stop dots is pulsed during tunnelling to smoothen the transition compared with the preliminary loading. The two-electron charge stability diagrams reconstructed from the shuttled spin polarization in Extended Data Fig. 1i–l also show charge

transitions that are effectively orthogonal to the virtualized detuning axis, confirming the validity of this approach.

We estimate that this remote-tuning strategy would be sufficient to tune on the order of 100 qubits at bus-stop-like locations in a sparse quantum-dot array. Taking a trilinear quantum-dot array as an example[49,50], with the central row operated as a shuttling channel, we could envision placing a single charge sensor and reservoir at one end and shuttling a distance on the order of 10 μm. As demonstrated in ref. 5, coherent spin shuttling with high fidelity over such a distance should be possible, although we emphasize that high fidelity is not necessary for our remote-tuning protocol to function. On the basis of our device geometry, we estimate that a total of 110 bus stops would fit adjacent to such a shuttling channel. With a shuttling speed of 50 m s^{-1} and a spin reload time on the order of 1 μs, loading every bus stop would require about 120 μs. Even with AC loading, this timescale is still well within the 100-ms bias-tee time of our sample board.

In this extreme example, qubit measurement for the purposes of quantum information processing would be impractically slow. However, it illustrates that shuttling can be used to massively multiplex tuning and qubit readout well beyond what is currently possible with dense spin arrays.

Spin reloading

Supplementary Fig. 7a illustrates the procedure used for reloading a new spin into the array after the original ancilla has been shuttled to occupy a bus stop. The sensor S1 doubles as an electron reservoir from which qubits can be loaded on-demand. It has a small but finite tunnel coupling to the dot below P1 where the readout ancilla R1 remains and a weaker coupling to the dot below P2 where the ancilla A1 is initialized as can be seen in the measured charge stability diagram of Supplementary Fig. 7b.

After shuttling the ancilla, the voltage configuration in the readout zone remains at the operation point *O* in the quasi-equilibrium (3, 0) charge state. As the direct tunnel rate to (3, 1) is very slow, this charge configuration persists for at least 20 ms and is limited by the bias-tee charging time of the sample PCB. No unwanted electrons tunnel into the empty dot during the experiments. To reload on-demand, the virtual detuning of the readout pair $v\epsilon_R$ is pulsed to the reload point R. The rate at which a new charge enters is evident from Supplementary Fig. 7c. Pulsing beyond the PSB region of the interdot transition allows for a relatively fast loading to the (4, 0) state in less than 10 μs, and ramping the detuning back to *O* returns the system to the equilibrium (3, 1) charge state and restores the ancilla spin. No additional barrier pulse (that is, on gate B0) is used to modulate the tunnel rate, and including one could increase the loading speed further. This reloading procedure repeats until all bus stops are occupied and the final ancilla spin is reloaded, after which the initialization protocol may begin.

The bus-stop spins are unloaded in one of two ways. First, they may be shuttled back to the readout zone in a sequence inverse to the loading protocol. In this case, the 5-electron charge state at the readout zone quickly equilibrates to the (3, 1) charge state in about 1 μs, and no detuning pulse is necessary. Alternatively, we can simply ramp all pulsed voltages back to their DC condition without any travelling-wave potential used. Bias-tee compensation pulses are applied over a period of several tens of microseconds before the next experimental shot begins, and the free spins vacate the bus stops within this timescale, presumably to one of the 2DEG reservoirs on either side of sparse array. We observe no adverse consequences when unloading spins in this manner, and this approach is used for most experiments presented in this work.

The necessity for unloading and subsequent loading is set by the finite bias-tee time and amplitude range of the AWG modules. In future work, loading bus stops or other remote quantum dots with DC voltages would eliminate the need for spin reloading altogether.

QND measurement

All qubits in the effective five-qubit processor can be measured in the computational basis as illustrated in Fig. 3d by a sequence of parity-mode PSB measurements $m_0, m_1, m_2, \ldots$. We use the convention that each projective measurement ideally yields $m_k = +1$ when an odd-parity spin state $|R_1\rangle \otimes |A_1\rangle$ is present and $m_k = -1$ when an even-parity spin state is present.

The ancilla is always measured first. By assuming that R1 remains in the prepared eigenstate $|1\rangle$ throughout all experiments, $m_0 = a_1$ gives the computational-basis measurement outcome of qubit A1. To perform a QND measurement on a data qubit D*i*, A1 is shuttled adjacent to the relevant bus stop and a calibrated CROT will flip the state of A1 conditional on the data qubit being in the $|1\rangle$ state. The next measurement m_k indicates whether an ancilla spin-flip took place by considering the previous measurement m_{k-1}. The *k*th computational-basis readout $d_{i,k}$ of D*i* is therefore given by the product $m_{k-1}m_k$.

Unlike for the ancilla measurement, repeated QND measurements can take place on the data qubits to improve the readout fidelity as indicated in Fig. 3a. To characterize the quality of the repeated QND readout, we perform Rabi oscillation measurements with 20 sequential QND readouts on the 4 data qubits individually. Extended Data Fig. 2a gives an exemplary circuit for D2. The QND single-shot outcomes $\{d_i\} = \{d_{i,1}, d_{i,2}, \ldots, d_{i,20}\}$ are used to infer the data qubit D*i* $|1\rangle$ state probability $P_1(t_b)$ through a majority-vote scheme. The resulting oscillation is fit to $P_1(t_b) = B - A\cos(2\pi f_R t_b)\exp(-t_b/T_2^R)$, where t_b is the microwave burst time, f_R is the Rabi frequency, and T_2^R is the Rabi oscillation decay time. Extended Data Fig. 2b shows the visibility, given by 2*A*, of the Rabi oscillations as a function of the number of QND readout cycles used in the majority vote. We use up to five QND repetitions in our experiments, as this yields the highest visibility for all data qubits.

We also characterize the QND fidelity of our readout, which quantifies the ability of the QND measurement to preserve the data qubit $|0\rangle$ and $|1\rangle$ states. We again utilize the 20 repetitive QND readouts but calculate the Rabi oscillation from each individual outcome $d_{i,k}$. This results in Rabi oscillations with decaying amplitudes and offsets as the data qubit state is disturbed by finite CROT fidelity and spin relaxation. The individual Rabi oscillations $P_{1,k}(t_b)$ are fitted to obtain the amplitude A_k and offset B_k for the *k*th QND measurement repetition. The decay of these parameters is then fitted using the model[60]:

$$A_k = A_0 \gamma^k, \tag{3}$$

$$B_k = \left(B_0 - \frac{1-\gamma_0}{1-\gamma}\right)\gamma^k + \frac{1-\gamma_0}{1-\gamma}, \tag{4}$$

where $\gamma_0 = \exp(-t_{QND}/T_1^{(0)})$, $\gamma_1 = \exp(-t_{QND}/T_1^{(1)})$ and $\gamma = \gamma_0 + \gamma_1 - 1$. t_{QND} is the time required for a cycle of QND measurement, which in our case is about 12 μs for all four data qubits, $T_1^{(0)}$ is the spin-flip time of the data qubit $|0\rangle$ state, and $T_1^{(1)}$ is the spin-flip time of the data qubit $|1\rangle$ state. We observed a decay in A_k for all data qubits. However, only data qubit D4 shows a decay in B_k; the remaining data qubits show no visible decay over the 20 QND repetitions. We conclude that the QND readouts of D1, D2 and D3 are mainly limited by unintentional data qubit spin flips owing to the CROT infidelity, whereas the QND readout of D4 is affected by both the CROT infidelity and intrinsic spin relaxation. We are unsure of the reason for this unique spin relaxation effect. One possible explanation could be that the valley splitting of the dot containing D4 is nearly degenerate with the Zeeman splitting, as spin relaxation would be enhanced. Although T_1 times were not measured in this device, we would expect them to be on the order of hundreds of milliseconds based on measurements in similar devices. This potential issue may be bypassed by changing the magnetic field to lift the degeneracy.

The fitted parameters A_k and B_k are related to the QND fidelities by the following relation[60]:

$$P_{1,k}(t_b) = (1 - F_{0,k}^{QND})(1 - P_{1,0}(t_b)) + F_{1,k}^{QND} P_{1,0}(t_b), \quad (5)$$

which translates to:

$$F_{0,k}^{QND} = 1 - B_k + \frac{B_0}{A_0} A_k, \quad (6)$$

$$F_{1,k}^{QND} = B_k + \frac{1 - B_0}{A_0} A_k. \quad (7)$$

Figure 2c shows the extracted QND fidelities $F_{0,k}^{QND}$ and $F_{1,k}^{QND}$, along with the average fidelity $F_{avg,k}^{QND} = (F_{0,k}^{QND} + F_{1,k}^{QND})/2$. For one QND repetition, the $F_{avg,1}^{QND}$ for D1–D4 are 96.7(1.8)%, 99.2(1.7)%, 99.1(1.3)% and 96.1(1.4)%, respectively.

Universal spin control

All primitive qubit operations can be derived from the Heisenberg Hamiltonian describing the sparse spin array. It can be expressed in terms of the Loss–DiVincenzo qubit operators as:

$$H = \sum_{ij} hJ_{ij} \left(\frac{\boldsymbol{\sigma}_i \cdot \boldsymbol{\sigma}_j}{4} - \frac{1}{4} \right) - \sum_i \frac{1}{2} g \mu_B \mathbf{B}_i \cdot \boldsymbol{\sigma}_i, \quad (8)$$

where $\boldsymbol{\sigma}_i = (X, Y, Z)^T$ is the vector of Pauli matrices acting on qubit i, $\mathbf{B}_i$ is the magnetic-field vector at the location of qubit i, h is the Planck constant, $g \approx 2$ is the electron spin g-factor in silicon, and μ_B is the Bohr magneton. J_{ij} gives the magnitude of the exchange interaction between spins. It is controllable via baseband pulses on the electrostatic gates and is effectively zero for non-adjacent spins.

When $J = 0$, single-qubit control is achieved via EDSR where an oscillating electric field $E_{ac}(t)\cos(2\pi f_{MW} t + \phi)$ with time-varying amplitude $E_{ac}(t)$, frequency f_{MW} and phase ϕ couples to the spin via a transverse gradient b_t originating from the micromagnet stray field. The single spin therefore experiences an effective magnetic field $\mathbf{B}(t) = (hf_R \cos(2\pi f_{MW} t + \phi), 0, hf_L)^T / g\mu_B$ where f_L is the Larmor frequency set by the total magnetic field at the qubit location and $f_R(t) = g\mu_B b_t e E_{ac}(t) a_0^2 / 2hE_{orb}$ is the on-resonance Rabi frequency, e is the electron charge, a_0 is the Fock–Darwin length scale of the quantum dot and E_{orb} is the orbital energy scale of the quantum dot.

In the rotating frame, the single-qubit Hamiltonian after application of the rotating wave approximation is:

$$H_{EDSR} = \frac{h(f_{MW} - f_L)}{2} Z + \frac{hf_R(t)}{2} (\cos\phi X - \sin\phi Y), \quad (9)$$

When driven on-resonance such that $f_{MW} = f_L$, the single-qubit unitary evolution is given by

$$U_{1Q} = \exp(-i2\pi f_R(t) t (\cos\phi, -\sin\phi, 0)^T \cdot \boldsymbol{\sigma}/2), \quad (10)$$

which is a rotation $R_{\hat{n}}(\theta)$ about an axis $\hat{n} = (\cos\phi, -\sin\phi, 0)^T$ by an angle $\theta = 2\pi f_R(t) t$. All single-qubit gates are derived from a single definition for an $X_{90} = \exp(-i\pi X/4)$ operation, which consists of a microwave burst of duration t_{90}. Rotations around other axes are implemented by changing the phase ϕ of the microwave burst, and arbitrary rotations $R_z(\theta)$ about the z axis of the Bloch sphere are similarly implemented by a phase update of the subsequent microwave bursts. X_{180} rotations are implemented with two concatenated X_{90} pulse definitions. The use of a unique single-gate primitive streamlines the calibration of crosstalk in the multi-qubit Hilbert space.

As all microwaves are delivered via a single antenna, we rely on spectral separation to address individual spins. To limit errors owing to off-resonant coherent driving, we use a Hamming window for the microwave pulse amplitude $E_{ac}(t)$ to limit the bandwidth of each microwave pulse to approximately $1/t_{90}$. For pulse durations of about 250 ns, the pulses therefore have a resolution of about 10 MHz. The remaining phase pickup owing to the AC Stark shift and heating effects is calibrated experimentally and accounted for in the form of virtual phase updates.

A CROT operation is used for initialization and readout by applying a resonant pulse while the exchange J_{ij} between the shuttled ancilla and a data qubit is finite. In the limit where the exchange is much smaller than the Larmor frequency difference between spins ($J_{ij} \ll |f_{L,i} - f_{L,j}|$), it is appropriate to approximate the resonance frequency of qubit i as conditional on the state of qubit j with a separation of J_{ij}. Qubit i can therefore be conditionally rotated depending on the state of qubit j via EDSR. The exchange $J_{ij}(t)$ is ramped on and off adiabatically with a Tukey pulse shape, and a microwave burst with a rectangular window is applied for a duration t_{180} required for a complete flip of qubit i. The synchronization condition $1/2t_{180} = J_{ij}/\sqrt{4n^2 - 1}$ with integer n is used to drive a 2π rotation in the subspace of the undesired transition[61]. The operation therefore performs the mapping $\{|00\rangle \to |00\rangle, |01\rangle \to |01\rangle, |10\rangle \to |11\rangle, |11\rangle \to |10\rangle\}$ which is suitable for a projective QND measurement of the control qubit in the computational basis. Although the CROT may form a universal entangling gate, we do not use the CROT as a coherent two-qubit operation and therefore do not track the single-qubit phases picked up during the operation. We also neglect the conditional phases in the CROT as they are unimportant for initialization and readout.

Coherent two-qubit operations are implemented by modulating the exchange J_{ij} adiabatically without any additional microwave burst. This ideally results in a unitary evolution $U_{2Q} = \mathrm{diag}(1, e^{-i\phi_{01}}, e^{-i\phi_{10}}, e^{-i\phi_{11}})$. U_{2Q} can be transformed into a controlled-phase gate via commuting virtual single-qubit z rotations such that $R_z(\phi_{10}) \otimes R_z(\phi_{01}) U_{2Q} = \mathrm{diag}(1, 1, 1, e^{i(\phi_{01} + \phi_{10} - \phi_{11})})$. A controlled S gate between qubits i and j is achieved when $J_{ij}(t)$ is modulated such that $\phi_{01} + \phi_{10} - \phi_{11} = \pi/2$. The duration for the gate is bounded by $t_{CS} > 1/4J_{ij,max}$, where $J_{ij,max}$ is the maximum exchange strength during the operation, and is necessarily longer to maintain adiabaticity.

The CS gate is used as the two-qubit entangling primitive as illustrated in Fig. 4a where the single-qubit z rotations are obviated by the refocusing pulses. The multi-qubit DCZ operation can be expressed in terms of controlled-phase gates CZ_{00}^i acting on the ancilla qubit and data qubit i, where $CZ_{xy}|m, n\rangle = (-1)^{\delta(x,m)\delta(y,n)}|m, n\rangle$. The circuit of Fig. 4a implements the unitary $X_{180}^{\otimes(w+1)} \Pi_{i=1}^{w} CZ_{00}^i$ acting on the ancilla qubit and w data qubits. With a universal single-qubit gate set, this operation is sufficient to apply any Pauli operation on the data qubits, conditional on the state of the ancilla qubit.

Gate calibration protocols

Periodic calibration of the five-qubit processor is necessary to compensate for slow drifts in the solid-state environment to maintain the gate fidelities required for the results presented in this work. We use a semi-automated calibration procedure that efficiently updates the control parameters for resonant gates (Supplementary Fig. 8), crosstalk compensation (Supplementary Fig. 9) and adiabatic two-qubit gates (Supplementary Fig. 10). The following protocols may be carried out once all bus stops can be populated, the ancilla can be shuttled with reasonable fidelity (specifically, the visibility of QND measurement of the data qubits will be bounded by how well spin polarization is preserved during shuttling), and all four exchange interactions are tunable over a workable range (for example, 100 kHz < J < 10 MHz).

Single-qubit gate and CROT calibration. Each resonant gate calibration begins with a coarse calibration followed by a finer one. We coarsely calibrate the Larmor frequency of the ancilla qubit A1 using microwave spectroscopy. The dip in the measured odd-state return

probability is isolated and the resonance frequency is estimated via a quadratic fit. We then drive A1 with a microwave burst shaped by Hamming window of varying duration and we fit the Rabi oscillations to extract the current Rabi frequency f_R^{fit}. As we aim for $f_R^{targ} = 1$ MHz, or $t_{90} = 250$ ns, we rescale the driving amplitude by f_R^{targ}/f_R^{fit}.

A finer calibration is then performed using a Ramsey experiment, with the rotating frame virtually detuned by 1 MHz from the coarsely calibrated Larmor frequency. Fitting the resulting Ramsey oscillations yields a frequency correction. Finally, we fine-tune the 250-ns microwave burst amplitudes. The procedure applies multiple 2π qubit rotations (typically 4), each decomposed into 4 repeated X_{90} gates, to amplify any systematic over-rotation. The sequence is terminated with either an X_{90} or a X_{-90} gate to prepare the qubit in a superposition state. By sweeping the pulse amplitude, we select the value that yields a 50% odd-parity measurement probability for both final states (corresponding to $\langle Z \rangle = 0$). The last two calibration steps are often iterated until they converge.

The CROT is calibrated using a four-step procedure, beginning with a coarse frequency estimation obtained by fitting a double-Gaussian function to an exchange spectroscopy trace acquired with the relevant data qubit in a mixed state and the exchange activated. This is possible before resonant control of the data qubits has been calibrated. For all CROTs, the higher-frequency branch is selected to drive the ancilla conditional on the data qubits occupying the $|\uparrow\rangle \equiv |1\rangle$ state. The Rabi frequency of the CROTs is used to calibrate the driving amplitude required to meet the synchronization condition.

The coarse CROT calibrations are sufficient to initialize the data qubits using QND measurement and post-selection of the desired CROT outcome, and resonant control of D1–D4 may then be calibrated analogously to A1. A finer CROT calibration is then performed by initializing the data qubits to the $|1\rangle$ state. The same calibrations are repeated, yielding more accurate estimates of both the conditional resonance frequency and the required drive amplitude owing to the improved trace visibility.

A finer calibration of the CROTs, along with resonant control of the data qubits, allows for higher visibility of the data qubits by using the full QND measurement framework presented in Fig. 3. Consequently, resonant control of the data qubits can be calibrated more precisely, and the process can be iterated until satisfactory convergence of the parameters has been achieved.

Single-qubit phase correction. As all resonant control signals are applied to the same screening gate, operating the device as a five-qubit processor requires mitigating crosstalk effects when driving different qubits that may arise owing to a combination of the AC Stark effect, device heating and induced shifts in the stray magnetic-field gradient. As the addressability gradient and pulse-shaping limit off-resonant rotations given by equation (10), this crosstalk predominantly manifests as phase pickup, which can be compensated for by virtual $R_z(\phi)$ gates.

To characterize these phases and determine the corresponding per-gate phase corrections, we perform a series of Hahn-echo-like experiments as shown in Supplementary Fig. 9a in which the target qubit remains idle while repeated sequences of X_{90} and X_{-90} gates are applied to each of the other qubits. We limit the number of applied gates to a maximum of $N = 4$ to remain in the linear regime, allowing us to extract the per-gate accumulated phase via a linear fit.

These induced phases can be compared with the predicted AC Stark shifts, showing partial qualitative agreement. However, the presence of self-induced phase accumulation (non-zero diagonal elements) as well as magnitude and sign discrepancies with the experimental data indicate that other effects, such as heating, have a significant role.

Adiabatic CS calibration. We calibrate coherent two-qubit interactions between the ancilla qubit and data qubits using an approach similar to ref. 21. The dynamic range of the exchange interaction is probed to find a suitable empirical relation $J_i(v\mathrm{BB}i)$ for all four bus stops. The charge-symmetry point is also identified via a fingerprint scan as an approximately linear function of the barrier voltage such that $v\epsilon_i \propto v\mathrm{BB}i$. This allows for pulse-shaping of the exchange strength $J_i(t)$ to maximize the adiabaticity of the interaction while remaining robust to charge noise[62,63].

Each effective CS operation is actuated by a series of baseband pulse segments as exemplified in Supplementary Fig. 10a. The first segment is a fast detuning ramp to the symmetry point. The second segment is a linear ramp to a subthreshold exchange magnitude (for example, $J < 1$ MHz). The central segment is a Hamming-shaped exchange modulation characterized by a pulse duration and magnitude $v\mathrm{BB}i^{\mathrm{ON}}$, which are selected to balance speed and adiabaticity. The remaining two segments are time-reversed copies of the first two to uncouple the qubits.

The pulse sequence in Supplementary Fig. 10b is used to fine-tune the amplitude $v\mathrm{BB}i^{\mathrm{ON}}$ in a DCZ sequence such that the total conditional phase picked up by A1 can be identified for both computational-basis state preparations of the relevant data qubit Di. This is exemplified for the two-qubit interaction at bus stop 2 in Supplementary Fig. 10c,d. A total conditional phase difference of π is selected to ensure each individual CS operation accrues π/2 radians of conditional phase.

Single-qubit characterization

The dephasing times measured using CPMG decoupling can be used to gain insight into the noise spectrum influencing each qubit (Fig. 3e). We assume a monotonic noise spectrum $S(\omega) = A/\omega^{\alpha}$ acting on each qubit such that $T_2 = T_2^0 N_\pi^{\alpha/(1+\alpha)}$ and $T_2^0 = (2/A)^{1/(\alpha+1)}\pi^{\alpha/(1+\alpha)}$ and observe a good fit in all cases[64]. T_2^* measurements use a total integration time of about 25 minutes.

Single-qubit gate fidelities are evaluated using randomized benchmarking. We use the primitive gate set $\{I, X_{90}, Y_{90}\}$ of only positive rotations such that a Clifford gate is composed of 3.125 primitive gates on average[65]. A X_{90} gate duration of 250 ns is used for each primitive gate. The single-qubit Clifford gate fidelities are 98.98(3)%, 99.930(5)%, 99.90(1)%, 99.87(1)% and 99.924(6)% for A1, D1, D2, D3 and D4, respectively. Individual single-qubit gate fidelities in the single-qubit subspace are all well above 99.9% for the data qubits, and slightly lower for the ancilla qubit (Fig. 3g). We speculate that the lower ancilla fidelity may be due to its relative proximity to the reservoir, which is tunnel-coupled to R1 for the purposes of spin reloading. In the experiment, pairs of single-qubit operations were performed simultaneously when applicable. When all four bus stops were used, D1/D2 and D3/D4 were parallelized. When three bus stops were used, the ancilla would be driven in parallel with one of the bus stops.

To benchmark the shuttling performance, we use interleaved randomized benchmarking. The resonant control of qubit A1 when localized below P2 is used as the reference set. The interleaved operation consists of shuttling from below P2 to a location in the shuttling bus adjacent to a bus stop, idling for 50 ns, and shuttling back. A calibrated phase correction is added to make the targeted interleaved operation an identity gate. The measured fidelities do not change substantially with a small increase in the idling time; therefore, we believe that most of the infidelity originates during shuttling itself. A significant fraction of the shuttling error originates during loading and unloading the conveyor, when A1 moves from below gate P2 to below gate C0, as seen from the 97.9% round-trip shuttling fidelity to bus stop 1. This transition is induced with a linear voltage ramp of 40 ns duration and may be possible to optimize further. Only a 0.2% decrease in fidelity is observed when shuttling the remaining round-trip distance to bus stop 4. One round-trip of the ancilla from below P2 to bus stop 4, in the absence of any 2-qubit interactions, takes place in 730 ns. Considering that the T_2^H of A1 is 47.6 μs with a decay exponent of 1.7 when localized below P2, we estimate that dephasing alone could contribute about 0.1% to the

infidelity. Increasing the speed of the travelling-wave potential would be the most effective way to increase this limit (in ref. 5, conveyor speeds were up to 25 times faster).

To implement the refocusing pulse during the DCZ operation, we shuttle the ancilla back to below P2 as opposed to keeping the qubit adjacent to bus stop 4. This redundant shuttling adds 730 ns of shuttling and incurs an additional error of about 2.7%, much of which is picked up between P2 and C0. We include the redundant operation for three reasons. First, the Zeeman energy difference between the ancilla localized adjacent to bus stop 4 and data qubit D4 is relatively small, and therefore vulnerable to coherent errors if not calibrated at the synchronization condition. Second, we find that single-qubit EDSR driving within the conveyor potential does not always exhibit high fidelity, so optimizing high-fidelity control would require additional baseband pulses. Third, activating the conveyor shifts all qubit frequencies. For experimental ease of avoiding added calibration overhead, we opt to perform all single-qubit operations at the same voltage setpoint when the conveyor is deactivated.

We did not observe any clear evidence of valley excitations limiting the quality of the multi-qubit demonstration. For example, such excitations could result in observing two closely spaced resonance frequencies as spins occupying different valley–orbit states will have slightly different g-factors[66,67]. This effect was observed during the initial tuning of the exchange coupling of bus stop 1, but subsequent changes to the loading pulse sequence removed the effect.

It is understood that fluctuations in the valley splitting across a silicon shuttling channel can limit the quality of spin shuttling[42,57,68]. It is possible that we would be able to resolve such effects by further optimizing the shuttling channel and rigorously characterizing the valley splitting across the array.

Two-qubit characterization

We use character randomized benchmarking (CRB) to evaluate the performance of the two-qubit interaction between the shuttled ancilla and the four data qubits[69]. CRB allows us to use simultaneous single-qubit Clifford gates as the reference gate set as opposed to general two-qubit Clifford operations, which require many native CZ gates to compile.

As seen in Fig. 4a, the entangling interaction used to implement parity checks is a composite operation consisting of coherent shuttling, two-qubit interactions and single-qubit gates for refocusing phase pickup. Furthermore, we take advantage of the fact that the native controlled-phase interactions commute. We therefore benchmark each individual DCZ interaction to estimate the isolated error contribution from each component of this composite interaction.

We perform two different rounds of interleaved CRB for each two-qubit interaction. First, only the decoupled shuttling sequence is interleaved with no exchange activated. As this operation should be logically equivalent to $X_{180} \otimes X_{180}$, this provides an estimate of the error rate associated with qubit shuttling and the refocusing gates in the two-qubit Hilbert space of the ancilla and the relevant data qubit. Then, we interleave a maximally entangling DCZ interaction such that the interleaved gate is $X_{180} \otimes X_{180}\mathrm{diag}(1, 1, 1, -1)$. The inverting Clifford gate is implemented using a directly calibrated CZ gate consisting of a single two-qubit interaction and explicitly calibrated phase corrections on both participating qubits. This allows us to use a verified lookup table to implement the inverting Clifford. We also verify with interleaved CRB that this direct CZ has comparable fidelity to the DCZ, in the range of 90–95%. The decoupled version of the gate is conceptually closer to the compound interaction presented in Fig. 4a used to implement parity checks in this work. Supplementary Table 1 summarizes all of the fidelities extracted from CRB.

On the basis of the interleaved CRB results, we coarsely estimate an error rate $r_{\mathrm{Dsh}} = 1 - F_{\mathrm{Dsh}}$ associated with the decoupled shuttling sequence, and an error rate $r_{\mathrm{DCZ}} = 1 - F_{\mathrm{DCZ}}$ associated with the full entangling two-qubit gate, including the evolution under exchange, shuttling and the refocusing pulses. By assuming that these errors are stochastic, independent and small, we approximate the error rate associated with the pure exchange component of the interaction as $r_J = r_{\mathrm{DCZ}} - r_{\mathrm{Dsh}}$. The fidelity of the two-qubit exchange interaction as reported in Fig. 3g is then given as $F_{2Q} = 1 - r_J$.

To verify these fidelity estimates, we can compare them with the quality factors obtained from observing exchange oscillations in a decoupled sequence. Extended Data Fig. 3 summarizes the effect of increasing exchange on qubit coherence, and the extracted quality factors Q for 1 MHz < J < 10 MHz fall in the range of 10 to 30. The quality factor puts a bound on the achievable fidelity limited by incoherent noise as $F_{2Q} < 1 - 1/Q$, as quasi-static noise is removed by the refocusing pulses when exchange oscillations are measured. This limit is consistent with the benchmarked fidelities of 90–95% that are obtained from interleaved CRB.

The two-qubit gate fidelities we characterize are well below state-of-the-art devices, where error rates lower than 1% have been achieved, and we can highlight a few important differences between many of these demonstrations and the present work. First, the barrier gates here modulate the exchange strength more strongly than in many previous studies[35,46], in some cases with double the lever arm as measured in dec V^{-1}, thereby coupling gate voltage fluctuations more strongly to the qubits. Second, we use relatively modest attenuation on the barrier control lines. Although useful for prototyping, lower attenuation allows more noise to propagate from higher-temperature stages to the device. Early demonstrations of high-fidelity exchange-based two-qubit gates exhibited quality factors in the range of 50–100 (ref. 35). Recently, this metric has improved to about 1,000 through methodical engineering of the fabrication process and heterostructure[50]. The composition of the gate stack can also be further improved to optimize the noise environment for the spins[70]. We therefore predict modest device and set-up modifications to bring the two-qubit gate fidelities much closer to the state of the art, and we do not anticipate these changes to compromise other aspects of the device operation, such as spin shuttling.

Error budget for logical-state preparation

The combination of qubit characteristics (Fig. 3e), operation benchmarks (Fig. 3g) and circuit compilation can be used to construct an error budget for the five-qubit processor. We choose the relevant example of preparing the logical $|0\rangle_{\mathrm{L}} = \frac{1}{\sqrt{2}}(|0000\rangle + |1111\rangle)$ state for a $[\![4, 1, 2]\!]$ surface code as it utilizes all operations. As shown in Fig. 4f and Extended Data Fig. 8, the sparse processor produces such a state with a fidelity of about 63%. The quantum circuit producing this state, shown in Fig. 4c, utilizes all four 2-qubit interactions between the ancilla and each data qubit, 2 round-trips of shuttling the ancilla qubit, 16 decomposed single-qubit gates, and initialization and measurement of the ancilla qubit. The final single-qubit gates on each data qubit are compiled into the quantum-state tomography (QST) projections, and measurement errors associated with the data qubits are not considered as they are corrected during state reconstruction. Extended Data Fig. 10a summarizes the error sources from all operations and idling taking place in the circuit.

Extended Data Fig. 10b represents the relative proportions of errors originating from single-qubit gates and dynamical decoupling, two-qubit interactions, shuttling, idling and measurement. For a first-order estimate, we assume that all errors p_i are depolarizing such that the circuit produces a state $\rho = (1 - P)|\psi_{\mathrm{GHZ}}\rangle\langle\psi_{\mathrm{GHZ}}| + P\frac{I}{16}$ where $(1 - P) = \Pi_i(1 - p_i)$ and I is the identity matrix, yielding a logical-state fidelity of about 67%. A remaining error of about 6% between the estimated and measured state fidelities is unaccounted for, but this can reasonably be expected to originate from sources that are not captured by the individual benchmarking protocols. These sources include crosstalk beyond the benchmarked Hilbert spaces and slow device drift. We believe that the latter is particularly relevant for longer experiments.

For example, collection of all tomographic projections of the five-qubit GHZ state shown in Extended Data Fig. 9 took 2 hours, during which all control parameters are held constant, and the measured state fidelity of 53% is substantially lower than the 63% four-qubit logical-state initialization fidelity despite the circuits being very similar. Here the solution is to interleave fine calibrations more densely through such experiments, and we would expect observing a five-qubit GHZ-state fidelity above 60% to be possible with the present level of performance.

We can use the same strategy to estimate the parity-check accuracy based on the individual fidelities. Unlike for logical-state preparation, when the parity checks are benchmarked all data qubits are spin eigenstates during the DCZ sequence, and therefore robust to dephasing. By excluding data qubit idling errors from the calculation, we estimate weight-four Z-type and X-type parity checks to have accuracies of about 70.5% and 70.0%, respectively, which compares reasonably well with the extracted accuracies of 72% and 67%. The X-type check is expected to have lower accuracy primarily owing to the additional dephasing that is incurred during preparation of the X-type basis states. During the preparation of these superposition states, the data qubits are more sensitive to crosstalk errors that are not captured by our benchmarked fidelities.

Although the presented analysis is coarse, the overall performance of the device is well captured by the individual benchmarks. Crucially, we believe that the most performance-limiting error sources are apparent. The two-qubit interaction fidelities represent the majority of the error present in the device, and the incoherent noise limiting them must be addressed. Fortunately, previous demonstrations of two-qubit gate fidelities well above 99% in similar device architectures provide evidence that this is possible. The next-largest error sources are idling and shuttling. These processes are dominated by dephasing, meaning that increasing the speed of shuttling should suppress both sources of error.

Quantum-state tomography

QST for an n-qubit state is performed by measuring the expectation value of all 4^n Pauli observables A_k using the individual computational-basis readout available for all qubits in the system. We bin the results into a probability vector P_{meas} of length 2^n.

As the data qubits are read out indirectly and have finite visibility, readout errors are corrected by transforming P_{meas} according to the visibility of Rabi oscillations extracted using the same initialization and readout sequence[39]. We use a single round of QND measurement such that the data qubits have readout visibilities of about 80% to 85% (Extended Data Fig. 2). If qubit i has visibility limits $[V_{i,\min}, V_{i,\max}]$, the corrected probability vector P_{corr} is given by:

$$P_{\text{corr}} = S_i^{-1} P_{\text{meas}} = \begin{pmatrix} 1 - V_{i,\min} & 1 - V_{i,\max} \\ V_{i,\min} & V_{i,\max} \end{pmatrix}^{-1} P_{\text{meas}} \tag{11}$$

For multi-qubit corrections, the tensor product of the correction matrices S_i for all participating qubits is used. The pseudo-inverse is used to calculate the inverse numerically to improve stability, the elements of P_{corr} are clipped to 1 and 0, and the vector is renormalized to maintain physicality (if applicable, these corrections are small and tend to lower the fidelity of the reconstructed state). The expectation value of the relevant operator is then calculated by weighting the entries of P_{corr} and averaging appropriately. For example, the expectation value $\langle XIY \rangle$ is extracted as $\text{Tr}((Z \otimes I \otimes Z)\text{diag}(P_{\text{corr}}))$. When reconstructing states that include the ancilla qubit, we include its (relatively small) readout correction for consistency. For reconstructing states initialized via a parity check, no ancilla measurement correction is possible as data must be binned shot by shot. These reconstructed states therefore necessarily include errors in the ancilla measurement.

The density matrix ρ_{meas} is reconstructed from all measured expectation values M_k using maximum likelihood estimation to minimize $\sum_{k=1}^{4^n} |M_k - \text{Tr}(A_k \rho_{\text{meas}})|^2$ while enforcing the Hermiticity and unit-trace properties of ρ_{meas}. The optimization is implemented using the CVXPY convex optimization package.

We use bootstrapping to estimate a statistical error on the extracted fidelity by performing the reconstruction multiple times by sampling P_{meas} from a multinomial distribution according to the measured probability and number of shots. We also uniformly sample the visibility limits used for readout correction, using the Rabi oscillation fit errors as bounds. Each state reconstruction is performed 500 times to ensure good convergence, and the mean fidelity is reported along with the $\pm 1\sigma$ standard deviation of the distribution of reconstructed state fidelities. We note that this uncertainty captures the statistical nature of the tomographic data, but it does not account for the variation arising from possible experimental drift and different circuit fidelities for different combinations of qubits. The spread of reported fidelities in Fig. 4f due to these sources therefore exceeds the interval of uncertainty for each individual data point.

Parity-check analysis

To estimate the accuracy of the parity checks as applied to eigenstates of the stabilizer, we use a similar process as for full state reconstruction with QST. After performing the weight-w check and measuring the ancilla qubit, all data qubits are measured in the eigenbasis of the stabilizer. This yields a probability vector P_{meas} of length 2^{w+1}. Readout errors on the data qubits are corrected as in QST to acquire a corrected vector P_{corr}. The ancilla qubit visibility is not corrected. We report the element of P_{corr} that corresponds to the intended data qubit-state preparation and the correct ancilla measurement outcome. This yields a lower estimate for the parity-check accuracy (Fig. 4e) than an average of the correct ancilla outcome probabilities for all state preparations (Fig. 4d), as it also accounts for instances where the parity-check operation corrupted the data qubit state, even if the ancilla measurement gives the correct outcome.

We further assess the performance of a repetitive parity-check circuit using bus stops 1 and 2. We initialize these bus stops in one of the states $|00\rangle, |01\rangle, |10\rangle$ or $|11\rangle$ and perform 35 rounds of ZZ parity checks (Extended Data Fig. 5a). The measured parity is +1 (−1) if the first single-shot result returns a value of +1 (−1). Subsequent shots are compared with the previous shot to detect a flip or no flip in the parity; a trace of the single-shot values and the corresponding parity is shown in Extended Data Fig. 5b. We took 2,000 single shots to obtain the average parity value for each parity-check cycle. The decay of the average parity is fitted with the model $\text{Ar}^N + C$, where N is the number of rounds, to determine the parity retention rate r. The resulting retention rates are $r_{00} = 92.64(5)\%$, $r_{01} = 93.52(5)\%$, $r_{10} = 92.70(5)\%$ and $r_{11} = 94.89(4)\%$.

Data availability

Data and analysis scripts supporting this work are available via Zenodo at https://doi.org/10.5281/zenodo.17368102 (ref. 71). Source data are provided with this paper.

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Acknowledgements We acknowledge discussions with L. Schreiber, Y. Matsumoto, M. De Smet, S. van der Meer, S. Ivlev, I. Fernández de Fuentes, E. Raymenants, M. Rimbach-Russ and X. Xue. We thank Y. Matsumoto and M. Rimbach-Russ for feedback on the paper. We are grateful to O. Benningshof and E. van der Wiel for providing cryogenic support and for designing the cold finger; and Y. van der Linden for designing and testing the PCB and Qblox for support in using the control electronics. We thank the Groove Quantum team for many instances of collaborative set-up debugging as well as the remainder of the spin-qubit groups at QuTech for input and discussions.

Author contributions B.U., N.M., Y.-H.W. and S.R.K.-F. performed the experiments. B.U. and N.M. built the experimental set-up. B.U. designed the device and L.T. fabricated the device with substantial input from D.D.E. S.L.d.S. developed the software used in the experiments. G.S. provided the ^{28}Si/SiGe heterostructure. B.U. and L.M.K.V. conceived of the project. E.G. and L.M.K.V. supervised the project. B.U., N.M., Y.-H.W. and L.M.K.V wrote the paper with input from all authors.

Funding This publication is part of the 'Quantum Inspire - the Dutch Quantum Computer in the Cloud' project (with project number [NWA.1292.19.194]) of the NWA research programme 'Research on Routes by Consortia (ORC)', which is funded by the Netherlands Organization for Scientific Research (NWO) (B.U. and Y.-H.W.). This research was supported by the Horizon Europe programme of the European Union under grant agreement number 101174557 (QLSI2) (N.M.). Research was sponsored by the Army Research Office and was accomplished under award number W911NF-23-1-0110 (S.R.K.-F. and S.L.d.S.). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office or the US Government. The US Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein. This research was sponsored in part by The Netherlands Ministry of Defense under award number QuBits R23/009 (D.D.E. and G.S.). The views, conclusions and recommendations contained in this document are those of the authors and are not necessarily endorsed, nor should they be interpreted as representing the official policies, either expressed or implied, of The Netherlands Ministry of Defense. The Netherlands Ministry of Defense is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein. L.T., E.G. and L.M.K.V. declare no relevant funding.

Competing interests The authors declare no competing interests.

Additional information
Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41586-026-10766-3.

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Peer review information *Nature* thanks Joseph Kerckhoff, John Nichol and the other, anonymous, reviewer(s) for their contribution to the peer review of this work. Peer reviewer reports are available.

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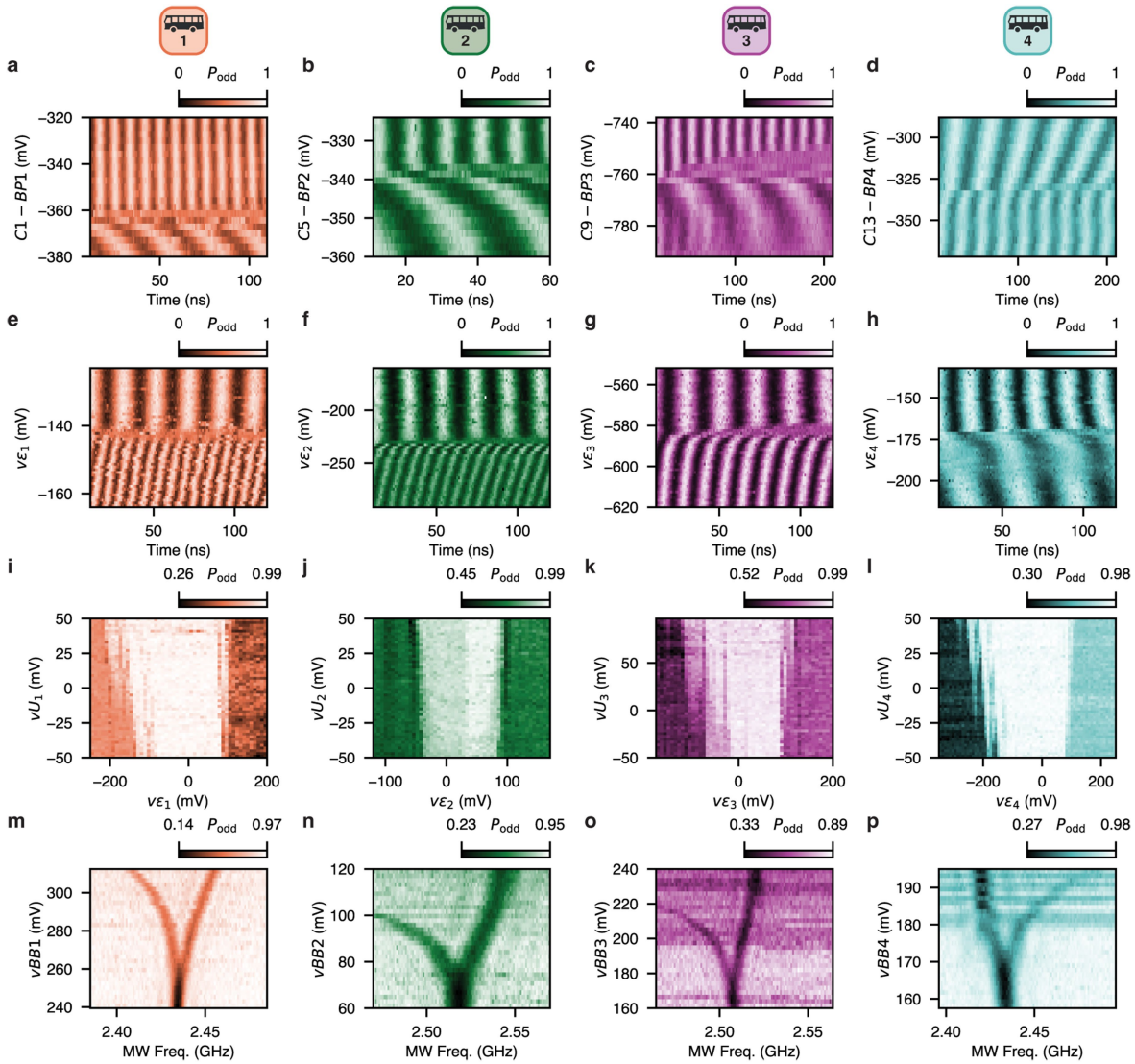
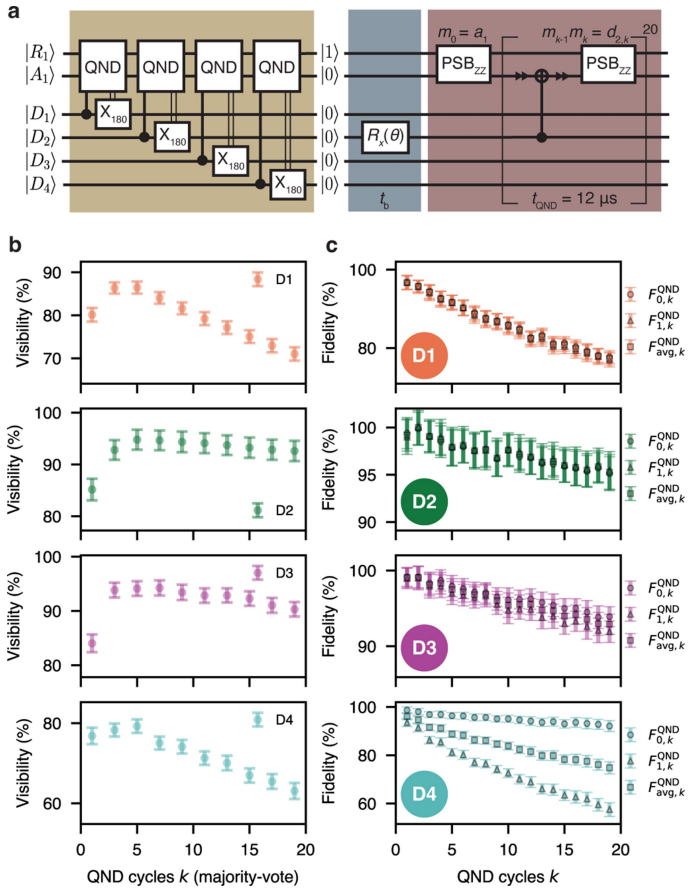
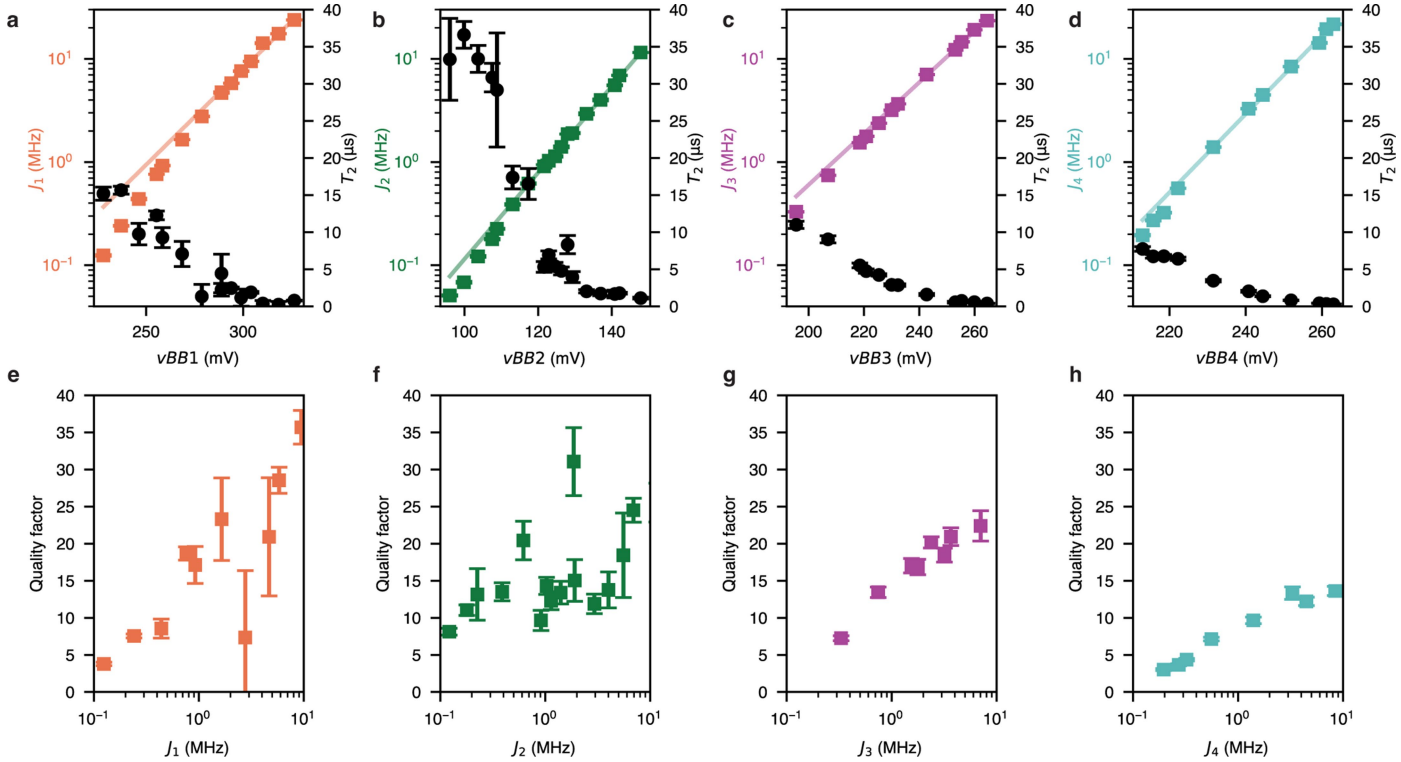


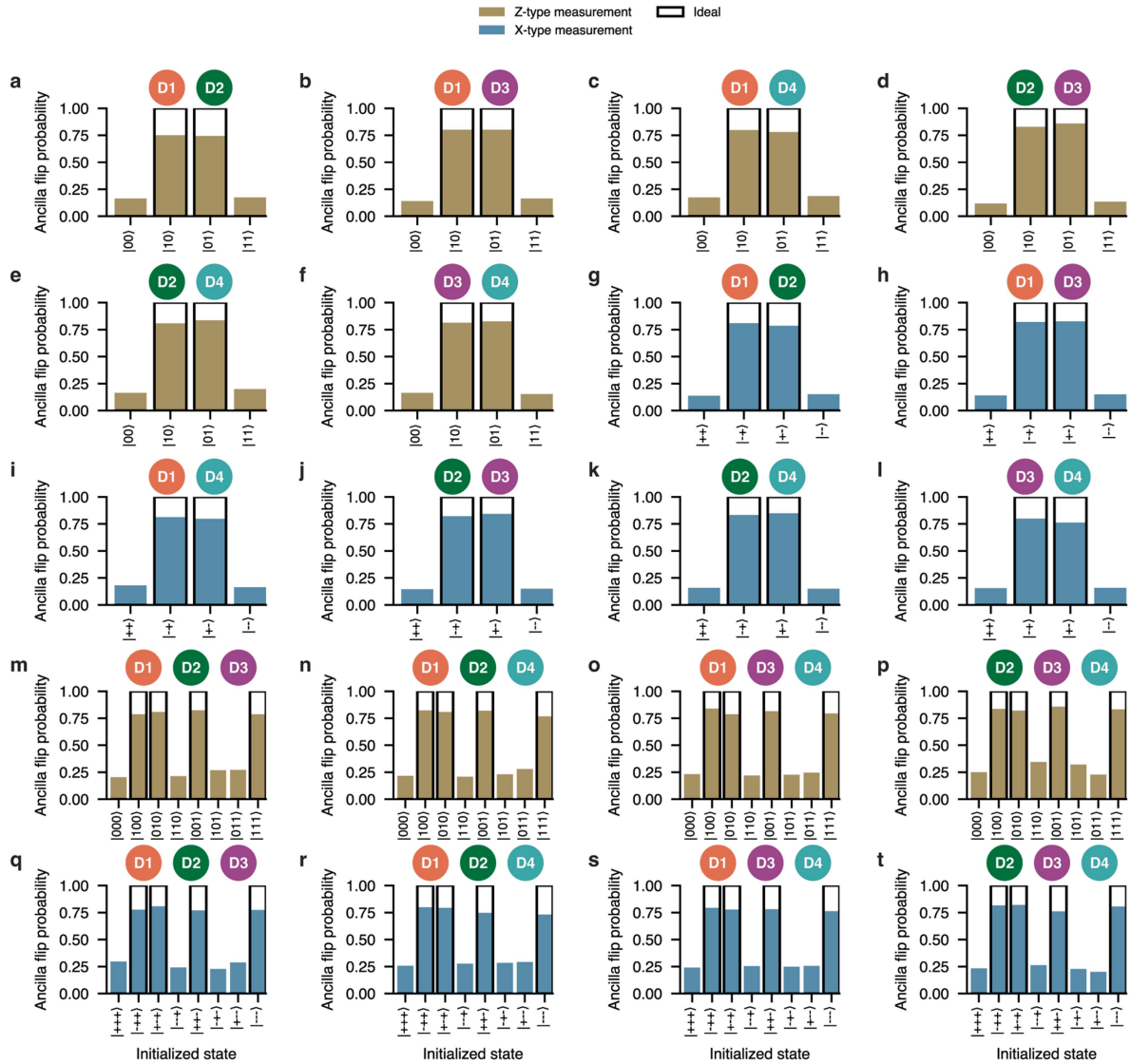
Extended Data Fig. 1 | Remote tuning of the four bus stops. a–d First signatures of remote single-electron charge transitions measured within the four bus stops when exploring the empty array by shuttling a spin in superposition before gate virtualization or tunnel coupling tuning had taken place. **e–h** Remote single-electron charge transitions measured within the four bus stops after virtualizing control of each effective double-dot system and increasing the tunnel coupling. A fixed ramp time of 40 ns was used, therefore the tunneled spin picks up a phase that depends on the magnitude of the detuning pulse. The Larmor precession frequency in each dot is effectively constant. **i–l** Remote two-electron charge stability diagrams measured for all four bus stops when all other bus stops are populated with a single-electron. Multiple features parallel to the charge transition line likely indicate tunneling to excited orbital states. **m–p** Exchange splitting measured with EDSR for all four bus stops when all other bus stops are populated with a single electron. The four bus stops are color-coded for clarity, but the measured signal is the probability of an odd-parity PSB outcome P_{odd} in all cases.



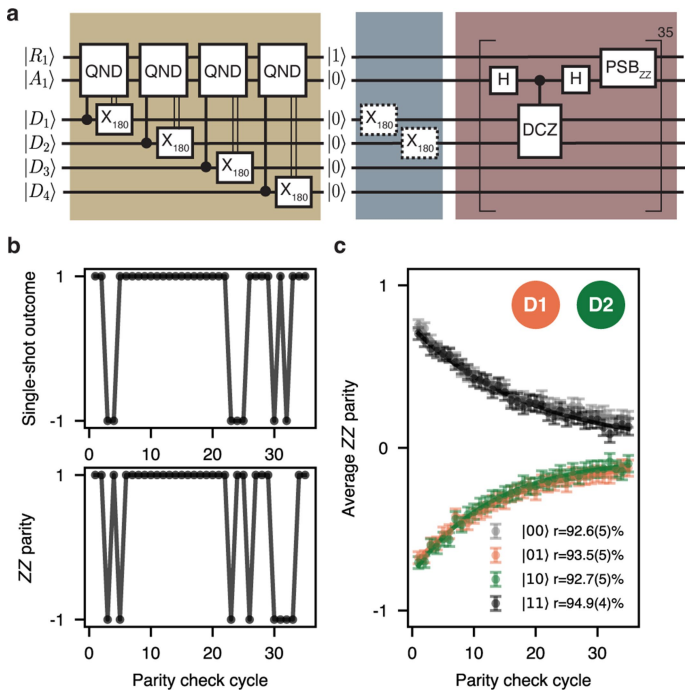
Extended Data Fig. 2 | Repeated QND measurements. a Example of a repeated QND measurement circuit for D2. After the loading and initialization of all qubits, a resonant microwave burst is applied to one of the data qubits for a time t_b. This is followed by 20 successive QND measurement cycles on the data qubit. The single-shot computational-basis measurement for the k-th cycle is given by $d_{i,k} = m_{k-1}m_k$. Each QND measurement cycle requires about 12 µs. **b** Visibility of data qubit Rabi oscillations as a function of the number of successive QND measurement cycles used to conduct a majority-vote. **c** QND fidelities calculated as a function of the number of successive QND cycles.



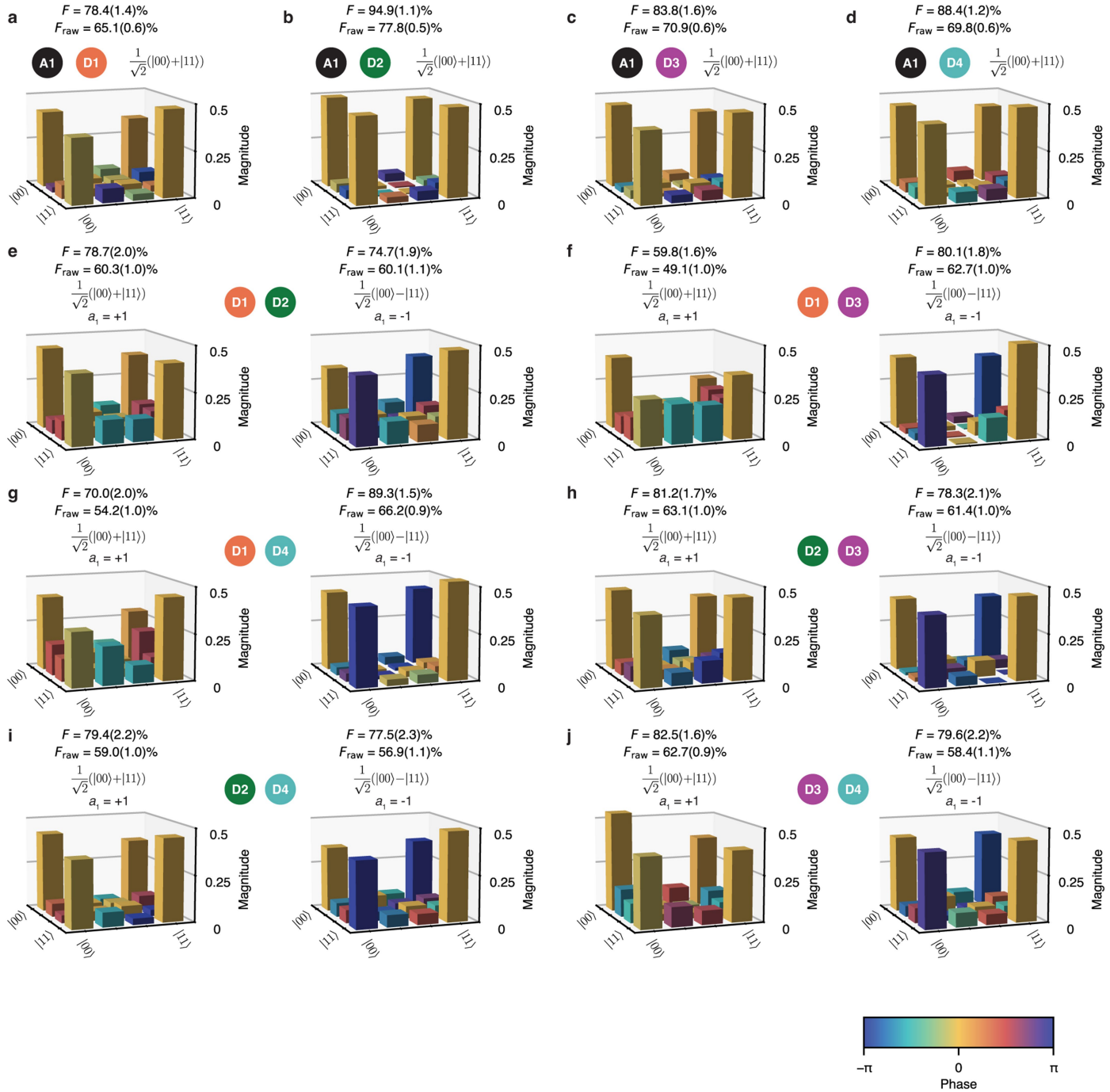
Extended Data Fig. 3 | Coherence of the exchange interactions. a–**d** Exchange strength and dephasing time of A1 as a function of barrier voltage for two-qubit interactions at the four bus stops respectively. **e**–**h** Quality factors for the two-qubit interactions at the four bus stops, calculated as $Q = 2JT_2$, estimating the number of maximally entangling two-qubit interactions that can take place within the characteristic decay time.



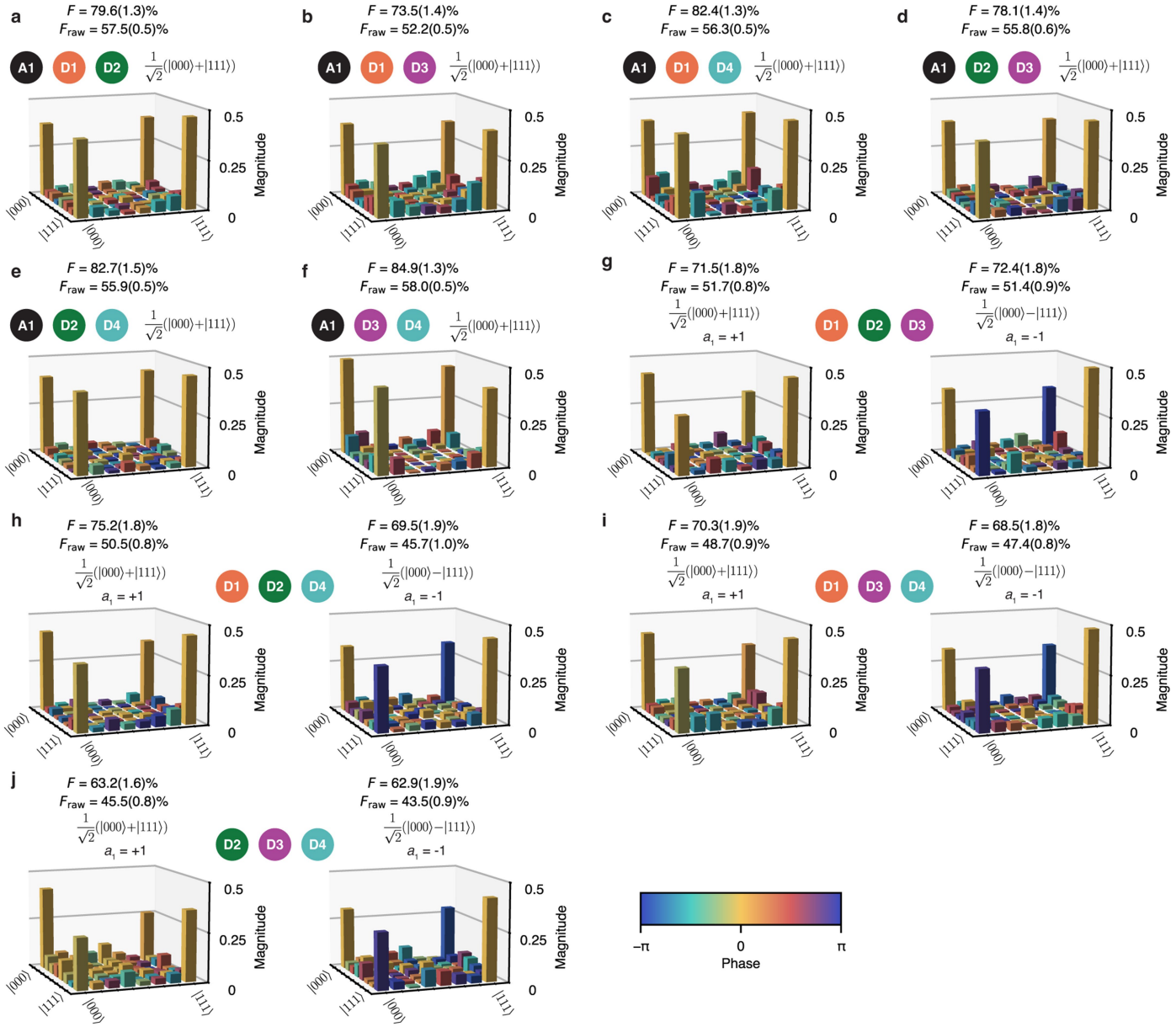
Extended Data Fig. 4 | Weight-two and weight-three parity checks. **a**–**f** Weight-two *Z*-type parity checks for all combinations of data qubits. **g**–**l** Weight-two *X*-type parity checks for all combinations of data qubits. **m**–**n** Weight-three *Z*-type parity checks for all combinations of data qubits. **q**–**t** Weight-three *X*-type parity checks for all combinations of data qubits.



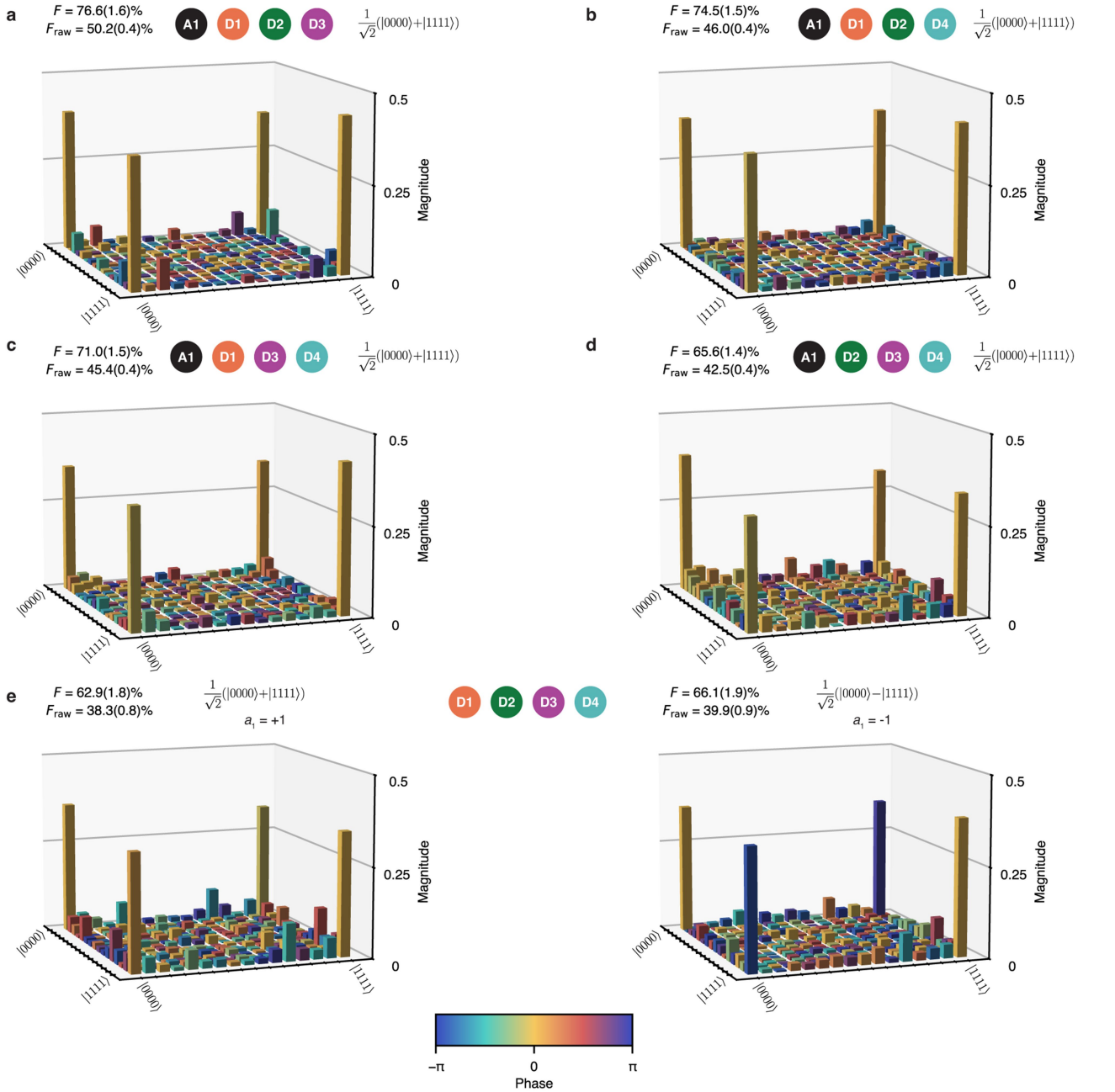
Extended Data Fig. 5 | Repeated parity checks. a Circuit for repetitive parity checks on bus stops 1 and 2. **b** Trace of the single-shot outcomes and the corresponding parity values for a single run of the circuit with the $|00\rangle$ input state for bus stops 1 and 2. **c** Average parity values for all input states $|D_2D_1\rangle$ as a function of the number of parity check cycles. The decay is fitted with $Ar^N + C$, where N is the number of rounds and r is the parity retention rate. Error bar represents the 95% confidence interval.



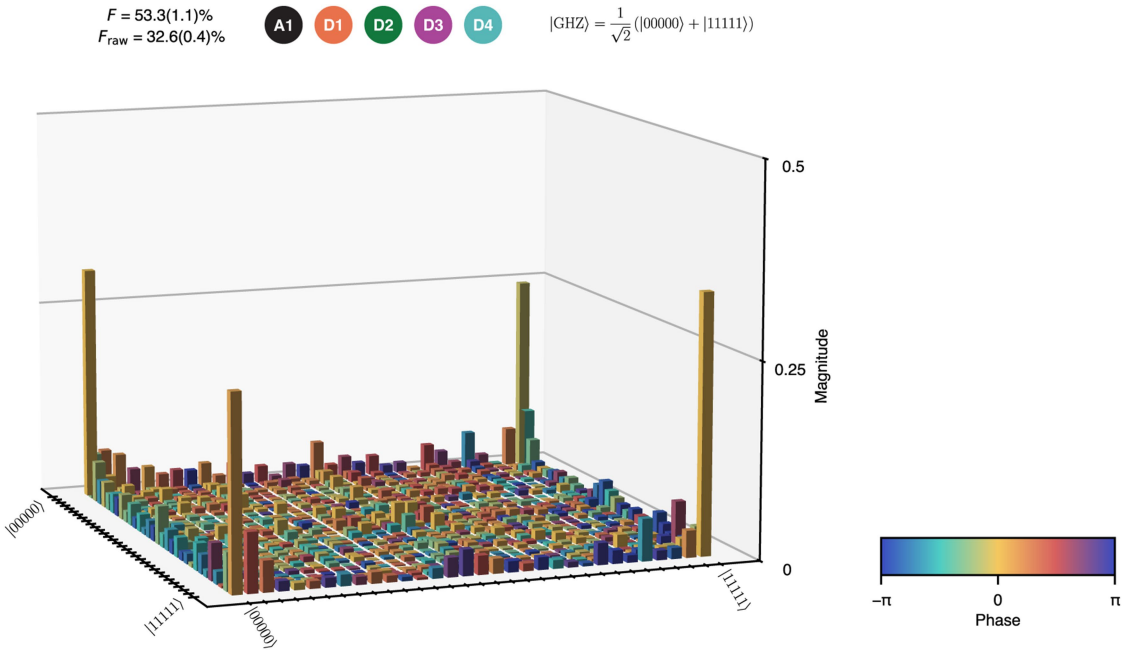
Extended Data Fig. 6 | Two-qubit GHZ state tomography. a–d Two-qubit GHZ state density matrices for all qubit combinations including the ancilla qubit A1. The states are prepared by running a circuit analogous to Fig. 4c and performing QST on all qubits at the dashed line. **e–j** Two-qubit GHZ state density matrices for the displayed data qubit combinations. For each combination, two GHZ states differing in phase are probabilistically generated depending on the outcome of the weight-two X-type parity check used to create them as displayed above the plots. The fidelity $F = \langle\psi_{GHZ}|\rho_{meas}|\psi_{GHZ}\rangle$ is calculated with respect to the target state displayed next to each plot where ρ_{meas} is the reconstructed density matrix including corrections for readout errors. $F_{raw} = \langle\psi_{GHZ}|\rho_{raw}|\psi_{GHZ}\rangle$ provides the analogous fidelity where ρ_{raw} is the reconstructed density matrix in the absence of readout corrections. Error intervals represent $\pm 1\sigma$ and are calculated by bootstrapping in all cases. Uncertainties in the readout corrections are included in the boostrapping procedure and therefore yield larger uncertainties for F than F_{raw}.



Extended Data Fig. 7 | Three-qubit GHZ state tomography. a–f Three-qubit GHZ state density matrices for all qubit combinations including the ancilla qubit A1. **g–j** Three-qubit GHZ state density matrices for the displayed data qubit combinations. For each combination, two GHZ states differing in phase are probabilistically generated depending on the outcome of the weight-three *X*-type parity check used to create them as displayed above the plots. The displayed fidelities are calculated as described by the caption of Extended Data Fig. 6.



Extended Data Fig. 8 | Four-qubit GHZ state tomography. a–**f** Four-qubit GHZ state density matrices for all qubit combinations including the ancilla qubit A1. **g**–**j** Four-qubit GHZ state density matrices for all four data qubits. The two GHZ states differ in phase and are probabilistically generated depending on the outcome of the weight-four *X*-type parity check used to create them as displayed above the plots. The displayed fidelities are calculated as described by the caption of Extended Data Fig. 6.

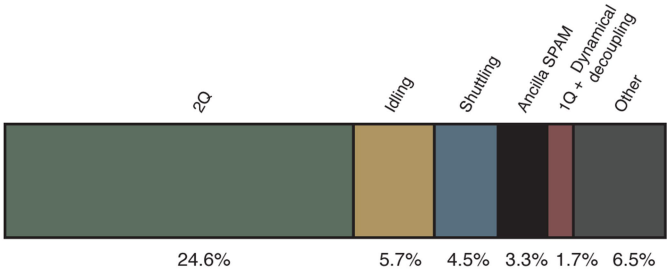


Extended Data Fig. 9 | Five-qubit GHZ state tomography. The five-qubit GHZ state density matrix supported by the ancilla qubit and all four data qubits. The displayed fidelities are calculated as described by the caption of Extended Data Fig. 6.

a

Operation	Duration	Error estimate
A1 X_{90}	250 ns	0.0033
D1 X_{90}	250 ns	0.0002
D2 X_{90}	250 ns	0.0003
D3 X_{90}	250 ns	0.0004
D4 X_{90}	250 ns	0.0002
A1 and D1 exchange	440 ns	0.076
A1 and D2 exchange	220 ns	0.051
A1 and D3 exchange	360 ns	0.099
A1 and D4 exchange	360 ns	0.046
A1 round-trip shuttle	730 ns	0.023
A1 idling (excl. shuttle)	1.5 µs	0.003
D1 idling	3.65 µs	0.010
D2 idling	3.87 µs	0.020
D3 idling	3.48 µs	0.016
D4 idling	3.48 µs	0.010
A1 measurement	10 µs	0.017

b



Extended Data Fig. 10 | Error budget for logical state preparation. a Table summarizing the operations required to initialize a surface code logical state and their associated timescales and estimated error rates. For operations with a fidelity F benchmarked with randomized benchmarking, the error rate is taken as $1-F$. The idling times t_{idle} are determined based on the nominal pulse sequence used to run the circuit shown in Fig. 4c where single-qubit gates on D1/D2 and D3/D4 are parallelized. The idling errors are estimated using $1-\exp(-(t_{\mathrm{idle}}/T_2^{\mathrm{H}})^{\alpha'})$ where T_2^{H} are the measured Hahn echo times for each qubit (47.6(1.0) µs, 43.2(1.0) µs, 32.6(8) µs, 37.8(7) µs, 65.1(1.6) µs for A1, D1, D2, D3, D4 respectively) and α' is the measured echo decay exponent (1.71(9), 1.86(11), 1.83(13), 1.74(8), 1.58(10) for A1, D1, D2, D3, D4 respectively). The A1 measurement error is commensurate with a qubit visibility of 97%. **b** Graphical representation of the error budget for initializing a $[\![4, 1, 2]\!]$ surface code logical state.