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MOSFET-BASED AND P-N DIODE BASED TEMPERATURE SENSOR IN A 4H-SIC CMOS TECHNOLOGY

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ABSTRACT

This paper presents p-n diode temperature sensors and MOSFET temperature sensors in low-voltage silicon carbide (SiC) CMOS technology. The reported temperature sensors directly make use of the existing doping layers in the CMOS process, thus enabling the monolithic integration of the SiC temperature transducer and the SiC readout electronics. The temperature sensor is characterized from 25 to 200°C. The diode-based temperature sensor has a maximum sensitivity of 3.27 mV/°C and a maximum R^2 of 99.81%. The MOSFET-based temperature sensor achieved a maximal sensitivity of 16.5 mV/°C, however, with less linearity (R^2_{max} = 99.11%). This technology shows a unique potential for implementing harsh environment smart temperature sensors.

KEYWORDS

Silicon carbide, temperature sensing, CMOS, harsh environment

INTRODUCTION

The Silicon-based integrated circuit (IC) is the greatest invention from the last century and has been widely applied in every field. By leveraging the temperature dependencies of various components in the Si technology, such as resistors [1-3], bipolar junction transistors (BJTs) [4-6], and metal-oxide-semiconductor field effect transistors (MOSFETs) [7-9], integrated temperature sensors are fabricated with excellent specifications. However, when it comes to high-temperature applications, the Si-based integrated temperature sensor is not a good choice. As summarized by a survey conducted by K. Makinwa et al. [10], the maximum operating range of a Si smart temperature sensor is 180°C. For integrated temperature sensors, the usage of active components containing the p-n junction is inevitable. However, the Si p-n junction experiences a large leakage current at a high temperature, and this causes the malfunction of the transducer and/or ICs [11].

SiC is a promising compound semiconductor for harsh environment applications thanks to its outstanding mechanical and electrical properties [11, 12]. The wide bandgap (E_g = 3.26 eV) of 4H-SiC is particularly attractive for high-temperature electronics. The SiC's bandgap is almost three times larger than that of Si and therefore gives a lower electron/hole pair generation rate at high temperatures. As a result, the leakage can be largely suppressed, and the operating temperature of SiC electronics will be much higher than Si. Not surprisingly, people have developed temperature sensors based on SiC, including pin diode [13], Schottky diode [14, 15], and p-n diode [16]. The highest temperature limit of the SiC temperature sensor was reported by Zhang et al. in [16], which is 600ºC. Nevertheless, all the temperature sensors reported so far are discrete components and show poor compatibility with planar SiC IC technology. This will lead to a two-die system, causing increased cost and complexity.

When it comes to the most representative SiC low-voltage IC technologies, e.g., HiTSiC SiC CMOS technology developed by Raytheon UK [17] and HOTSiC SiC BJT technology developed by the group of Zetterling [18], various SiC ICs have been reported and can work up to 500°C [19]. However, the performance of temperature sensing components are not investigated. In addition, these technologies are either discontinued or for internal research, which is hard to access. Recently, an emerging 4H-SiC CMOS IC technology has been developed by Fraunhofer Institute for Integrated System and Devices Technology (IISB) which is available through Europractice. With this technology, we have successfully implemented circuit blocks and an integrated UV sensing system for harsh-environment applications [20, 21].

In this paper, we have characterized the basic temperature sensing elements, i.e., p-n diodes and MOSFETs, in the IISB's SiC CMOS technology. These devices are fully compatible with SiC CMOS technology, so they can be directly integrated with proper SiC readout electronics. The measurement was performed from room temperature to 200ºC, which is beyond the typical operation temperature of Si-based temperature sensors. The result demonstrates that both types of measured elements have good sensitivity and linearity. This work paves the way for the complex SiC integrated temperature sensor design in the future.

SENSING PRINCIPLES

P-n diode

Among all the temperature sensing elements in ICs, one of the most often used elements is the p-n diode due to its long-term stability, high linearity, and excellent accuracy [22]. The p-n diode can be used as a temperature sensor due to the temperature dependency of forward voltage drop (V_F) under a certain bias current (I_{bias}). The ideal *I-V* characteristic of a p-n diode can be described by the following equation:

$$I_{bias} = I_s[\exp(qV_F/nkT) - 1] \quad (1)$$

where q is the elementary charge, n is the ideality factor, k is the Boltzmann constant, T is the temperature in Kelvin,

and I_s is the reverse saturation current, which can be expressed as [22]:

$$I_s \sim KT^{\gamma} \exp(-E_g/kT) \quad (2)$$

where K is a geometric parameter, γ is a process dependent parameter. As $qV_F \gg nkT$ is application for most cases, V_F can be then written as:

$$V_F = \frac{nkT}{q}(\ln I_{bias} - \ln K - \gamma \ln T) + \frac{nE_g}{q} \quad (3)$$

From Equation (3), it can be seen that V_F has an almost linear response to temperature under a constant I_{bias}. In silicon technology, dV_F/dT is around -2 mV/°C and fluctuates by 7% from room temperature to 200°C [23].

MOSFET

A diode-connected MOSFET is a common way to realize a temperature sensor in Si technology. For a MOSFET working in saturation region and strong inversion, i.e., diode-connected MOSFET, the drain current (I_{drain}) is (neglecting the effect of channel-length modulation):

$$I_{drain} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \quad (4)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, $\frac{W}{L}$ is the width/length ratio of the gate, V_{gs} is the gate-source voltage difference, and V_{th} is the threshold voltage. For common practice, a constant I_{bias} is injected into the drain terminal, and voltage drop $V_{F_{MOS}}$, i.e., V_{gs} is measured:

$$V_{F_{MOS}} = \left(\frac{2I_{bias}L}{\mu C_{ox}W}\right)^{\frac{1}{2}} + V_{th} \quad (5)$$

in which, the temperature sensitivity of $V_{F_{MOS}}$ is mostly contributed by μ and V_{th}. From [22]:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-\alpha} \quad (6)$$

$$V_{th}(T) = V_{th}(T_0) + \beta(T - T_0) \quad (7)$$

where α is a constant (between 1.5-2 for silicon), and β is strongly dependent on technology. The performance of the MOSFET-based temperature sensor is expected to be worse than the p-n diode because the $V_{th}(T)$ is defined by two temperature-dependent parameters and is non-linear. However, the advantage is that the design kit provides the model for MOSFET. This allows the simulation of the sensor together with the integrated readout, and the sensor performance is more predictable than the sensing component that is not modeled in the design kit.

DEVICE STRUCTURE

The IISB's SiC CMOS technology is performed on the 100 mm 4H-SiC wafer with an n-type epitaxial layer. N-well (NW), p-well (PW), shallow-n (SN), and shallow-p (SP) layers are implemented by ion implantations with different doses and energy. The implantation activation was done in argon atmosphere with a carbon cap. After this, the gate stack (thermal oxide/poly-Si) was grown and patterned. Formation of silicide was carried out at SN/NiAl and SP/Ti-Al interfaces for n-type and p-type contact, respectively. Finally, a metal stack (Ti/Al/Ti) was employed and patterned for the interconnection layer. The cross-sectional view of the N-/PMOS and p-n diode in IISB's SiC CMOS technology is demonstrated in Figure 1a, and the top view of both types of devices under the optical microscope is given in Figure 1b and 1c.

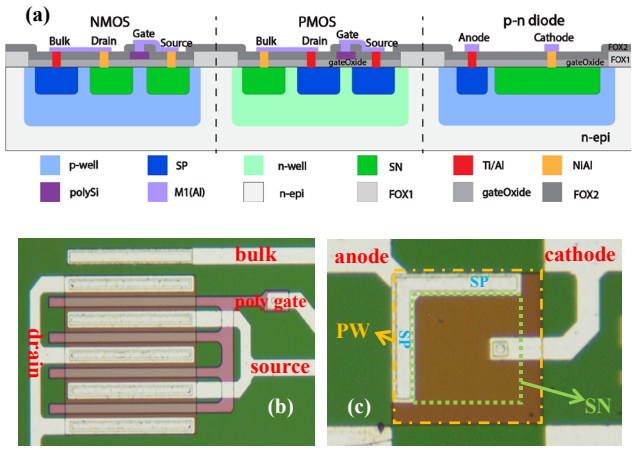

Figure 1: (a) The cross-section of the MOSFETs and p-n junction in the SiC CMOS process; Optical images of (b) a SiC PMOS with a gate length of 6 µm and gate width of 500 µm and (c) an 80 µm × 80 µm SiC p-n diode (the area encircled by the dashed green line indicates the metallurgic junction).

MEASUREMENT & RESULT

The measurement was performed using a Microtech Cascade probe station with a chuck that can be heated up to 200°C. The station is connected to a Keysight B1500A semiconductor device parameter analyzer controlled by IC-CAP software.

P-n diode

The p-n diodes were measured by the four-probe method to eliminate the wire resistance. The I-V curves of p-n diodes with four different metallurgical junction dimensions (50^2, 60^2, 70^2, and 80^2 µm^2) at room temperature and 200°C were obtained by sweeping the current from 0 to 10 µA, and the result is plotted in Figure 2. It can be seen that the device shows a typical diode behavior, where the device starts to conduct significantly after the so-called knee point voltage. With the increase in temperature, the knee point voltage decreases because of the increase of intrinsic carrier concentration. An additional observation is that the current under a certain voltage does not scale precisely with the device area, which could arise from the non-ideality of the contact. However, this effect needs to be further investigated.

Figure 3 demonstrates the temperature-dependent

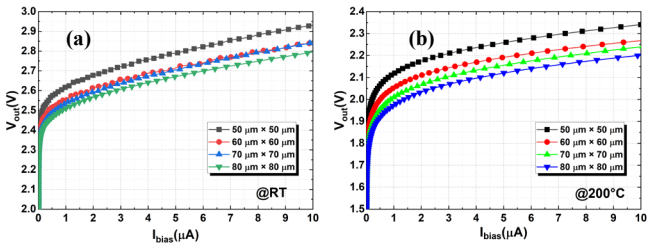

Figure 2: I-V curves of p-n diodes with different dimensions at (a) room temperature and (b) 200°C. The metallurgical areas of the measured diodes are 50^2 µm^2, 60^2 µm^2, 70^2 µm^2, and 80^2 µm^2.

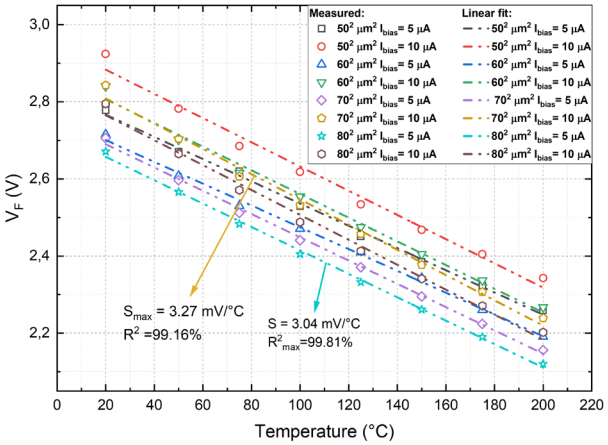

Figure 3: The forward voltage (V_F) of the p-n diode under a certain bias current from room temperature to 200°C, with a step of 25°C. The dotted lines are linear fits of the measured data (symbol).

voltage output when the diode is at constant current forward biasing (CCFB) mode. The evaluation of each device was from room temperature to 200°C, with steps of 25°C. Each device was biased at 5 µA and 10 µA, and the voltage drop was measured after the temperature was stable. The average sensitivity of all measured devices is 3.06 mV/°C. The maximum sensitivity is 3.27 mV/°C, which is obtained with a 70^2 µm² device when I_{bias} = 10 µA. Compared with Si technology, designers can generally expect a better sensitivity of p-n diode from SiC CMOS technology.

The linearity of temperature sensors is evaluated by the coefficient of determination (R^2) as in most of the work. In general, all devices demonstrate excellent linearity, and R^2 ranges from 98.64% to 99.81%. It is worth mentioning that the linearity of the device (with the same geometry) being biased at a smaller current is better. This is due to the non-linear temperature sensitivity of the series resistance, which will contribute more to the total sensitivity at higher biasing current.

MOSFET

Similar measurement procedures were performed on N-/PMOS temperature sensors with different $\frac{W}{L}$ ratios. Specifically, 20/6, 60/6, and 250/60 for NMOS, and 80/6, 200/6, and 500/6 for PMOS. The source/bulk and drain/gate terminals were shorted together for the diode-connected configuration.

The diode-like I-V characteristic of the MOSFET temperature sensors at room temperature and 200°C is illustrated in Figure 4. The knee point voltage is a useful

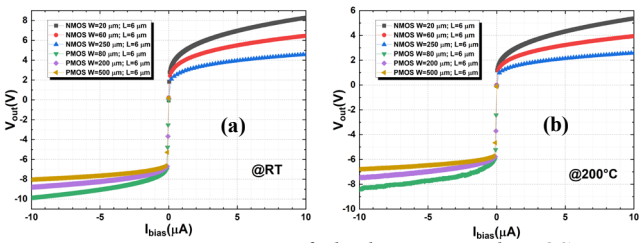

Figure 4: I-V curves of diode-connected MOSFETs with different dimensions at (a) room temperature and (b) 200°C. Diode-like behavior is obvious.

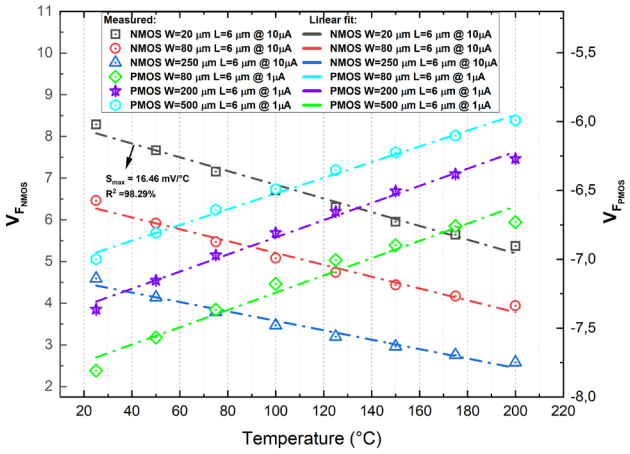

Fig. 5 Temperature-dependent $V_{F_{NMOS}}$ and $V_{F_{PMOS}}$ at different biasing current.

estimate for the MOSFET threshold voltage. At room temperature, the knee point voltage of the diode-connected N- and PMOS are approximately 2 V and -6.9 V, respectively, which aligns with the threshold voltage of the MOSFET reported previously [20]. When the temperature is 200°C, the knee point voltage becomes 1 V and -5.8 V for NMOS and PMOS, respectively. Therefore, β in Equation (7) is around -5.71 mV/°C for the NMOS and 6.29 mV/°C for the PMOS.

The temperature response of the MOSFET-based sensors were also measured in CCFB mode. I_{bias} for NMOS was 10 µA, while for PMOS, I_{bias} was 1 µA because of the much lower mobility of the holes. The temperature response of the MOSFET-based sensor is given in Figure 5. In general, The sensitivity of the MOSFET temperature sensor is larger than the p-n diode. The maximum sensitivity of the measured device is 16.46 mV/°C. However, the linearity of the output is compromised, and R^2 is only up to 99.11%. This is due to the fact that the sensitivity is a function of both threshold voltage and mobility. It is also notable that the NMOS temperature sensor is 2~3 times more sensitive compared to the PMOS counterpart. As mentioned above, the change in the threshold voltage of P- and NMOS is almost the same, so it can be inferred that the difference in the temperature dependency of electron and hole mobility causes the

Table 1: A comparison of the reported SiC temperature sensors with literature.

Ref.	Max. Sensitivity (mV/ºC)	Max. R^2 (%)	Max. Temperature (ºC)	Technology/Compatibility with ICs
[13]	4.50	99.93	460	Vertical diode/no
[14]	5.11	99.90	300	Vertical diode/no
[15]	1.18	99.97	167	Vertical diode/no
[16]	3.50	Poor	600	Planar diode/ not mentioned
This work	16.46	99.24	200	FhG SiC CMOS/yes
This work	3.27	99.81	200	FhG SiC CMOS/yes

difference in sensitivity. In conclusion, Compared with other SiC discrete temperature sensors summarized in Table 1, the reported sensors have great advantages in terms of implementing the monolithically integrated temperature sensor.

CONCLUSION

In this paper, we have introduced FhG IISB low-voltage SiC CMOS technology and characterized two categories of temperature sensors, i.e., p-n diode and diode-connected MOSFET, in this emerging technology. All the sensors are measured up to 200°C and show stable performance at elevated temperatures. The SiC p-n diode temperature sensor has excellent linearity (R^2_{max} = 99.81%) and greater sensitivity (averaged sensitivity 3.06 mV/°C) than its counterpart in Si technology. For SiC diode-connected MOSFETs, the sensitivity, especially for NMOS, is larger than the diode. However, the linearity is compromised.

Future work will include investigation of other sensing components, characterization at higher temperatures, and integration with SiC ICs.

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