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22.3 A Multi-Qubit Cryo-CMOS SoC with Polar-Based Electron-Spin and PDM-Based Nuclear-Spin Controllers for Color Centers in Diamond

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Abstract

Co-integrating a cryo-CMOS SoC with nitrogen-vacancy (NV) centers in diamond enables a scalable quantum platform. This work introduces a combined Class-DE RFDAC and class-D PDM driver for multi-qubit electron- and nuclear-spin control. A switch allows shared coil driving enabling multi-band 2.5-3.2GHz(1.9-2.1MHz), large-current 70mA(38mA), high-Rabi frequency 2.31MHz(1.93kHz) and high-fidelity 99.34(3)%(99.78(2)%) electron(nuclear) quantum logic gates with decoupled coherence times >50ms.

Quantum bits (qubits) based on nitrogen-vacancy (NV) centers in diamond combine high-fidelity electron-spin gates with long-coherence nuclear-spin memories, making them strong candidates for exploring quantum computation and networking. Electron spins enable fast GHz control and photon-mediated entanglement for distributed quantum architectures [1,2], while coupled nuclear spins provide stable memories [3] and localized quantum error correction [4]. NV centers operate near 4K [1], a temperature where cryostats offer significant cooling power. Such qubits can then be directly co-integrated with cryo-CMOS controllers, removing interconnect bottlenecks and enabling scalable quantum processors [5–7].

Figure 22.3.1 shows a quantum processing unit (QPU) composed of many NV-center unit cells, each hosting one electron and several nuclear spins in a static magnetic field B_0. The cells, spaced by 1mm, are interconnected via optical waveguides for readout and entanglement, while cryo-CMOS chips above each cell generate GHz/MHz pulses, control the optics, and read out single-photon detectors.

The B_0 field splits the energy levels of the electron spin, defining its Larmor frequency ($f_{0,e}$~2.5GHz), with slight variations due to the B_0 non-uniformity across the QPU. Hyperfine coupling to local Nitrogen-14 (^{14}N) and Carbon-13 (^{13}C) nuclear spins shifts $f_{0,e}$ by ±2.5MHz, creating multiple resonance peaks. Thus, to achieve high-fidelity single-qubit electron gates, the controller must generate fast (<200ns), broadband (>5MHz), and spectrally flat pulses, requiring ~100mAp of GHz current due to the ~20µm coil-to-electron-spin spacing.

Each unit cell also hosts several randomly positioned ^{13}C nuclear spins with distinct hyperfine couplings to the electron spin and unique Larmor frequencies ($f_{0,c}$). Due to their smaller gyromagnetic ratio, ^{13}C spins are limited to a lower Rabi frequency, which then requires long (>100ms) pulses with large amplitude (>40mAp).

The prior-art cryo-CMOS NV controller [7] demonstrated electron-spin driving, but had key limitations: it relied on a dedicated DC magnetic field regulator and a dedicated coil to align $f_{0,e}$ across units, degrading system scalability due to the extra coil, and lowering qubit coherence due to the regulator noise. Also, its limited phase resolution and amplitude shaping affected gate fidelity. Moreover, it did not demonstrate nuclear spin control of ^{13}C spins [8], essential for realizing a scalable NV-based quantum computer.

The proposed electron and nuclear spin controller (Fig. 22.3.1(top-right)) overcomes those limitations by introducing 1) a digital-intensive intermediate-frequency (IF) generation with single-sideband up-conversion, allowing each cell to operate at its unique Larmor frequency due to B_0 inhomogeneity, eliminating the need for DC field regulation. Setting the LO (f_{LO}) 20MHz above the Larmor frequencies minimizes undesired qubit rotations from LO leakage. 2) An efficient digital architecture for precise amplitude and phase; 3) A class-D Pulse-Density Modulator (PDM) to efficiently generate accurate MHz pulses for nuclear spins, using a DS modulator for quantization-noise shaping and ADC feedback to reduce sensitivity to supply and process spread; 4) A switchable output passive network that allows a single coil for both GHz and MHz driving, improving coil-to-qubit coupling and scalability.

For the electron-spin controller (Fig. 22.3.2), the digital polar architecture comprises the RFDAC for amplitude modulation (AM) and a single-sideband upconverter for frequency shifting and phase modulation (PM). In the PM path, a numerically controlled oscillator (NCO) generates the required IF tone [9] and a digital rotational CORDIC [10] converts the truncated triangular phase input into four sinusoidal quadrature streams. Unlike prior art [11–13] that rely on ~1.6kb sinusoidal lookup tables (LUTs) to achieve <0.2° phase accuracy, the CORDIC uses only 8 LUT entries for storing arccot(2^1, 2^2, …, 2^8) phase steps (88 bits total) and performs rotations with bit shifts and summations. This reduces the area by 10× and the simulated power consumption by 6×, while also enabling direct phase word (PW) inputs as required for instant phase updates in qubit gates.

Four 6-bit resistive unary-weighted DACs then generate the quadrature IF currents, which are up-converted by single-sideband passive mixers to f_{LO}-f_{IF}. Since the DAC output common-mode voltage is approximately ~V_{DD}/2, a level shifter raises the LO voltages to 0.5–1.5V_{DD} to minimize mixer size and on-resistance. The mixers' output currents are converted to voltage by a transimpedance amplifier (TIA), whose low input impedance ensures current-mode DAC operation and suppresses voltage swings at the mixer terminals, improving linearity. Five inverter stages convert the TIA's sinusoidal output into frequency and phase-modulated square wave signals for RFDAC.

The RFDAC consists of 255 unary-weighted cells, each individually addressable to modulate the driver on-resistance and enable arbitrary envelope shaping. As the RFDAC requires 25% duty-cycle input clocks to operate in class-DE switching mode, each cell includes four (N)AND gates to convert the 50% duty-cycle quadrature inputs into the 25% pulses. Its matching network includes: (i) a series coil (L_{coil}) magnetically coupled to the electron spin, (ii) shunt capacitors (C_X) absorbing the parasitics of both GHz and MHz controllers for zero-voltage/current switching, and (iii) a series capacitor (C_S) incorporating the parasitics from the matching network switch transistors. Due to the voltage division between the coil parasitic resistance and the AM-dependent on-resistance class-DE driver, the amplitude and phase of the coil current do not scale linearly with the AM codeword. To correct this, two on-chip predistortion LUTs are used: one in the AM path and one before the PM data enters the CORDIC. Finally, since the AM and PM data experience different paths, a controllable delay aligns them before being combined in the RFDAC.

The nuclear-spin controller (Fig. 22.3.3) adopts a class-D output stage for high linearity and power efficiency while driving large currents. For the signal generation, 10 different 24-bit NCOs track the frequency (f_{nco}) and phase with an accuracy of 3Hz and 2e-5°, respectively, to address 10 carbon spins in the 200kHz bandwidth and enable driving of 2 tones simultaneously. The sawtooth NCO output is folded into a triangular waveform to suppress the even harmonics of f_{nco}, while avoiding another CORDIC or LUT. The amplitude of the triangular waveform is modulated using SRAM data, truncated to 10bit, and fed into a digital 1bit DS modulator that shapes the quantization noise for optimal resolution. The DS modulator allows 1) digital feedback from the 1bit quantizer output for minimum noise, power dissipation, and high linearity, and 2) analog feedback, which uses a SAR ADC sensing L+, to improve the robustness to supply variations and process spread, e.g., in the on-resistance of the output-bridge devices. Operating at 50MHz, the 2nd-order feed-forward loop filter uses zero compensation to counteract the analog-feedback path delay and a programmable resonator coefficient g to optimally place the resonator notch for minimum in-band quantization noise. The class-D output stage is implemented in a half-bridge structure with large devices to achieve a low on-resistance R_{ON}, allowing the use of low supplies ($\pm V_{sup}$) to reduce the power consumption for the same coil current, while also filtering high-frequency current noise thanks to the large L_{coil}/R_{ON} time constant. However, as excessively large devices would introduce more parasitic capacitance that cannot be completely absorbed in the matching network of the GHz driver, this design limits R_{ON} to 2Ω to enable a 40mAp output current with ±100mV supplies.

Figure 22.3.3 also shows the schematic of the matching-network switch, with series thick-oxide transistors M1-M2 designed to withstand large voltage swings when off during GHz operation. In MHz mode, EN is high, turning on M1 and M2 to form a low-impedance path to ground. In GHz mode, the transistors act as back-to-back diodes, limiting M2's AC gate voltage to keep it off and ensuring the gate-oxide voltages of both transistors remain within the foundry-specified limits.

The chip (Fig. 22.3.7) was fabricated in 40nm CMOS and characterized at room (RT) and cryogenic temperatures (CT). An alternate GHz driver with on-chip driving coil (L_{coil}) was tested in a cryogenic probe station using an on-chip pick-up coil with results shown in Fig. 22.3.4(left). At 2.5GHz(3.0GHz), it achieves >80(70)mAp coil current and >270(600)% output-stage current efficiency, while drawing 30(15)mA from a 1.1(0.85)V supply at RT (CT), and showing SNR= 53(52)dB over 50MHz bandwidth. The controller can generate arbitrary waveforms with 3ns-3µs pulse length, and <10kHz and <0.5° frequency and phase accuracy across 25MHz f_{IF} bandwidth. The MHz driver, measured in a liquid-helium bath with an on-chip buffer (Fig. 22.3.4(right)), achieves 57(58)dB SNDR in single-tone tests and 47(51)dB SFDR in two-tone tests over 1.9-to-2.1MHz.

To demonstrate the quantum controller's performance (Fig. 22.3.5), the cryo-CMOS was bonded to an NV-center sample with a gold-patterned stripline (L_{coil}=1.1nH) and placed in

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a cryostat at ~6K. RT electronics and optics were used for (^{14}N, ^{13}C, electron) spin initialization and readout. A permanent magnet (B_0=1980 Gauss) induces $f_{0,e}$=2.49GHz for electron spin and $f_{0,C0}$=2.46, $f_{0,C1}$=2.03MHz for two ^{13}C spins. The cryo-CMOS driver achieves a maximum Rabi frequency $f_{R,e}$=2.31MHz for the electron spin and $f_{R,C0}$=1.93kHz, $f_{R,C1}$=1.16kHz for the nuclear spins. The qubit characteristic chevron patterns were demonstrated for the electron spin by sweeping the f_{IF} frequency of the GHz NCO over the range f_{LO}-20±5MHz and for the nuclear spin by sweeping the MHz NCO over the range 2.025±0.1MHz. Coherence time T_2 could be extended from 0.8ms to 50ms by increasing N_{Dec} decoupling pulses in an echo experiment. For the electron {nuclear} spin, an average gate fidelity of 99.34(3)% {99.78(2)%} was found by gate set tomography (GST) with depth L=128 {L=64} [14].

The cryo-CMOS consumes an average of 45mW, 17mW and 12mW for the GHz and MHz drivers and in idle mode, respectively. Compared to other works (Fig. 22.3.6), this paper shows the first cryo-CMOS high-fidelity gate control of both nuclear and electron spins, proving co-integration of color centers with cryo-CMOS as a scalable candidate for quantum computing.

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References:
[1] S. Pezzagna and J. Meijer, "Quantum computer based on color centers in diamond," *Applied Physics Reviews*, vol. 8, no. 1, p. 011308, Feb. 2021. https://doi.org/10.1063/5.0007444
[2] A. J. Stolk *et al.*, "Metropolitan-scale heralded entanglement of solid-state qubits," *Science Advances*, vol. 10, no. 25, eadl4863, Jun. 2024. https://doi.org/10.1126/sciadv.adl4863
[3] C. E. Bradley *et al.*, "A ten-qubit solid-state spin register with quantum memory up to one minute," *Physical Review X*, vol. 9, no. 3, 031045, Sep. 2019. https://doi.org/10.1103/PhysRevX.9.031045
[4] M. H. Abobeih *et al.*, "Fault-tolerant operation of a logical qubit in a diamond quantum processor," *Nature*, vol. 606, pp. 884–889, Jun. 2022. https://doi.org/10.1038/s41586-022-04884-5
[5] R. Ishihara *et al.*, "3D integration technology for quantum computer based on diamond spin qubits," *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2021, pp. 1–4. https://doi.org/10.1109/IEDM19574.2021.9720552
[6] L. Enthoven, M. Babaie, and F. Sebastiano, "Optimizing the electrical interface for large-scale color-center quantum processors," *IEEE Transactions on Quantum Engineering*, vol. 5, pp. 1–17, 2024. https://doi.org/10.1109/TQE.2024.3416836
[7] N. Fakkel *et al.*, "A cryo-CMOS controller with class-DE driver and DC magnetic-field tuning for quantum computers based on color centers in diamond," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 11, pp. 3627–3643, Nov. 2024. https://doi.org/10.1109/JSSC.2024.3459392
[8] T. H. Taminiau *et al.*, "Detection and control of individual nuclear spins using a weakly coupled electron spin," *Physical Review Letters*, vol. 109, 137602, Sep. 2012. https://doi.org/10.1103/PhysRevLett.109.137602
[9] Analog Devices, Inc., "A technical tutorial on digital signal synthesis," Application Note, 1999, pp. 1–122. https://www.analog.com/media/en/training-seminars/tutorials/450968421DDS_Tutorial_rev12-2-99.pdf
[10] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Transactions on Electronic Computers*, vol. EC-8, no. 3, pp. 330–334, Sep. 1959. https://doi.org/10.1109/TEC.1959.5222693
[11] D. J. Frank *et al.*, "A cryo-CMOS low-power semi-autonomous qubit state controller in 14 nm FinFET technology," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 360–361. https://doi.org/10.1109/ISSCC42614.2022.9731538
[12] J. S. Park *et al.*, "A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22 nm FFL FinFET technology," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 208–209. https://doi.org/10.1109/ISSCC42613.2021.9365762
[13] B. Patra *et al.*, "A scalable cryo-CMOS 2-to-20 GHz digitally-intensive controller for 4 × 32 frequency-multiplexed spin qubits/transmons in 22 nm FinFET technology for quantum computers," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 304–306. https://doi.org/10.1109/ISSCC19947.2020.9063109
[14] H. P. Bartling *et al.*, "Universal high-fidelity quantum gates for spin qubits in diamond," *Physical Review Applied*, vol. 23, 034052, Mar. 2025. https://doi.org/10.1103/PhysRevApplied.23.034052
[15] J. Yoo *et al.*, "A 28-nm bulk-CMOS IC for full control of a superconducting quantum processor unit-cell," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 506–508. https://doi.org/10.1109/ISSCC42615.2023.10067292
[16] Y. Guo *et al.*, "A cryo-CMOS quantum computing unit interface chipset in 28 nm bulk CMOS with phase-detection based readout and phase-shifter based pulse generation," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2024, pp. 476–478. https://doi.org/10.1109/ISSCC49657.2024.10454392
[17] L. Guevel, C. Wang, and J. C. Bardin, "A 22 nm FD-SOI <1.2 mW/active-qubit AWG-free cryo-CMOS controller for fluxonium qubits," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2024, pp. 1–3. https://doi.org/10.1109/ISSCC49657.2024.10454522

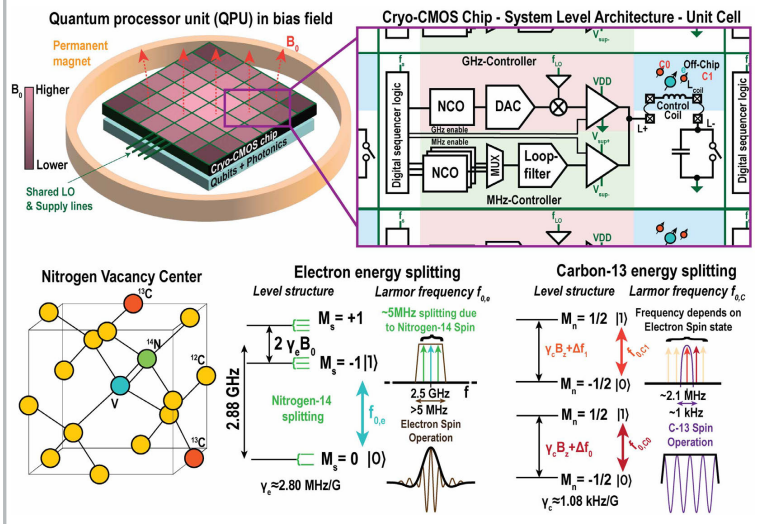


Figure 22.3.1: Quantum processor unit (QPU) based on nitrogen-vacancy (NV) centers and integrated cryo-CMOS SoC (top). The NV-center energy splitting and corresponding Larmor frequencies for electron and nuclear driving (bottom).

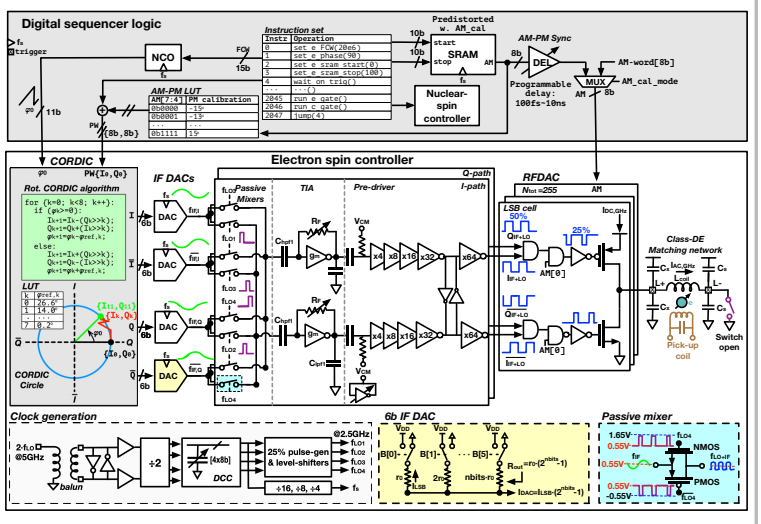


Figure 22.3.2: Electron spin controller comprising digital sequencer controller, SRAM, rotational CORDIC with f_{IF} DACs, quadrature mixers and pre-drivers for up-conversion to f_{LO}-f_{IF}, and Class-DE RFDAC output stage to drive the off-chip coil.

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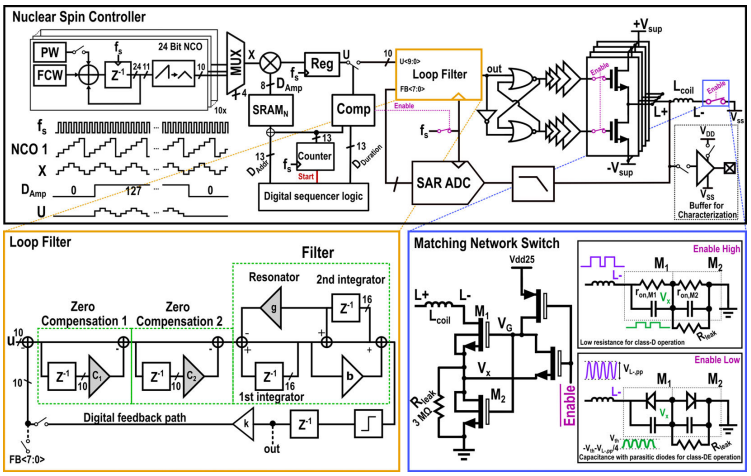


Figure 22.3.3: Nuclear spin controller comprising a class-D output stage with low supplies ($\pm V_{sup}$) and 10 NCOs for phase tracking (top); loop filter and thick oxide matching network switch using transistors to share L_{coil} (bottom).

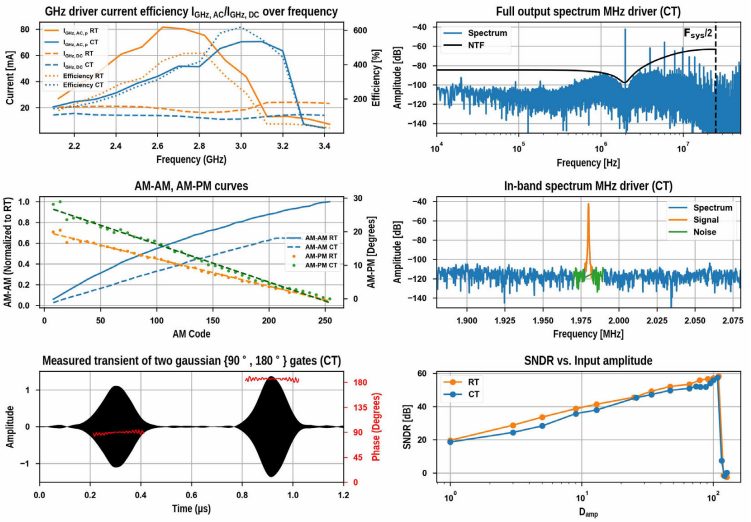


Figure 22.3.4: Measured GHz-controller driver current efficiency, AM-AM and AM-PM, and phase control pulses(left); MHz-driver out-of-band PSD, in-band spectrum and SNDR using the analog feedback (right).

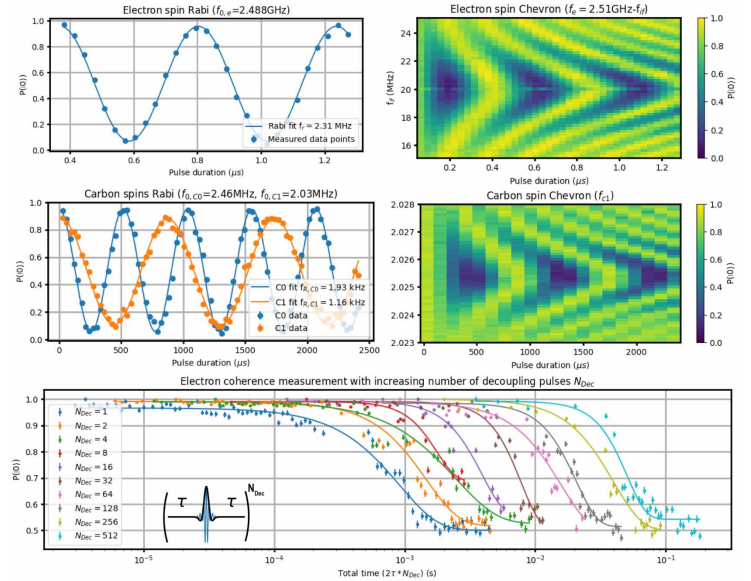
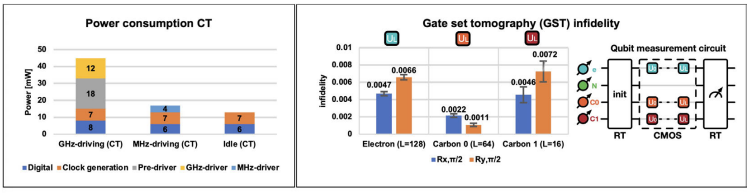


Figure 22.3.5: Rabi oscillation and chevron pattern with NCO sweep for electron spin (top), and for nuclear spins (middle); Coherence measurement (bottom).



Qubit controllers	This work		[7] JSSC 2025	[17] ISSCC 2024	[16] ISSCC 2024	[15] ISSCC 2023	[11] ISSCC 2022	[12] ISSCC 2021
Qubit type	NV electron	NV carbon	NV electron	Fluxonium	Transmon	Transmon	Transmon	Spin
Qubit temperature	6 K		4.5 K	20 mK	10 mK	20 mK	20 mK	20 mK
Architecture	Polar	PDM	Const. Env.	Const. env.	Polar	I/Q Direct	I/Q SSB	I/Q SSB
Cryo-CMOS temp.	6 K		4.5 K	4 K	3 K	3 K	3 K	3 K
AC driver Class	DE	D	DE	D	A(B)†	A(B)†	A(B)†	A
Frequency range	2.5-3.2 GHz	1.9-2.1MHz	2.6-3 GHz	0.8-1.2 GHz	4-6 GHz	4-8 GHz	4.5-5.5 GHz	11-17 GHz
Maximum I_{AC} [mAp]	70	36	30.1	N.A.	0.8*	N.A.	0.6*	4.0*
SNR [dB]	>52	>57	>47	N.A.	>40	N.A.	N.A.	>44
Rabi frequency	>2.31 MHz	>1.16 kHz	2.5 MHz	77 MHz‡	N.A.	91 MHz‡	23.5 MHz‡	N.A.
1-Qubit gate fidelity	>99.34%	>99.78%	>98%	>99.6%	N.A.	>99.6%	>99.2%	>99.7%
Chip Area [mm²]	1.55		0.59	1	1.2	7	1.6	~4
Technology	40-nm		40-nm	22-nm	28-nm	28-nm	14-nm	22-nm
Power per qubit under active control	45 mW	17 mW	16.8 mW	1.2 mW	13.7 mW	<4 mW	23 mW	90 mW∞

†Derived from schematic; * Assuming P_{out} with 50Ω; ‡ Based on reported gate duration; ∞Estimated

Figure 22.3.6: Summary of the electrical and quantum-control performance and benchmark with prior art.

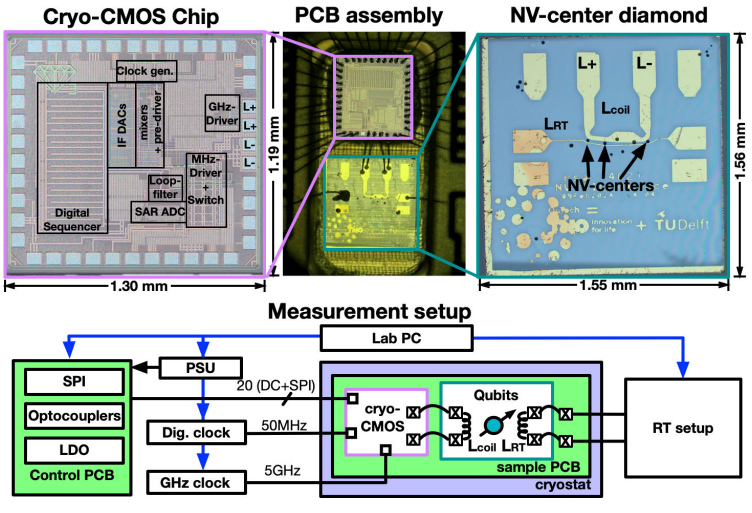


Figure 22.3.7: Qubit measurement assembly of the cryo-CMOS chip and NV-center sample. Two striplines are patterned close to the NVs; L_{coil} is bonded to the cryo-CMOS; L_{RT} is used with the RT setup as experimental reference.

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