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Revisiting the Reverse Switched Current of Buck, Boost, and Buck–Boost Converters in Voltage-Mode TCM–ZVS Control Considering Parasitic Resistances

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***Abstract*—Triangular current mode (TCM) zero-voltage switching (ZVS) modulation method is widely adopted in power electronic converters to achieve acceptable efficiency in high switching frequency operations. For bidirectional dc–dc converters, in order to realize ZVS turn-ON, a reverse inductor current can be utilized for this purpose through variable frequency control. In this article, this reverse switched current is revisited considering the parasitic resistances presented in the MOSFET switches and the inductor for three common types of dc–dc converters, i.e., buck, boost, and buck–boost converters, which study was normally neglected in the previous research. Universal closed-form equations of the modified duty cycle and switched current are derived, which can be utilized to calculate the reverse current under different operating conditions. It is found that the parasitic resistances can have a negative impact on the switched current value, and this may lead to an unexpected loss of ZVS turn-ON. A laboratory prototype of a four-switch buck+boost converter featuring TCM–ZVS buck, boost, and buck–boost operation capability was built to investigate and verify the proposed concepts. The operating voltage and power range are from 100 V to 400 V, and 300 W to 1 kW, respectively.**

***Index Terms*—DC–DC power converters, parasitic resistances, triangular current mode (TCM), zero-voltage switching (ZVS).**

I. Introduction

NONISOLATED dc–dc converters can operate as a power buffer interfacing different power stages, which makes them indispensable in many applications, including battery energy storage systems, photovoltaic applications, wireless power transfer, etc. [1], [2], [3]. In pursuit of achieving high power density, switching frequency has been increasing over the last decades due to the continual advancement of power semiconductor device technology [4]. However, a high switching frequency is also accompanied by increased switching losses, even with the adoption of wide band-gap devices [5]. Therefore, soft switching techniques, including zero-voltage switching (ZVS) and zero-current switching (ZCS), are still required in order to guarantee a satisfactory efficiency.

A state-of-the-art review on soft switching technologies for nonisolated dc–dc converters is well presented in [6]. Among the various soft switching implementations, triangular current mode (TCM) modulation is a widely adopted and relatively simpler technique to realize soft switching for conventional power converters without the need to use auxiliary circuits, which also maintains the fundamental characteristics of the conventional topology [7]. In order to realize TCM–ZVS modulation, the diode presented in the unidirectional buck, boost, and buck–boost converters for the inductor current freewheeling is required to be replaced by a synchronous MOSFET, thus making it bidirectional. Fig. 1 shows the circuit topologies of the bidirectional buck, boost, and buck–boost converters with parasitic resistances presented in MOSFET and inductor [8]. In TCM–ZVS modulation, the reverse switched inductor current is the key to realize ZVS turn-ON of switch S_1 (cf., Fig. 1). TCM–ZVS modulation is normally accompanied by variable-frequency control to maintain the reverse current of I_0 (cf., Fig. 2), and the closed-form equations can be simply solved under ideal cases. However, due to nonideal factors, including parasitic resistances, this reverse current might change. To guarantee the ZVS operation, an inductor current zero crossing detection circuit can be implemented [9], which increases the system complexity and may introduce more losses due to additional sampling circuits. In addition, the detection of switching current operating at high frequencies of hundreds of kHz is also a challenge [10]. Therefore, the realization of TCM–ZVS operation without an inductor or switch current detection is preferred. Apart from the current detection method, a conservative and simple solution is to select a reverse current large enough (an absolute value) to ensure ZVS margin. However, a larger reverse current results in a larger peak inductor current and its root-mean-square (rms) value, and thus the circuit conduction losses increase [11]. Most of the previous research did not consider the parasitic resistance when evaluating TCM–ZVS operation. In [12] and [13], the parasitic resistance is considered for the high step-up and noninverting buck–boost converters operating under continuous conduction mode (CCM). In this mode, the inductor current is assumed to be a dc constant during the analysis, which is not the case for TCM operation since the inductor current has a large peak-to-peak ripple.

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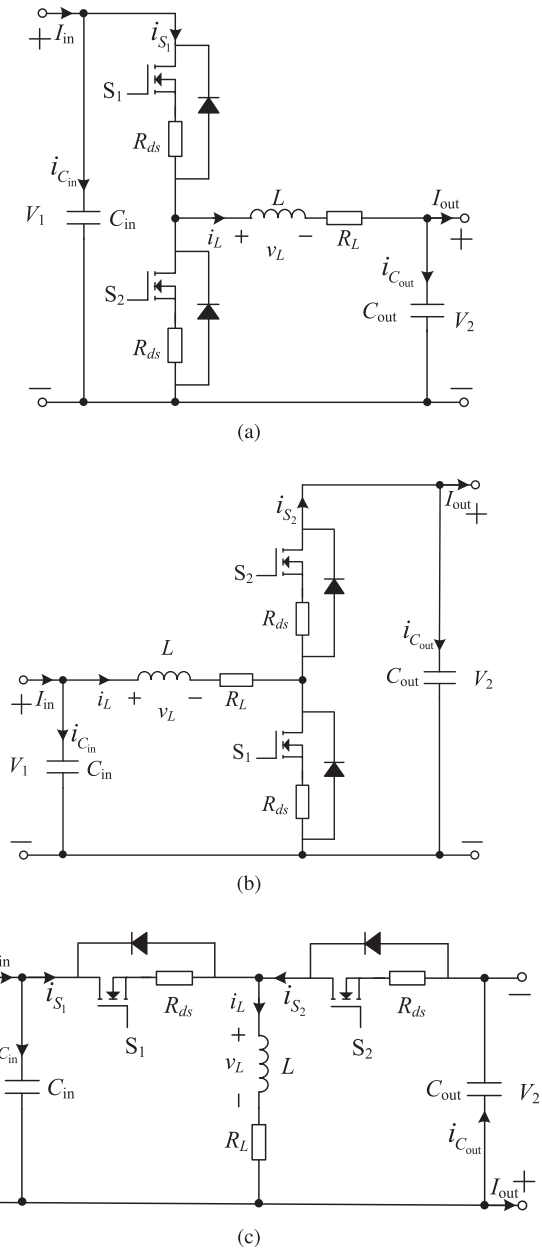


Fig. 1. Circuit topologies of bidirectional nonisolated DC–DC converters with parasitic resistances. (a) Buck converter. (b) Boost converter. (c) Buck–boost converter.

The main purpose and contribution of this article is to reevaluate the reverse switched current of the TCM–ZVS modulation for the three most common types of nonisolated dc–dc converters taking into account the parasitic resistances. Detailed and universal closed-form equations are derived for the new modified duty cycle and switched current under variable-frequency voltage-mode TCM–ZVS control, which, to the best of the authors' knowledge, has not been analyzed elsewhere in the literature. It is found by theoretical calculation, simulation, and experimentation that the parasitic resistance has a different impact on the reverse switched current for buck and boost mode operations even with same voltage and power values adopted

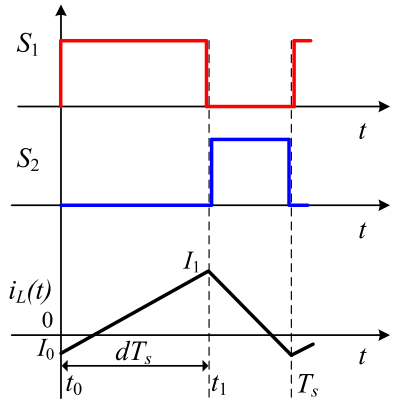


Fig. 2. Inductor current waveform and gating signals under TCM–ZVS modulation for the three types of DC–DC converters in Fig. 1.

by this article, and this phenomenon cannot be revealed by the previous formulas derived from ideal cases. Compared to the previous research, the newly derived formulas taking into account the parasitic resistance reveal the reverse current change at different operating points, and it can also serve as a better theoretical guidance for reverse current selection.

The rest of the article is organized as follows. In Section II, the variable-frequency TCM–ZVS modulation and its universal voltage-mode control method are described. In Section III, newly closed-form equations for modified duty cycle and switched current are derived for three common types of dc–dc converters, i.e., buck, boost, and buck–boost converters. In Section IV, design considerations including input and output capacitor selection and simulation verification are given. In Section V, the switched ZVS current is evaluated through a silicon carbide (SiC) MOSFET-based four-switch buck+boost (FSBB) converter featuring TCM–ZVS buck, boost, and buck–boost mode operation capability. Finally, Section VI concludes this article.

II. Description of Variable-Frequency TCM–ZVS Modulation

In this section, a brief mathematical description of variable-frequency TCM-ZVS modulation for buck, boost, and buck–boost converters will be given under ideal circumstances followed by an introduction of its corresponding voltage-mode control.

A. Brief Review of Variable-Frequency TCM–ZVS Modulation

The switching waveforms of TCM–ZVS modulation is given in Fig. 2.

Taking the buck converter as an example, without considering dead time and parasitic resistances, the inductor current waveform can be expressed as follows with $t_0 = 0$:

$$i_L(t) = \begin{cases} I_0 + \frac{V_1 - V_2}{L} t, & 0 < t \le t_1 \\ I_1 - \frac{V_2}{L}(t - t_1), & t_1 < t \le T_s \end{cases} \quad (1)$$

TABLE I
SUMMARY OF DUTY CYCLE AND FREQUENCY IN IDEAL CASE

Converter type	Duty cycle	Frequency
Buck converter	$d = \frac{V_2}{V_1}$	$f_s = \frac{V_1 d(1-d)}{2L(I_{\text{out}} - I_0)}$
Boost converter	$d = 1 - \frac{V_1}{V_2}$	$f_s = \frac{V_1 d(1-d)}{2L[I_{\text{out}} - I_0(1-d)]}$
Buck–boost converter	$d = \frac{V_2}{V_1+V_2}$	$f_s = \frac{V_1 d(1-d)}{2L[I_{\text{out}} - I_0(1-d)]}$

where V_1 and V_2 are the input and output voltages, L is the inductance, T_s is the switching period, d is the duty cycle of S_1, namely, $t_1 - t_0 = dT_s$, I_0 and I_1 are the valley and peak current shown in Fig. 2.

From (1), the voltage gain can be derived as

$$G_v = \frac{V_2}{V_1} = d. \tag{2}$$

Since $I_{\text{out}} = \frac{I_0 + I_1}{2}$, combining (1) and (2), the switching frequency can be derived as

$$f_s = \frac{V_1 d(1-d)}{2L(I_{\text{out}} - I_0)}. \tag{3}$$

The formulas of duty cycle and frequency for boost and buck–boost converters can be derived similarly. Table I summarizes the results for these three dc–dc converters [14], [15]. In Table I, d is all defined as the duty cycle of S_1. For single-switch buck–boost converter, the output voltage is inverted, so the reference direction of output voltage polarity is reversed compared with buck or boost converters [cf., Fig. 1(c)].

B. Brief Introduction of Voltage-Mode TCM–ZVS Control

A universal voltage-mode variable-frequency TCM–ZVS modulation control method for buck, boost, and buck–boost converters without inductor current detection is also proposed herein based on the formulas in Table I. An example of this control for buck converter is shown in Fig. 3, which can be easily modified for boost and buck–boost converters as well. Herein, the switching frequency is determined by the formulas in Table I, while the duty cycle of d is regulated to meet the output voltage requirement.

As it can be seen from Fig. 3, the output voltage of the converter can be regulated well due to the direct feedback control with the reference voltage. However, the inductor current is not controlled directly, and therefore, the nonideal factor, including parasitic resistances, will affect the reverse current of I_0, which is required to be a negative value in order to discharge the parasitic capacitance of C_{oss} from S_1 (or to charge C_{oss} from S_2) during the dead time to ensure the ZVS turn-ON of S_1. Therefore, to study the influence from the nonideal factors on I_0 under a voltage-mode TCM–ZVS modulation control is meaningful and necessary. In this article, the parasitic resistances from MOSFETs and inductor will be considered and studied.

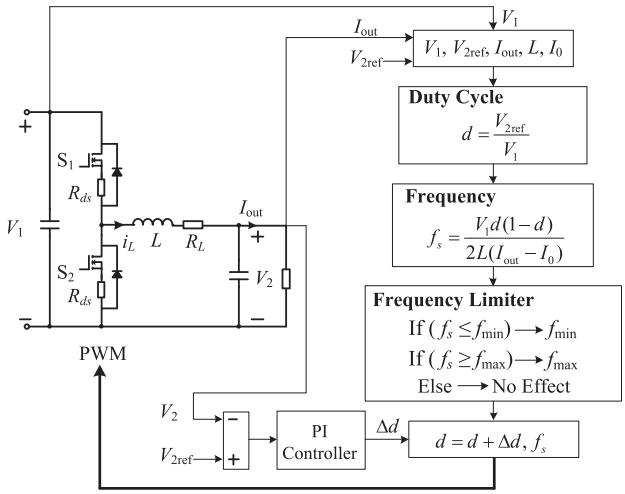


Fig. 3. Universal voltage-mode variable-frequency TCM–ZVS modulation control diagram, buck converter is taken as an example.

III. TCM–ZVS MODULATION CONSIDERING PARASITIC RESISTANCES

In this section, detailed and universal closed-form equations for the modified duty cycle and switched current of I_0 in voltage-mode TCM–ZVS modulation considering parasitic resistances will be derived.

A. Derivation Procedures of General Expressions

The parasitic resistances from the MOSFETs and inductor are defined as R_{ds} and R_L, respectively, as shown in Fig. 1. Some assumptions are made for the following analysis:

1) the inductance is a constant;
2) the gating signals for S_1 and S_2 are complementary and their dead time is neglected;
3) the inductor current connecting I_0 and I_1 is a straight line;
4) during reverse conduction, the current only passes through the MOSFET channel, not through the body diode. These assumptions are further discussed in Section IV-D.

1) During the ON Period of S_1: Defining d as the duty cycle of S_1 for all the three converter topologies in Fig. 1. When S_1 is ON, the voltage across the inductor can be expressed as follows, for buck converter, it is:

$$v_L(t) = V_1 - V_2 - (R_{ds} + R_L) i_L(t). \tag{4}$$

For both boost and buck–boost converters, it is

$$v_L(t) = V_1 - (R_{ds} + R_L) i_L(t). \tag{5}$$

In (4) and (5), $i_L(t)$ is the inductor current, and its reference direction is given in Fig. 1.

Based on (4) and (5), the net change of the inductor current during ON period of S_1 can be derived. For buck converter, it is

$$I_1 - I_0 = \int_{t_0}^{t_1} \frac{(V_1 - V_2) - (R_{ds} + R_L) i_L(t)}{L} dt. \tag{6}$$

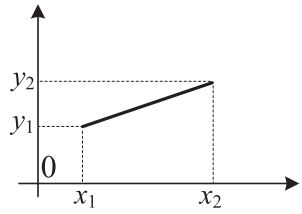


Fig. 4. Linear function.

Similarly, for both boost and buck–boost converters, it is

$$I_1 - I_0 = \int_{t_0}^{t_1} \frac{V_1 - (R_{ds} + R_L) i_L(t)}{L} dt. \tag{7}$$

Since the integral of a linear function (cf., Fig. 4) can be simply solved by (8), so, (6) and (7) can be simplified to (9) and (10), respectively

$$\int_{x_1}^{x_2} f(x)dx = \int_{x_1}^{x_2} \left[\frac{y_2 - y_1}{x_2 - x_1}(x - x_1) + y_1\right] dx = \frac{(y_1 + y_2)(x_2 - x_1)}{2} \tag{8}$$

$$I_1 \left[1 + \frac{(R_{ds} + R_L)T_s}{2\,L} d\right] = I_0 \left[1 - \frac{(R_{ds} + R_L)T_s}{2\,L} d\right] + \frac{(V_1 - V_2)T_s}{L} d \tag{9}$$

$$I_1 \left[1 + \frac{(R_{ds} + R_L)T_s}{2\,L} d\right] = I_0 \left[1 - \frac{(R_{ds} + R_L)T_s}{2\,L} d\right] + \frac{V_1 T_s}{L} d. \tag{10}$$

Equations (9) and (10) can be reexpressed by the same form as follows:

$$I_1(1 + kd) = I_0(1 - kd) + md \tag{11}$$

where $k = \frac{(R_{ds} + R_L)T_s}{2\,L}$. In (11), for buck converter, $m = \frac{(V_1 - V_2)T_s}{L}$ while for boost and buck–boost converters, $m = \frac{V_1 T_s}{L}$.

2) During the ON Period of S_2: Similar to the previous analysis, during the ON period of S_2, the net change of the inductor current can be expressed as follows, for both buck and buck–boost converters, it is:

$$I_0 - I_1 = \int_{t_1}^{T_s} -\frac{V_2 + (R_{ds} + R_L) i_L(t)}{L} dt. \tag{12}$$

For boost converter, it is

$$I_0 - I_1 = \int_{t_1}^{T_s} -\frac{V_2 - V_1 + (R_{ds} + R_L) i_L(t)}{L} dt. \tag{13}$$

Based on (8), (12) and (13) can be simplified to (14) and (15), respectively

$$I_1 \left[1 - \frac{(R_{ds} + R_L)T_s}{2\,L}(1 - d)\right] = I_0 \left[1 + \frac{(R_{ds} + R_L)T_s}{2\,L}(1 - d)\right] + \frac{V_2 T_s}{L}(1 - d) \tag{14}$$

$$I_1 \left[1 - \frac{(R_{ds} + R_L)T_s}{2\,L}(1 - d)\right] = I_0 \left[1 + \frac{(R_{ds} + R_L)T_s}{2\,L}(1 - d)\right] + \frac{(V_2 - V_1)T_s}{L}(1 - d). \tag{15}$$

With the same definition of k given in (11), (14) and (15) can be reexpressed with the same form as follows:

$$I_1[1 - k(1 - d)] = I_0[1 + k(1 - d)] + q(1 - d). \tag{16}$$

In (16), for both buck and buck–boost converters, $q = \frac{V_2 T_s}{L}$ while for boost converter, $q = \frac{(V_2 - V_1)T_s}{L}$.

3) Analytical Solutions: If k is 0, i.e., $R_{ds} + R_L = 0$, (11) and (16) degenerate to the formulas in ideal cases, otherwise, combining (11) and (16) yields

$$\begin{cases} I_0 = \frac{md[1 - k(1 - d)]}{2\,k} - \frac{q(1 + kd)(1 - d)}{2\,k}. \\ I_1 = \frac{(1 - kd)I_0}{1 + kd} + \frac{md}{1 + kd}. \end{cases} \tag{17}$$

Based on (17), one can simply get

$$\frac{I_0 + I_1}{2} = \frac{(m + q)d - q}{2\,k}. \tag{18}$$

For buck converter, the output current is

$$I_{\text{out}} = \frac{I_0 + I_1}{2}. \tag{19}$$

For both boost and buck–boost converters, the output current is

$$I_{\text{out}} = \frac{I_0 + I_1}{2}(1 - d). \tag{20}$$

As it can be seen from (19) and (20), in order to transfer power from input side to output side, the sum of I_0 and I_1 should be larger than zero, i.e., $I_0 + I_1 > 0$. If $I_0 < 0$ and is selected as a value that can guarantee ZVS turn-ON of S_1, then the ZVS turn-ON of S_2 is also guaranteed automatically since the absolute value of I_1 is always larger than I_0, meanwhile the required net voltage change values across the switches in one arm are the same.

Combining (18) and (19) yields the modified duty cycle expression for buck converter, which is

$$d_{\text{new}} = \frac{q}{m + q} + \frac{2I_{\text{out}}}{m + q} k. \tag{21}$$

Combing (18) and (20) yields the modified duty cycle expression for both boost and buck–boost converters, which is

$$d_{\text{new}} = \frac{q}{m + q} + \frac{m - \sqrt{m^2 - 8k(m + q)I_{\text{out}}}}{2(m + q)}. \tag{22}$$

TABLE II
SUMMARY OF NEW MODIFIED DUTY CYCLE EXPRESSIONS

Converter type	New modified duty cycle	Expression of k	Expression of m	Expression of q
Buck converter	$d=\frac{q}{m+q}+\frac{2I_{\text{out}}}{m+q}k$	$k=\frac{(R_{ds}+R_L)T_s}{2L}$	$m=\frac{(V_1-V_2)T_s}{L}$	$q=\frac{V_2T_s}{L}$
Boost converter	$d=\frac{q}{m+q}+\frac{m-\sqrt{m^2-8k(m+q)I_{\text{out}}}}{2(m+q)}$	$k=\frac{(R_{ds}+R_L)T_s}{2L}$	$m=\frac{V_1T_s}{L}$	$q=\frac{(V_2-V_1)T_s}{L}$
Buck–boost converter	$d=\frac{q}{m+q}+\frac{m-\sqrt{m^2-8k(m+q)I_{\text{out}}}}{2(m+q)}$	$k=\frac{(R_{ds}+R_L)T_s}{2L}$	$m=\frac{V_1T_s}{L}$	$q=\frac{V_2T_s}{L}$

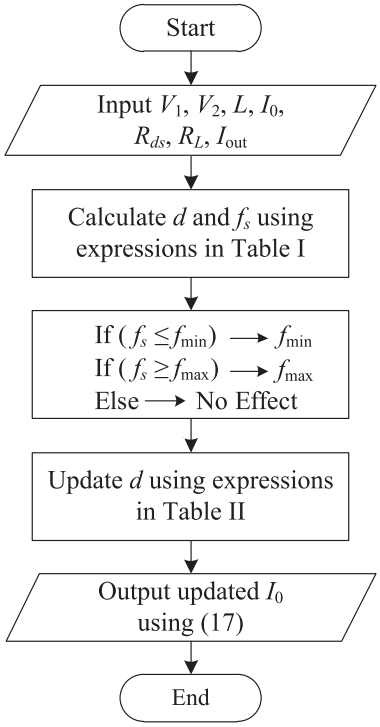


Fig. 5. Flowchart of I_0 calculation considering parasitic resistances.

With adoption of first-order Taylor expansion, (22) can further be simplified to

$$d_{\text{new}}=\frac{q}{m+q}+\frac{2I_{\text{out}}}{m}k. \tag{23}$$

When the parasitic resistances reduce to zero in ideal case, (21) and (22) [or (23)] can further be simplified to

$$d_{\text{ideal}}=\frac{q}{m+q}. \tag{24}$$

Equation (24) can be verified by the definition of m and q given in (11) and (16).

To summarize, the analytical solutions of the new modified duty cycle for the three dc–dc converters are presented in Table II. Once the duty cycle is known, then the switched current of I_0 can also be calculated based on (17). Fig. 5 briefly illustrates the calculation procedures of I_0 with the proposed analysis. The estimation of the parasitic resistances will be discussed in detail in Section IV-C.

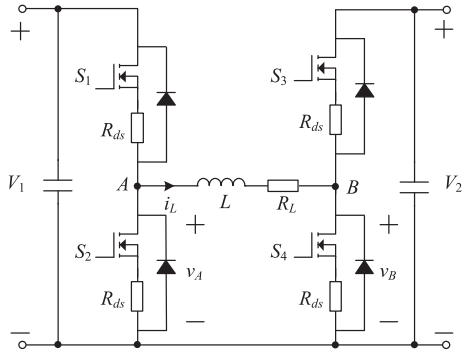


Fig. 6. Circuit topology of FSBB converter.

B. Application in an FSBB Converter

TCM–ZVS modulation can also be applied to an FSBB converter featuring multimode operation capability [14], [16], [17], and its circuit topology is shown in Fig. 6.

In order to apply the formulas derived in Table II to FSBB converter, simply, only the definition of k needs to be replaced by $k=\frac{(2R_{ds}+R_L)T_s}{2L}$. Taking TCM–ZVS buck mode operation as an example, in buck operation mode, S_3 is always ON, so, an additional R_{ds} is required to be counted. For boost operation mode, the R_{ds} of S_1 is required. It should be noted that under TCM–ZVS buck–boost mode operation, the output of the FSBB converter is not inverted compared with the single-switch buck–boost converter, but the operating principle is the same.

IV. Design Consideration and Simulation Verification

A. Switching Frequency and Inductance Parameters Selection

In practice, a frequency limiter is normally adopted to prevent the switching frequency from being too high or too low (cf., Fig. 3). In this article, the switching frequency is selected between 20 and 150 kHz. The minimum frequency is selected based on the frequency hearing range of human ear (less than

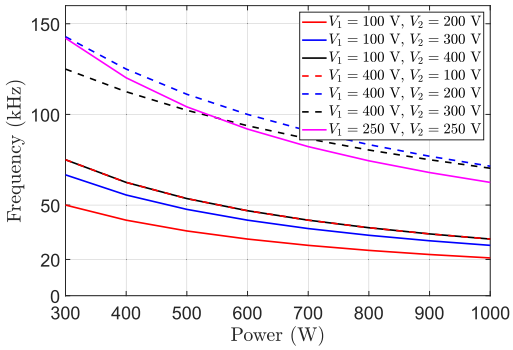


Fig. 7. Switching frequency under different operating conditions, $L = 100\ \mu$H, $I_0 = -2$ A.

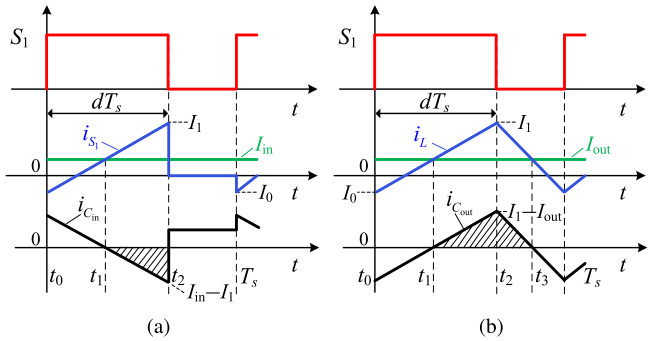


Fig. 8. Current waveforms of $i_{C_{\rm in}}$ and $i_{C_{\rm out}}$ of a buck converter under TCM–ZVS modulation. (a) $i_{C_{\rm in}}$. (b) $i_{C_{\rm out}}$.

20 kHz) while the maximum frequency is constrained by both the gate driver's driving capability and operating conditions.

For the inductance, a value of 100 μH was chosen to ensure that the switching frequency falls within the desired operational range. The calculated switching frequency is shown in Fig. 7 with the given operating specifications in this article.

B. Selection of Input and Output Capacitors

During the analysis in Section III, the input and output voltage are taken as a dc value. However, voltage ripple is always present and its value depends on the capacitance, so, the capacitance selection is important. In addition, the selection guideline of the input and output capacitors for a dc–dc converter under TCM–ZVS operation is often neglected. Herein, the capacitor voltage ripple is calculated as a selection basis for the capacitors in buck, boost, and buck–boost converters, respectively. The reference direction of the current is shown in Fig. 1. Different from traditional CCM operation when I_0 is larger than zero, in TCM–ZVS operation, since I_0 is negative while $I_{\rm in}$ and $I_{\rm out}$ (cf., Fig. 1) are positive, the ripple analysis of capacitor voltage is actually simpler in TCM–ZVS operations.

1) Case of Buck Converter: The waveforms of current flowing into the input and output capacitors are shown in Fig. 8.

The peak-to-peak value of the capacitor voltage ripple can be calculated based on the net change of charge in the shaded area. For the case of Fig. 8(a), the input capacitor peak-to-peak voltage ripple is

$$\Delta V_{\rm pp\_}C_{\rm in\_Buck} = \frac{(I_1 - I_{\rm in})(t_2 - t_1)}{2C_{\rm in}}, \tag{25}$$

where $t_2 - t_1 = \dfrac{I_1 - I_{\rm in}}{I_1 - I_0} dT_s$, $I_{\rm in}$ is the average input current.

For the case of Fig. 8(b), the output capacitor peak-to-peak voltage ripple is

$$\Delta V_{\rm pp\_}C_{\rm out\_Buck} = \frac{(I_1 - I_{\rm out})(t_3 - t_1)}{2C_{\rm out}}, \tag{26}$$

where $t_3 - t_1 = \dfrac{I_1 - I_{\rm out}}{I_1 - I_0} T_s$, $I_{\rm out}$ is the average output current.

2) Case of Boost Converter: The waveforms of current flowing into the input and output capacitors are shown in Fig. 9.

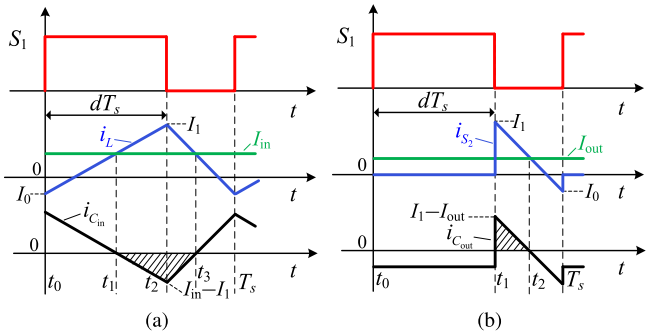


Fig. 9. Current waveforms of $i_{C_{\rm in}}$ and $i_{C_{\rm out}}$ of a boost converter under TCM–ZVS modulation. (a) $i_{C_{\rm in}}$. (b) $i_{C_{\rm out}}$.

For the case of Fig. 9(a), the input capacitor peak-to-peak voltage ripple is

$$\Delta V_{\rm pp\_}C_{\rm in\_Boost} = \frac{(I_1 - I_{\rm in})(t_3 - t_1)}{2C_{\rm in}}, \tag{27}$$

where $t_3 - t_1 = \dfrac{I_1 - I_{\rm in}}{I_1 - I_0} T_s$.

For the case of Fig. 9(b), the output capacitor peak-to-peak voltage ripple is

$$\Delta V_{\rm pp\_}C_{\rm out\_Boost} = \frac{(I_1 - I_{\rm out})(t_2 - t_1)}{2C_{\rm out}}, \tag{28}$$

where $t_2 - t_1 = \dfrac{I_1 - I_{\rm out}}{I_1 - I_0}(1 - d)T_s$.

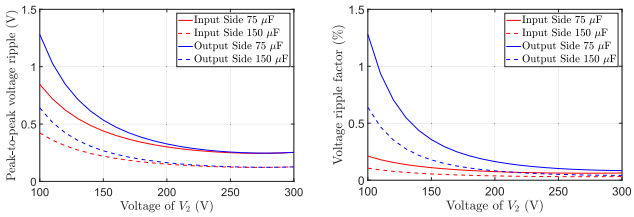
3) Case of Buck–Boost Converter: For a buck–boost converter given in Fig. 1(c), the current waveform flowing into the input capacitor can be illustrated by Fig. 8(a) while the current waveform flowing into the output capacitor can be illustrated by Fig. 9(b). Therefore, the peak-to-peak voltage ripple of the input and output capacitors can be expressed by (25) and (28), respectively.

Equations (25)–(28) can further be simplified, which are summarized in Table III. It can be concluded from Table III that for variable-frequency modulation, the input and output side voltage ripple are independent of the frequency if it is not limited.

Figs. 10 and 11 show the peak-to-peak voltage ripple and its ripple factor for both TCM–ZVS buck and boost operations with different capacitances. The voltage ripple factor is defined

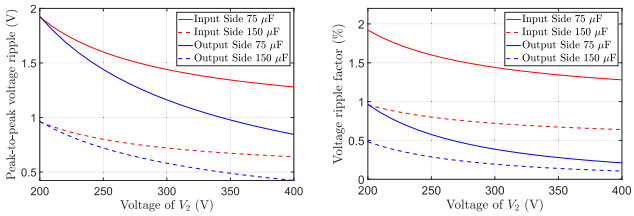
TABLE III
SUMMARY OF PEAK-TO-PEAK VOLTAGE RIPPLE OF INPUT AND OUTPUT CAPACITORS

Converter type	V_{pp} of C_{in}	V_{pp} of C_{out}
Buck converter	$\frac{L}{2C_{\text{in}}}\frac{(I_1-I_{\text{in}})^2}{V_1-V_2}$	$\frac{L}{2C_{\text{out}}}\frac{V_1(I_1-I_{\text{out}})^2}{V_2(V_1-V_2)}$
Boost converter	$\frac{L}{2C_{\text{in}}}\frac{V_2(I_1-I_{\text{in}})^2}{V_1(V_2-V_1)}$	$\frac{L}{2C_{\text{out}}}\frac{(I_1-I_{\text{out}})^2}{V_2-V_1}$
Buck – Boost converter	$\frac{L}{2C_{\text{in}}}\frac{(I_1-I_{\text{in}})^2}{V_1}$	$\frac{L}{2C_{\text{out}}}\frac{(I_1-I_{\text{out}})^2}{V_2}$



(a) (b)

Fig. 10. Peak-to-peak voltage ripple and its ripple factor under buck operation with 75 and 150 μF capacitance, $P_o = 1$ kW, $I_0 = -2$ A, and $V_1 = 400$ V. (a) Peak-to-peak voltage ripple. (b) Peak-to-peak voltage ripple factor.



(a) (b)

Fig. 11. Peak-to-peak voltage ripple and its ripple factor under boost operation with 75 and 150 μF capacitance, $P_o = 1$ kW, $I_0 = -2$ A, and $V_1 = 100$ V. (a) Peak-to-peak voltage ripple. (b) Peak-to-peak voltage ripple factor.

TABLE IV
KEY PARAMETERS OF THE FSBB PROTOTYPE

MOSFET Switch	C3M0075120J (2 in Parallel)
Input capacitor C_{in}	Vishay, 25 μF × 6
Output capacitor C_{out}	Vishay, 25 μF × 6
Inductor	PM 74/59, N87, 100 μH
Switching frequency	20–150 kHz

as $\gamma = \frac{\Delta V_{pp}}{V_{dc}}$ with V_{dc} being its dc value. In this article, both the input and output capacitances were chosen to be 150 μF.

C. Parasitic Resistances Estimation and Simulation Verification of the Proposed Analysis

With the control logic in Fig. 3 and the derived formulas in Table II and (17), the reverse switched current of I_0 can be calculated. In order to verify the correctness of the formulas, a set of simulation was carried out with the specifications in Table IV based on the laboratory prototype.

1) Estimation of Parasitic Resistances: Before simulation verification, the parasitic resistance needs to be estimated. The value of R_{ds} can be acquired from its datasheet while for the value of R_L, its equivalent value can be estimated by the energy-conservation approach (29) [18], [19], [20]

$$R_L = \frac{P_{\text{Loss\_}L}}{I^2_{\text{rms\_}L}}, \tag{29}$$

where $P_{\text{Loss\_}L}$ is the inductor loss, which consists of winding loss and core loss, $I_{\text{rms\_}L}$ is the rms value of the inductor current, which is

$$I_{\text{rms\_}L} = \sqrt{\frac{1}{3}(I_0^2 + I_1^2 + I_0 I_1)}. \tag{30}$$

To build the inductor, 600×0.071 mm Litz wire was adopted. The skin depth of $\delta_{C_{\text{u}}}$ at a certain switching frequency can be calculated through $\delta_{C_{\text{u}}} = \sqrt{\frac{2}{\omega \mu_{C_{\text{u}}} \sigma_{C_{\text{u}}}}}$ with $\omega, \mu_{C_{\text{u}}}, \sigma_{C_{\text{u}}}$ being its angular frequency, permeability, and electrical conductivity, respectively [21]. Therefore, at 25 °C with frequencies of 20 kHz and 150 kHz, the skin depth is calculated as 0.47 and 0.17 mm, respectively, which is much larger than the wire diameter. To facilitate the winding loss calculation, its dc resistance is adopted. The number of winding turns is 18, and its measured R_{dc} is 18 mΩ.

As for the core loss, due to the nonsinusoidal inductor current waveform, the improved generalized Steinmetz equation (iGSE) [22] is adopted, which is expressed as

$$P_{\text{core\_iGSE}} = \frac{1}{T_s}\int_0^{T_s} k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} V_e dt \tag{31}$$

$$k_i = \frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)}, \tag{32}$$

where k, α, and β are the Steinmetz coefficients, ΔB is the peak-to-peak flux density, V_e is the core volume and k_i can be calculated from (32) [22].

With TCM-ZVS operation, (31) can be simplified to the same expression for buck, boost, and buck–boost converters, which is

$$P_{\text{core\_iGSE}} = k_i f_s^{\alpha} (\Delta B)^{\beta} [d^{1-\alpha} + (1-d)^{1-\alpha}] V_e. \tag{33}$$

Therefore, combining (29)–(33) yields the estimation of R_L, which is

$$R_L = R_{\text{dc}} + \frac{k_i f_s^{\alpha} (\Delta B)^{\beta} [d^{1-\alpha} + (1-d)^{1-\alpha}] V_e}{\frac{1}{3}(I_0^2 + I_1^2 + I_0 I_1)}. \tag{34}$$

For the inductor design, PM 74/59 core with N87 material was adopted, the Steinmetz parameters are derived by curve fitting as $k = 47.69$, $\alpha = 1.11$, $\beta = 2.07$ at 25 °C with SI unit [23]. However, this estimation has a drawback since the core losses of ferrite material depend on dc bias [24] and also cross-sectional area [25], which is not modeled. Nevertheless, this estimation can still be used as a reference.

Fig. 12 shows the estimation of R_L under different operating conditions. Considering the MOSFETs of C3M0075120J (two in parallel) adopted in this article, a total parasitic resistance around several hundred milliohms could be utilized for simulation verification.

2) Simulation Verification: Simulation results from PLECS circuit simulator are provided for buck, boost, and buck–boost mode operations, respectively. Variable-step nonstiff solver with

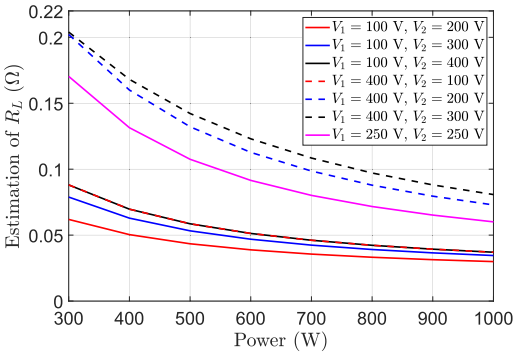


Fig. 12. Estimation of R_L under different operating points.

TABLE V
TCM–ZVS BUCK MODE OPERATION, $V_1 = 400$ V, $V_2 = 100$ V, $L = 100$ μH, $I_0 = -2$ A, $d_{\text{IDEAL}} = 0.25$, AND $R_{\text{PARASITIC}} = 0.6$ Ω.

Output power (W)	300	500	700	1000
Frequency (kHz)	75.00	53.57	41.67	31.25
Output voltage under ideal duty cycle (V)	98.2	97.0	95.8	94.0
Modified duty cycle	0.2545	0.2575	0.2605	0.2650
Output voltage under modified duty cycle (V)	100.0	100.0	100.0	100.0

TABLE VI
TCM-ZVS BOOST MODE OPERATION, $V_1 = 100$ V, $V_2 = 200$ V, $L = 100$ μH, $I_0 = -2$ A, $d_{\text{IDEAL}} = 0.5$, AND $R_{\text{PARASITIC}} = 0.6$ Ω.

Output power (W)	300	500	700	1000
Frequency (kHz)	50.00	35.71	27.78	20.83
Output voltage under ideal duty cycle (V)	196.3	193.8	191.3	187.5
Modified duty cycle	0.5092	0.5155	0.5220	0.5321
Output voltage under modified duty cycle (V)	199.9	199.8	199.7	199.5

TABLE VII
TCM-ZVS BUCK-BOOST MODE OPERATION, $V_1 = 250$ V, $V_2 = 250$ V, $L = 100$ μH, $I_0 = -2$ A, $d_{\text{IDEAL}} = 0.5$, AND $R_{\text{PARASITIC}} = 0.6$ Ω.

Output power (W)	300	500	700	1000
Frequency (kHz)	142.05	104.17	82.24	62.50
Output voltage under ideal duty cycle (V)	247.1	245.2	243.2	240.3
Modified duty cycle	0.5029	0.5049	0.5068	0.5098
Output voltage under modified duty cycle (V)	250.0	250.0	249.9	249.9

maximum step size of 1e-9 s (i.e., 1 ns) and 1e-4 relative tolerance is used.

First, the modified duty cycle expressions were verified based on the output voltage with a total 0.6 Ω parasitic resistance as an example. Both the input and output capacitors are 150 μF. In order to be consistent with the assumptions of theoretical analysis, the gating signals are fully complementary, which means no dead time is applied.

The results are summarized in Tables V–VII, as it can be seen, after applying the modified duty cycle values, the output voltage can reach the expected value, which proves the correctness of the proposed duty cycle formulas.

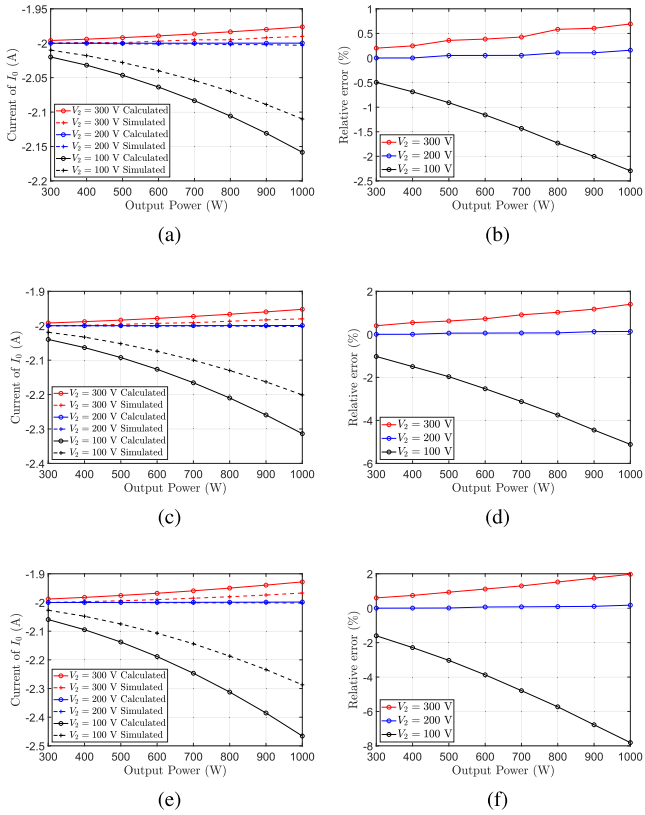


Fig. 13. Calculated and simulated switched current of I_0 and its relative error when $V_1 = 400$ V with different parasitic resistances of 0.2, 0.4, and 0.6 Ω, respectively. (a) I_0 at 0.2 Ω. (b) Relative error at 0.2 Ω. (c) I_0 at 0.4 Ω. (d) Relative error at 0.4 Ω. (e) I_0 at 0.6 Ω. (f) Relative error at 0.6 Ω.

Second, the simulated and calculated switched current of I_0 under 0.2, 0.4, and 0.6 Ω cases are given, which are shown from Figs. 13 to 15. The relative error is defined as $\varepsilon = \frac{\text{Calculated Value} - \text{Simulated Value}}{|\text{Simulated Value}|}$.

It can be seen from Figs. 13 to 15 that under a wide operational power range with different parasitic resistances, the simulated and calculated current values of I_0 could match well for buck and buck-boost mode operations while for boost mode operation, the difference is slightly larger. Both calculated and simulated values follow the same trend as the power changes. The cause of the difference between the calculated and simulated values is discussed in Section IV-D.

3) Estimation of I_0 Under Different Operating Cases: It can be concluded that in order to predict the reverse switched current well, accurate determination of the parasitic resistance is required, which is normally difficult in practice. Considering the adoption of C3M0075120J MOSFET and external resistor board as a comparison during the experimentation (cf., Fig. 25), herein, additional 0.1 and 0.2 Ω were added to the value given in Fig. 12 to represent the total parasitic resistance. Fig. 16 shows the estimation of I_0 under different operational cases, and its value is supposed to be -2 A in ideal condition.

From the results in Fig. 16, it can be inferred that the ZVS turn-ON is more likely to be lost when the converter is operating

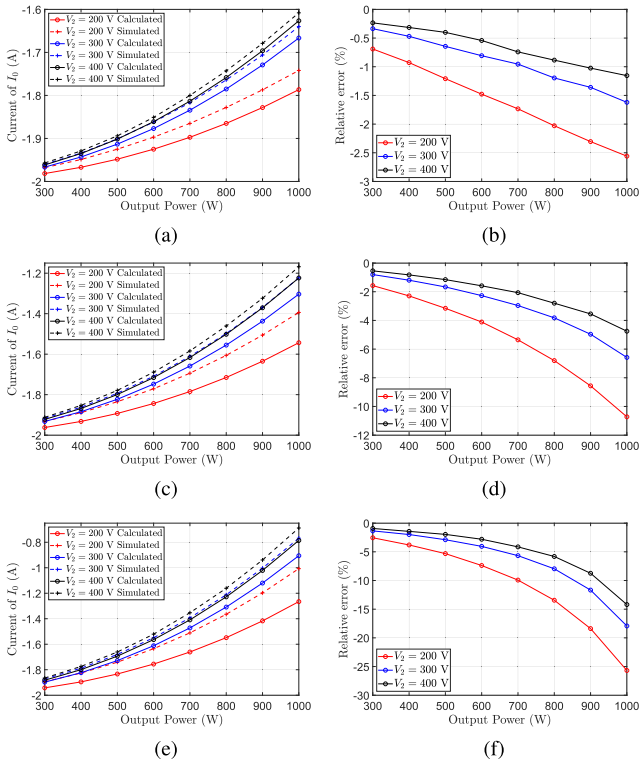


Fig. 14. Calculated and simulated switched current of I_0 and its relative error when $V_1 = 100$ V with different parasitic resistances of 0.2, 0.4, and 0.6 Ω, respectively. (a) I_0 at 0.2 Ω. (b) Relative error at 0.2 Ω. (c) I_0 at 0.4 Ω. (d) Relative error at 0.4 Ω. (e) I_0 at 0.6 Ω. (f) Relative error at 0.6 Ω.

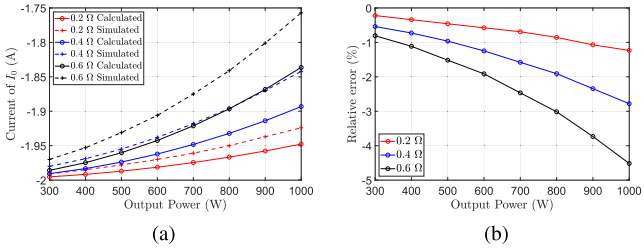


Fig. 15. Calculated and simulated switched current of I_0 and its relative error when $V_1 = V_2 = 250$ V with different parasitic resistances of 0.2, 0.4, and 0.6 Ω, respectively. (a) Value of I_0. (b) Relative error.

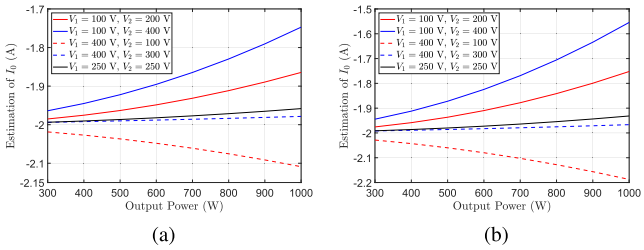


Fig. 16. Estimation of I_0 under different operating cases with two parasitic resistances. The total parasitic resistance is the sum of 0.1 or 0.2 Ω and the value in Fig. 12. I_0 is supposed to be −2 A in ideal condition. (a) I_0 with 0.1 Ω added to Fig. 12. (b) I_0 with 0.2 Ω added to Fig. 12.

TABLE VIII
MEASURED INDUCTANCE

f_s (kHz)	10	20	60	100	150	200	250
L (μH)	101.1	101.0	101.0	101.1	101.1	101.1	101.2

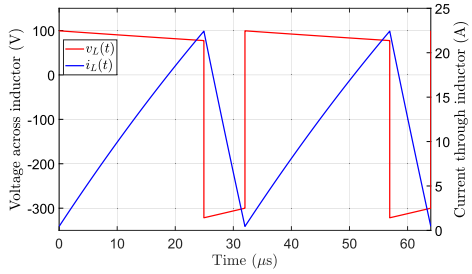


Fig. 17. Simulation example of inductor current and voltage, $V_1 = 100$ V, $V_2 = 400$ V, $f_s = 31.25$ kHz, $P_o = 1$ kW, $L = 100$ μH, and parasitic resistance is 1 Ω.

in boost mode with the operating specifications adopted in this article, which will be verified by the experimental results.

D. Discussion on Assumptions

First, during the analysis, the inductance is assumed to be a constant, which can be evidenced by the maximum possible flux density during converter operation. Its value can be calculated by

$$\hat{B} = \frac{L\hat{I}}{NA_e}. \tag{35}$$

Substituting corresponding values, i.e., $L = 100$ μH, $N = 18$, and $A_e = 790$ mm^2, the maximum dc bias flux density is calculated to be 70.3 mT, and the maximum flux density is 154.7 mT, and these values are much less than the N87 material saturation flux density of 490 mT at 25 °C or 390 mT at 100 °C [23]. Therefore, it is reasonable to assume the inductance to be a constant under dc current bias. As for the influence of variable frequency on the inductance, the inductor was measured within a wide frequency range between 10 and 250 kHz given in Table VIII in Section V. As it can be seen, the inductance maintains a constant during a wide frequency range.

Second, it is assumed that the inductor current line is linear, which might not be valid under high power case with a large parasitic resistance. For example, Fig. 17 shows the inductor voltage and current waveforms when the parasitic resistance is intentionally selected at 1 Ω. As it can be seen, the inductor current is not strictly linear, which introduces the difference between the calculated and simulated results. A larger resistance and a larger current will lead to a larger difference between these two values, which also explains the results shown in Figs. 13–15.

Third, different from the case of reverse parallel current conduction described in [26], it is assumed that during reverse conduction, the current only passes through the MOSFET channel, which is due to the larger forward voltage drop of the SiC MOSFET body diode compared with its Si counterparts. For example, the minimum initial conduction voltage drop of the body diode of

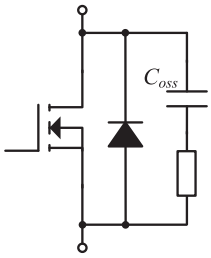


Fig. 18. MOSFET model including parasitic capacitance of C_{oss}.

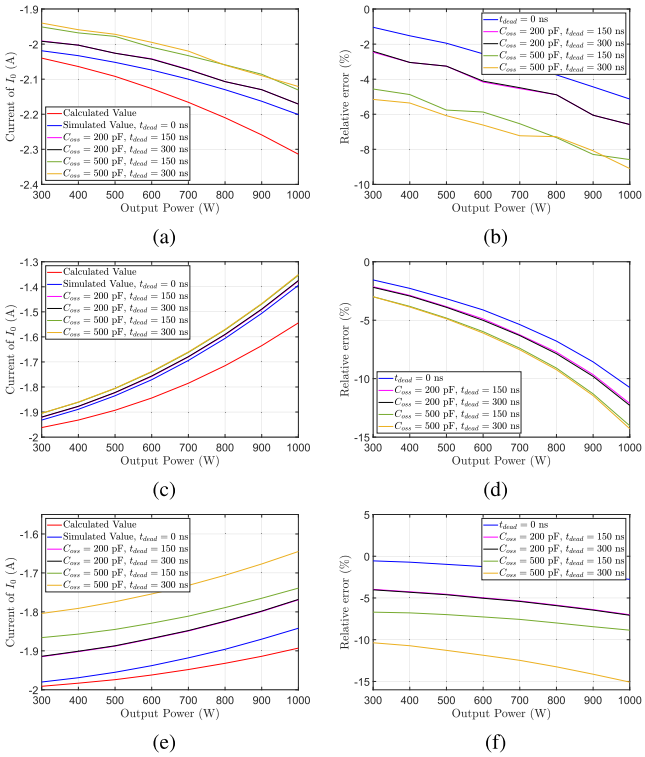


Fig. 19. Calculated and simulated values of I_0 and its relative error with different parasitic capacitance and dead time values using a more practical MOSFET model. (a) Buck operation case, $V_1 = 400$ V, and $V_2 = 100$ V. (b) Relative error under buck operation. (c) Boost operation case, $V_1 = 100$ V, and $V_2 = 200$ V. (d) Relative error under boost operation. (e) Buck–boost operation case, $V_1 = V_2 = 250$ V. (f) Relative error under buck–boost operation.

C3M0075120J is around 2.2 V, considering its typical 75 mΩ channel resistance, the current shunting phenomenon of the body diode will only occur when the reverse conduction current is larger than 29.3 A. In this work, two MOSFETs are in parallel, and the peak current is around 22 A, so, this assumption is valid.

Finally, during the proposed analysis, the dead time and its corresponding circuit resonant behaviour during this period is not considered, which might introduce extra error. Due to complexity of the circuit behavior, simulation was carried out in PLECS circuit simulator to study the influence from the dead time with a more practical modeling of the MOSFET shown in Fig. 18. It should be noted that a small resistor was connected in series with the parasitic capacitance to avoid simulation errors, and this value is selected to be 1e-4 Ω. The detailed parameters

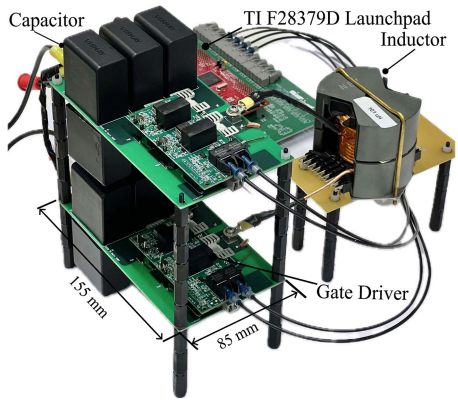


Fig. 20. Laboratory prototype of an FSBB converter featuring TCM–ZVS buck, boost, and buck–boost operating modes.

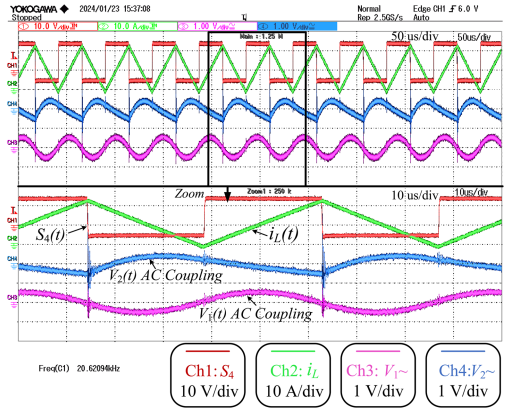
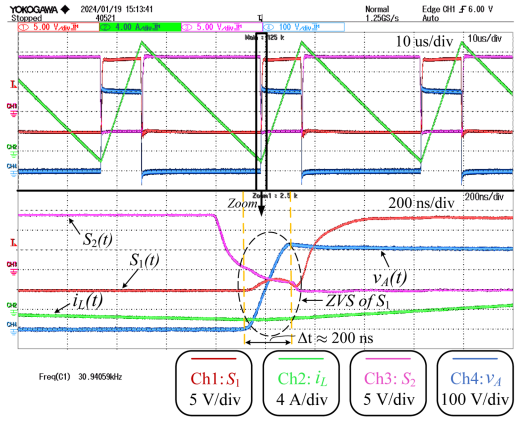


Fig. 21. Voltage ripple under boost operation, $V_1 = 100$ V, $V_2 = 200$ V, and $P_o = 1$ kW. $S_4(t)$ is the gate-to-source voltage of S_4.

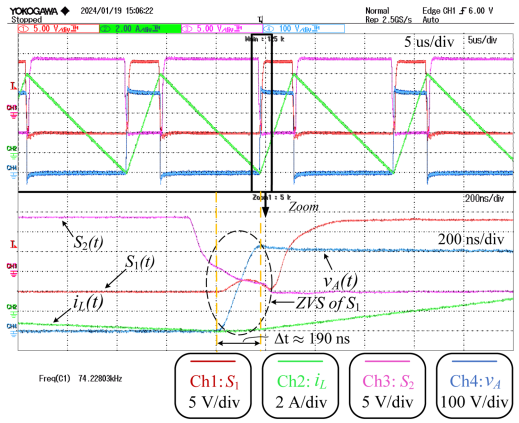
were selected as follows: the parasitic capacitance (C_{oss}) is 200 and 500 pF; the dead time (t_{dead}) is 150 and 300 ns. The MOSFET channel resistance (R_{ds}) is 50 mΩ while the inductor resistance (R_L) is 350 mΩ. As for the body diode, its forward voltage is 2.2 V and its on resistance is 0.18 Ω. The frequency is calculated through the formulas in Table I while the duty cycle is fine tuned with a 0.05% duty cycle step to meet the expected output voltage. Variable-step stiff solver is adopted with a maximum step size of 1e-9 s (i.e., 1 ns) and 1e-4 relative tolerance. The simulated results of the valley current (I_0) are shown in Fig. 19, and the definition of relative error was given in Section IV-C. It can be seen that the larger the C_{oss} and dead time, the larger the error between the calculated and simulated results. The maximum error can reach 15% in the given example. Therefore, the circuit resonant behavior during the dead time could be considered to improve the proposed analysis.

V. Experimental Verification

A laboratory prototype of FSBB converter was built for the experiment, which can be operated in TCM–ZVS buck, boost, and buck–boost modes. The converter prototype is shown in Fig. 20.

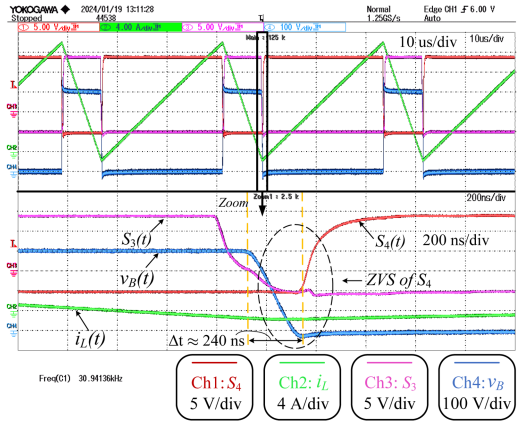


(a)

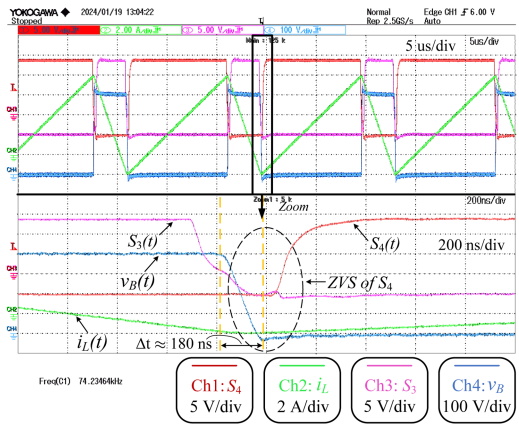


(b)

Fig. 22. TCM–ZVS buck operation, $V_1 = 400$ V, $V_2 = 100$ V. $S_1(t)$ is the gate-to-source voltage of S_1, $S_2(t)$ is the gate-to-source voltage of S_2, $v_A(t)$ is the voltage across switch S_2 shown in Fig. 6. (a) $P_o = 1$ kW. (b) $P_o = 300$ W.



(a)



(b)

Fig. 23. TCM–ZVS boost operation, $V_1 = 100$ V, $V_2 = 400$ V. $S_3(t)$ is the gate-to-source voltage of S_3, $v_B(t)$ is the voltage across switch S_4 shown in Fig. 6. (a) $P_o = 1$ kW. (b) $P_o = 300$ W.

The experiment was carried out in three cases, i.e., buck, boost, and buck–boost operating modes. For buck operation case, the input voltage is 400 V, while in the boost operation case, the input voltage is 100 V. For buck–boost operation case, both the input and output voltages are 250 V. The output power varies between 300 W and 1 kW. The switched ZVS current of I_0 is selected as -2 A for the experiment. The dead time defined by the two gate-to-source voltage signals crossing zero volt was around 230 ns. The measured inductance value is given in Table VIII, which is around 101 μH by Keysight E4990A impedance analyzer. The SiC MOSFET channel resistance (two in parallel) was also measured, and its values are given in Appendix A.

Keysight current probe N2782B featuring 50 MHz bandwidth, ± 10 mA amplitude accuracy, and maximum 30 Arms current rating was adopted to measure the inductor current. Before each set of measurements, the current probe is demagnetized to guarantee its measurement accuracy. Keysight N2791A differential voltage probe with 25 MHz bandwidth was adopted to measure the voltage signals.

A. Voltage Ripple Verification

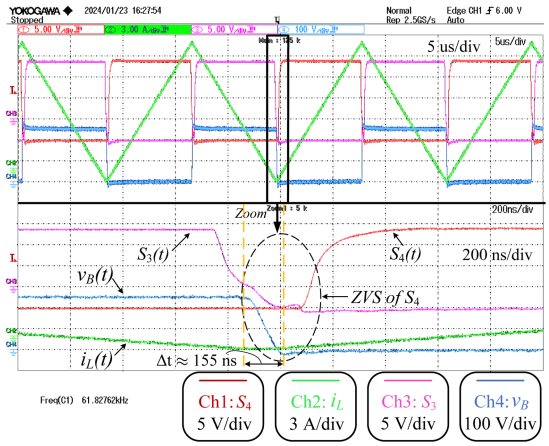
Fig. 21 shows the voltage ripple of the converter under boost mode operation when $V_1 = 100$ V, $V_2 = 200$ V, and $P_o = 1$ kW. As it can be seen, the peak-to-peak voltage ripples of the input and output sides match the derived formulas in Table III and the result shown in Fig. 11(a).

B. TCM–ZVS Operating Waveforms

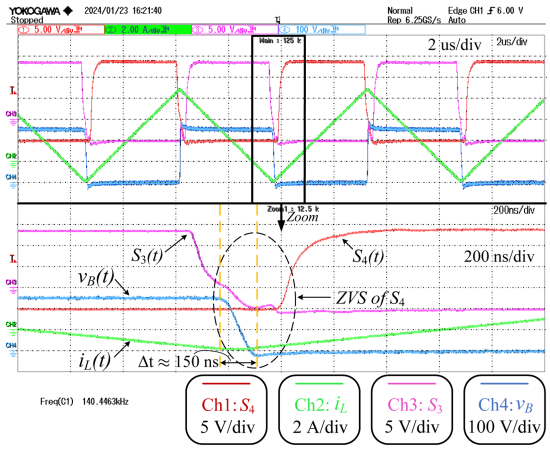
In order to show the parasitic resistance influence on the value of I_0, two sets of experiments were carried out with or without external 84 mΩ resistor.

Figs. 22–24 show the typical experimental results in buck, boost, and buck–boost mode operation cases under 300 W and 1 kW without external resistor, respectively.

By comparing the gate-to-source voltage of S_4 at the moment when v_B drops to zero (marked by the orange dashed line) or the time it takes for v_B to drop to zero (the time between the two orange dashed lines) in Fig. 23, it can be inferred that the absolute value of I_0 from 1 kW operation is smaller than the one in 300 W condition. However, this phenomenon is not obvious



(a)



(b)

Fig. 24. TCM–ZVS buck–boost operation, $V_1 = 250$ V, $V_2 = 250$ V. (a) $P_o = 1$ kW. (b) $P_o = 300$ W.

in Figs. 22 and 24 when the converter operates in buck and buck–boost modes, which is as expected from the description in Section IV-C.

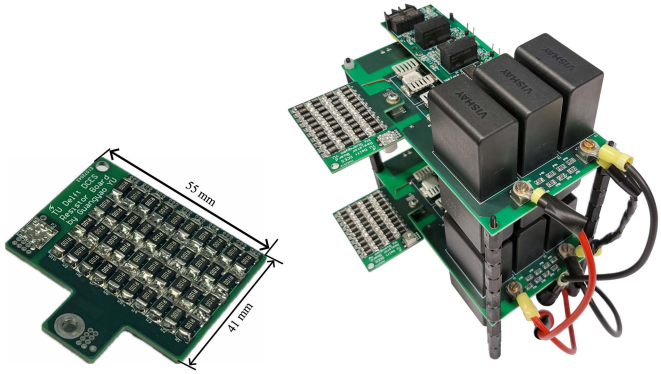
C. Measured Values of Reverse Switched Current

The external 84 mΩ resistor consists of two 42 mΩ resistor boards, which is inserted into the inductor path illustrated in Fig. 25.

Since the reverse switched current is more likely to deviate from the ideal value under high power condition, and therefore the measured waveforms at 1 kW output power are given in Fig. 26 as a comparison. By comparing the time between the two dashed orange lines, the absolute value of I_0 in Fig. 26(b) is much less than the one in Fig. 26(a).

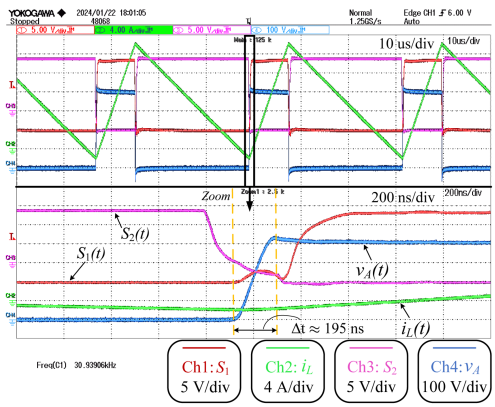
In order to show the measured results of I_0, each operating point was measured twice. The averaged value of I_0 are given in Fig. 27, and the length of the error bar represents the standard deviation σ of the measurement at that point, which is $\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \bar{x})^2}$, where x_i is the measured I_0 for each test, $\bar{x}$ is the averaged value, and N is the number of measurements. In particular, when $N = 2$, the standard deviation is $\sigma = \frac{1}{2}|x_1 - x_2|$. The deviation of I_0 from ideal value is also given, which is defined as deviation $= \frac{I_{0\_measured} - I_{0\_ideal}}{|I_{0\_ideal}|}$.

From the measured results, it can be seen that under TCM–ZVS boost mode operation, I_0 increases obviously when power

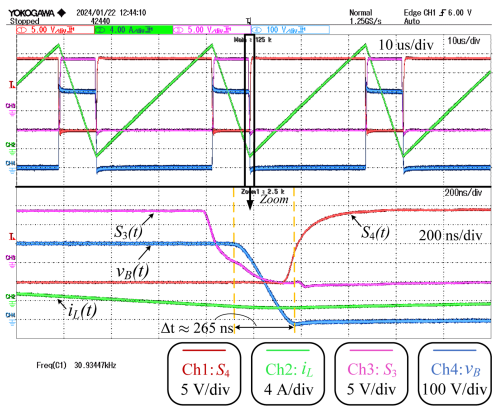


(a) (b)

Fig. 25. Resistor board and its insertion into the inductor path. (a) 42 mΩ external resistor board. Resistor type is CRA2512-FZ-R100ELF. (b) FSBB converter with external resistor.



(a)



(b)

Fig. 26. Measured waveforms with an external 84 mΩ resistor, $P_o = 1$ kW. (a) Buck operation, $V_1 = 400$ V, $V_2 = 100$ V. (b) Boost operation, $V_1 = 100$ V, $V_2 = 400$ V.

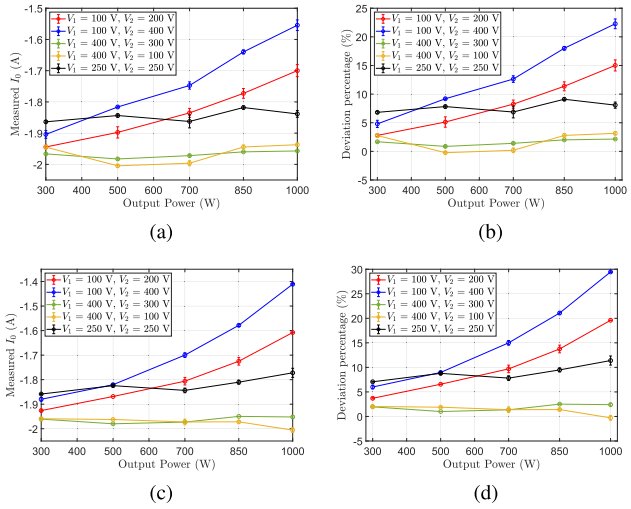


Fig. 27. Measured value of I_0 and its deviation from the ideal value at different operating points with and without external 84 mΩ resistor. (a) Measured I_0 without external resistor. (b) Deviation percentage of I_0 without external resistor. (c) Measured I_0 with external resistor. (d) Deviation percentage of I_0 with external resistor.

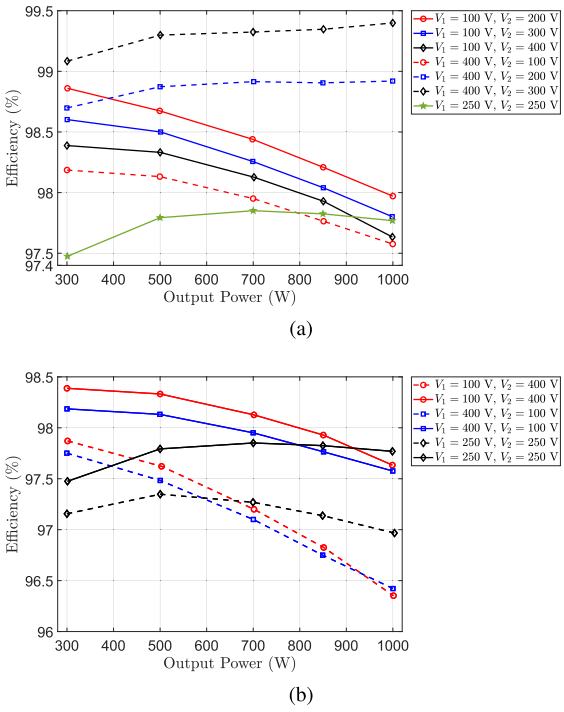


Fig. 28. Measured efficiency of FSBB converter at different operating points. (a) Measured efficiency without external resistor. (b) Efficiency comparison, dashed lines represent the values with an external 84 mΩ resistor while solid lines represent the values without external resistor.

increases, besides, when the parasitic resistance increases by adding an external resistor, this phenomenon is more obvious, which is as expected according to the analysis in Section IV. For TCM–ZVS buck operation, I_0 basically maintains at a constant value close to -2.0 A indicating that it is less susceptible to the parasitic resistance.

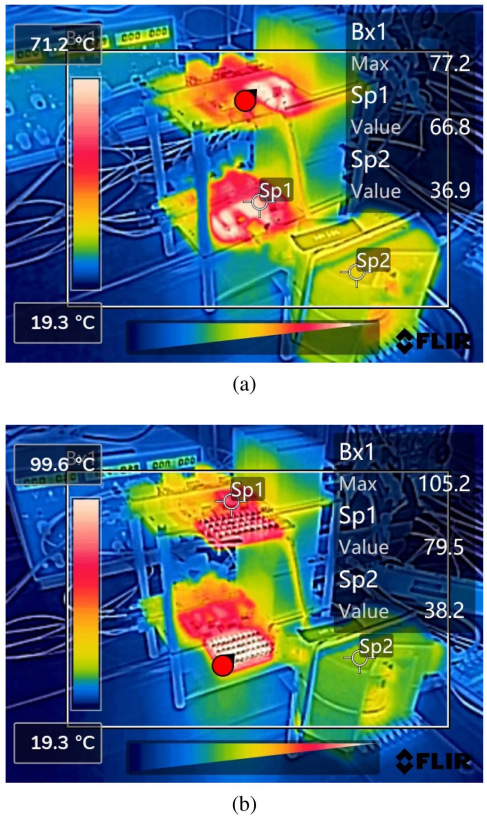


Fig. 29. Steady-state thermal image of the converter operating continuously at $V_1 = 100$ V, $V_2 = 200$ V, $f_s = 20.63$ kHz, and $P_o = 1$ kW after 40 min with an ambient temperature around 21 °C. (a) Thermal image without adding external resistor board, and measured efficiency is 97.9%. (b) Thermal image with external resistor board, and measured efficiency is 96.6%.

D. Efficiency and Thermal Performance

The efficiency performance of the FSBB converter is shown in Fig. 28 as a reference. It should be noted that the power losses from the auxiliary power supply for the gate drivers are not included. The efficiency was measured by Yokogawa WT500. The measured efficiency values in Fig. 28(a) are comparable to the mainstream efficiency of similar converters today [3], [9], [14], [16], [27]. Therefore, the measured results of the reverse switched current in Fig. 27 also provide valuable information for the TCM–ZVS modulation design based on current commercial SiC MOSFET.

Fig. 29 shows the steady-state thermal image of the prototype converter operating at $V_1 = 100$ V, $V_2 = 200$ V, $f_s = 20.63$ kHz, and $P_o = 1$ kW condition continuously after 40 min with an ambient temperature around 21 °C by Teledyne FLIR C5. Due to the possible reflection from the adopted 7106DG heatsink, black electrical tape was used to increase its emissivity according to [28]. The converter is natural cooled and the hottest spot from Fig. 29(a) is around 77.2 °C. In this case of the boost operation, S_1 is always ON and has the highest thermal stress among the four switches. The rms current through each (two in parallel) MOSFET is around 6.1 A, and the calculated conduction loss would be around 2.7 W. By further checking the thermal resistance

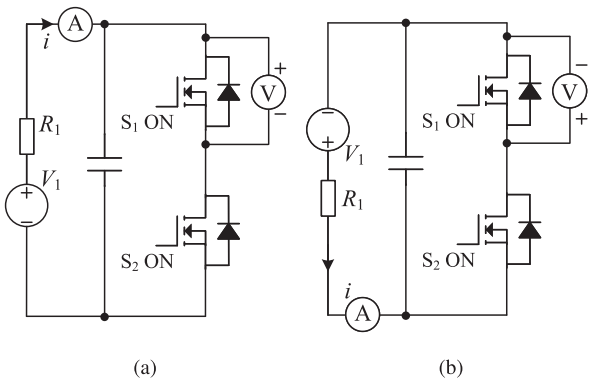


Fig. 30. Static MOSFET R_{ds} measurement circuit, taking S_1 as an example. (a) Forward conduction R_{ds} measurement. (b) Reverse conduction R_{ds} measurement.

TABLE IX
MEASURED RESULTS OF FORWARD AND REVERSE CONDUCTION CHANNEL VOLTAGES AND CURRENTS

Current (A)	1	3	5	7	9
V_{ds} of S_1 (mV)	35.47	107.04	180.20	256.99	335.62
V_{ds} of S_2 (mV)	38.28	115.33	194.69	279.90	361.63
V_{ds} of S_3 (mV)	36.62	110.74	186.32	265.36	346.60
V_{ds} of S_4 (mV)	34.37	103.77	174.93	248.80	324.00
V_{sd} of S_1 (mV)	35.44	106.11	176.89	248.92	327.89
V_{sd} of S_2 (mV)	37.49	112.35	187.75	265.67	345.90
V_{sd} of S_3 (mV)	36.49	109.20	182.09	256.14	333.00
V_{sd} of S_4 (mV)	34.30	102.76	171.65	242.30	314.90

(40 °C at 2 W) of the 7106DG heatsink, this temperature rise is reasonable.

VI. CONCLUSION

In this article, the reverse switched current required for TCM–ZVS modulation is revisited for buck, boost, and buck–boost converters considering the influence from the parasitic resistances with variable-frequency voltage-mode control. Universal and detailed closed-form equations of the new modified duty cycle and switched current are derived. The models show that the parasitic resistance could have a negative impact on the reverse switched current, which may lead to an unexpected loss of ZVS turn-ON. For the operating specifications adopted in this article, this phenomenon is more obvious in boost mode. An FSBB converter featuring multimode operation capability was built to verify the proposed analysis. The influence of the dead time combined with the parasitic resistance can be a future study to further improve the accuracy of the analytical model.

APPENDIX
STATIC MOSFET CHANNEL RESISTANCE MEASUREMENT

Fig. 30 shows the static MOSFET channel resistance measurement circuit.

In Fig. 30, R_1 functions as a current limiting resistor. Due to the extremely large insulation resistance of the dc link capacitor, the leakage current through this branch is negligible. The measured results are given in Table IX at a room temperature of 20 °C. S_1–S_4 correspond to the switches shown in Fig. 6.

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