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Over-the-Air Frequency Calibration for Crystal-Less BLE Nodes Achieving ±20 ppm Accuracy at -23 dB SIR

Amir Arsalan Kiavar, Niels Fakkel, Masoud Babaie
Delft University of Technology, the Netherlands
a.kiavar@tudelft.nl

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***Abstract*—Bluetooth Low Energy (BLE) powers large-scale Internet-of-Things networks but remains constrained by costly off-chip crystal oscillators. This work presents a 730 µW over-the-air frequency calibration technique that compares the energy of the upper and lower sidebands of a received BLE-compliant signal to calibrate the frequency accuracy of an on-chip LC oscillator from ±340 ppm to ±20 ppm within a 1.1 ms calibration period, while maintaining robust operation under a -23 dB signal-to-interference ratio at the adjacent channel.**

***Keywords*—Crystal-less, BLE, Energy-Detection Band-Pass Filter, Impedance-Transforming Quadrature Hybrid Coupler (IT-QHC).**

I. Introduction

Bluetooth Low Energy (BLE) has become the dominant standard for Internet of Things (IoT) applications, where large-scale deployments demand devices that are low-cost, energy-efficient, and virtually maintenance-free. The off-chip crystal oscillator remains a primary bottleneck in cost, size, and assembly complexity, motivating the adoption of integrated LC [1] and RC [2] oscillators as frequency references. However, such CMOS references exhibit insufficient frequency stability to comply with BLE's frequency accuracy specification.

This work assumes that a frequency accuracy of ±300 ppm is achievable using CMOS LC oscillators, as demonstrated in [1], and proposes an over-the-air (OTA) frequency calibration technique to reduce this error to ±20 ppm using existing BLE infrastructure. In this scheme, advertising devices such as smartphones retain precise crystal references, while dense networks of IoT scanning nodes employ low-cost on-chip oscillators and calibrate their frequency using received Gaussian frequency-shift keying (GFSK)-modulated BLE signals, as illustrated in Fig. 1. Each crystal-less node periodically activates a wake-up receiver (WuRX) to detect a predefined multidimensional wake-up signature (WuS) transmitted by the advertising device following a channel-hopping sequence. Upon WuS detection, an OTA-based frequency-locked loop (FLL) is triggered to reduce the local oscillator (LO) frequency error from ±340 ppm to BLE's ±20 ppm specification. The oscillator then operates in open-loop mode during BLE packet transmission or reception (0.4 ms to 2 ms) [3], as the frequency noise and drift of LC oscillators remain within BLE limits over this short duration.

II. System Architecture

Fig. 2 shows the simplified block diagram of the proposed system, supporting three modes: a back-channel WuRX for detecting advertising events, an OTA-FLL for frequency calibration, and a zero-IF receiver for data communication. An impedance-transforming quadrature hybrid coupler (IT-QHC) splits the received signal into I/Q paths for sideband

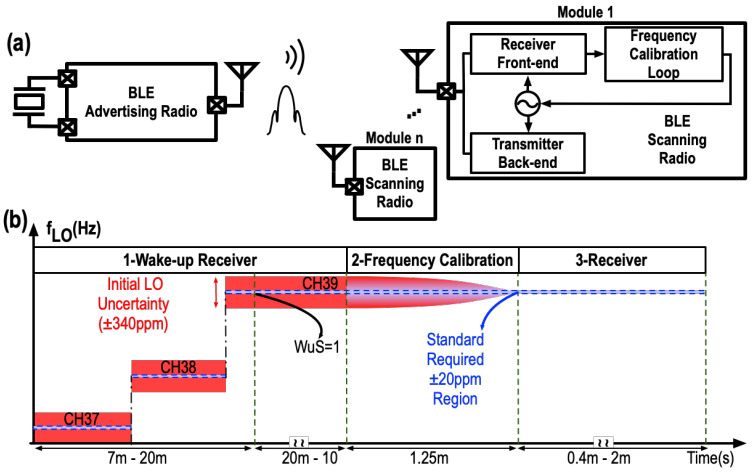


Fig. 1. Conceptual (a) block and (b) timing diagrams of the proposed over-the-air frequency calibration technique.

detection while providing 5.3 dB passive voltage gain via impedance upscaling and satisfying input matching through a 50 Ω termination at the isolation port. A four-stage balun-amplifier mixer (BALIXER) [4] exploits capacitive stacking to deliver 21 dB passive gain while down-converting the RF signal using a differential LO, followed by a low-pass filter (LPF). Combined, the BALIXER and LPF provide 46 dB gain and second-order real-pole filtering with an approximately 1 MHz cutoff frequency to attenuate out-of-band blockers, especially those at harmonics of the sampling frequency of the subsequent analog finite impulse response (AFIR) filter. The wide front-end cutoff frequency ensures the desired signal passes despite LO uncertainty.

The AFIR filters serve as two energy-detection bandpass filters (EDBPFs) to extract the energy of the upper (USB) and lower (LSB) sidebands of the downconverted signal. Accounting for the near (±1 MHz) LO uncertainty, the center frequencies of the USB and LSB filters are set at ±500 kHz with a 660 kHz bandwidth (BW), balancing energy capture and sideband rejection, as narrower filters improve opposite-sideband attenuation but reduce detected energy. The EDBPFs operate with a 16 MHz clock, selected to balance power consumption and aliasing suppression. The AFIR outputs feed two envelope detectors, whose output signals are digitized by level comparators (CMPs) and processed by a digital signal processor (DSP) to detect wake-up signatures. The DSP measures USB and LSB durations and declares a hit if either sideband falls within a valid duration range. This sideband-based detection reduces false misses compared to conventional full-spectrum evaluation [5], since at least one sideband remains valid even under large LO frequency error and strong adjacent-channel interference (ACI).

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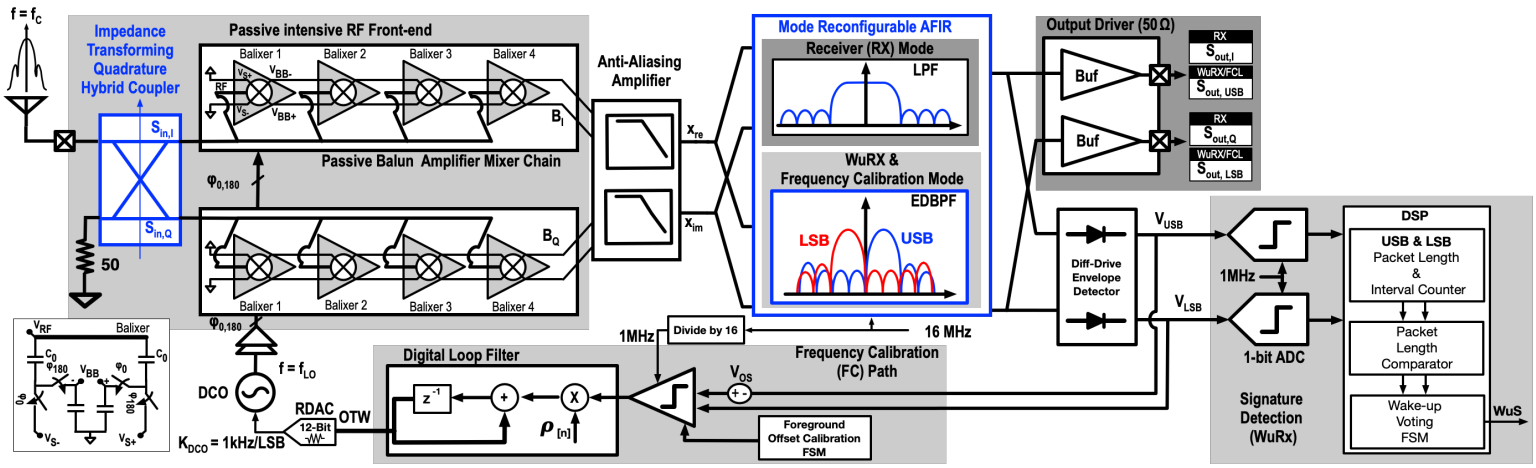


Fig. 2. Block diagram of the proposed multi-mode receiver with over-the-air frequency calibration.

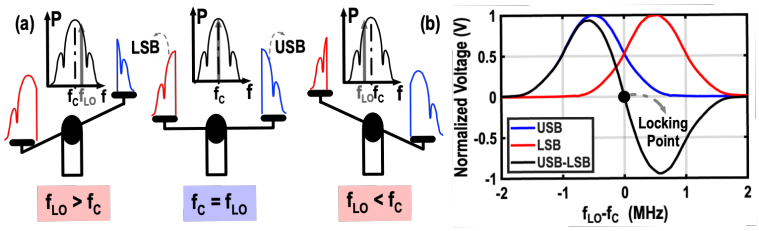


Fig. 3. (a) Operating principle and (b) open-loop transfer function of the OTA-FLL.

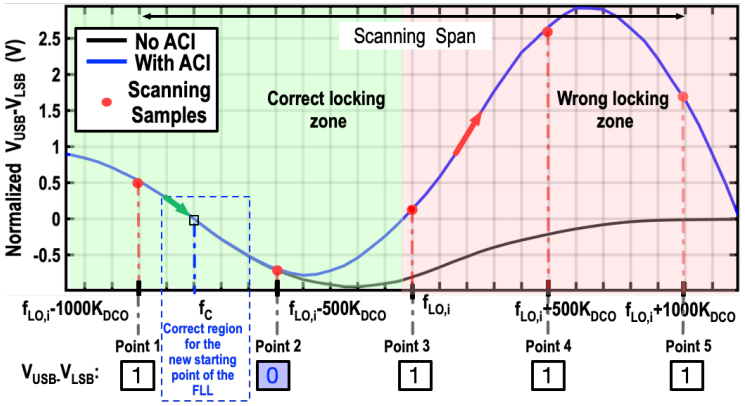


Fig. 4. OTA-FLL open-loop transfer function with and without ACI, and channel-scanning principle.

After wake-up detection, the system enters OTA frequency calibration. As shown in Fig. 3 (a), when the LO frequency (f_{LO}) matches the input center frequency (f_c), the detected USB and LSB energies are equal, since a whitened GFSK signal with equiprobable 0 and 1 symbols produces balanced sidebands. If $f_{LO} > f_c$, LSB power exceeds USB, indicating the Digitally-Controlled Oscillator (DCO) frequency should be reduced, and vice versa. Hence, in the FLL, a comparator monitors the voltage difference of the USB and LSB envelope detectors (V_{USB}, V_{LSB}), acting as a bang-bang frequency detector. Its output is integrated by a digital loop filter (DLF) to adjust the oscillator tuning word (OTW) and correct its frequency error ($\Delta f_{LO} = f_{LO} - f_c$). Both the integrator and comparator operate at a 1 MHz clock, divided from the AFIR clock, and its frequency accuracy does not affect the FLL locking point. A foreground on-chip calibration reduces the comparator offset voltage (V_{OS}) to 100 µV [6]. This results in a residual frequency error of $V_{OS}/K_{FD} \approx 0.2$ kHz, where $K_{FD} \approx 0.5$ V/MHz is the frequency-detection gain of the proposed OTA-FLL, depending on the input signal power and receiver gain.

ACI poses a key challenge during frequency calibration. As shown in Fig. 4, if the desired signal is in channel k and a strong interference lies in k+1, the ACI can dominate the USB energy when the initial Δf_{LO} is large and positive, reversing the polarity of the USB–LSB power (i.e., red area in Fig. 4) and causing the loop to lock incorrectly to the ACI. In contrast, if Δf_{LO} initially lies in the correct locking zone (i.e., green area), the loop converges properly. To prevent false locking, a channel-scanning method based on Bolzano's intermediate value theorem is used to position the DCO frequency in the correct zone before activating the FLL. After wake-up detection, the loop is held open while the LO frequency is stepped across five points equally spaced within the expected ±400 ppm (±1 MHz) range around the initial DCO frequency ($f_{LO,i}$). At each step, USB–LSB power is integrated for approximately 50 µs to determine the USB–LSB polarity. The DCO tuning word is then set to the region where USB–LSB polarity transitions from positive to negative, ensuring operation in the correct locking zone. This procedure reliably avoids false locking for all initial Δf_{LO} and ACI conditions with a signal-to-interference ratio (SIR) above −23 dB. Following channel scanning, Δf_{LO} is reduced from ±400 ppm to ±100 ppm, after which the FLL reduces Δf within ±20 ppm. In the final OTA calibration stage, the OTW is averaged over 512 cycles to improve accuracy. During data reception, this OTW is then held, and the AFIR circuits are reconfigured as two 750 kHz LPFs.

III. Circuit Implementation of Key Components

IT-QHC: As shown in Fig. 5, an IT-QHC with an impedance transformation ratio of T uses two horizontal $\lambda/4$ lines with characteristic impedance of $Z_0 \times \sqrt{0.5T}$ and two $\lambda/4$ vertical lines of Z_0 and $T \times Z_0$. It provides equal power split with a 90° phase shift, while transforming the port impedance from Z_0 at the input to $T \times Z_0$ at the through and

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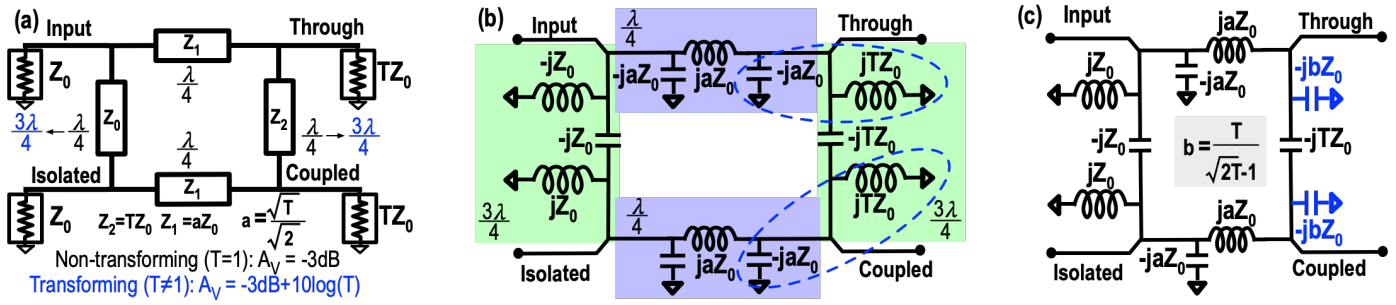


Fig. 5. Evolution of the impedance-transforming QHC: (a) branch-line coupler; (b) π-model equivalent; (c) proposed IT-QHC.

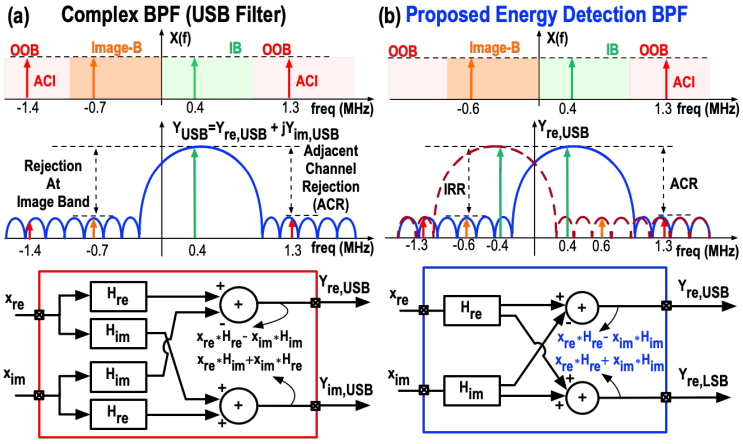


Fig. 6. Transfer function and block diagram of: (a) complex bandpass filter; (b) energy detection bandpass filter.

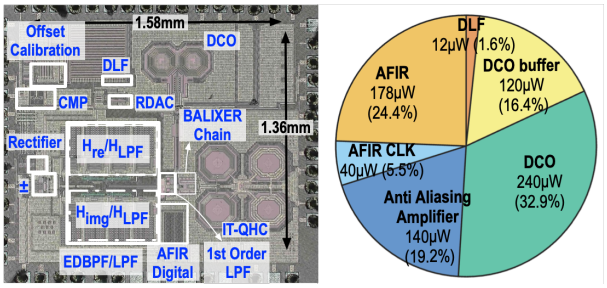


Fig. 7. Chip micropgraph and power consumption breakdown.

coupled ports, yielding a voltage gain of $-3 + 10\log(T)$ dB. Directly replacing $\lambda/4$ lines with CLC π-models requires impractically large series inductors of jTZ_0. To avoid this, the right vertical $\lambda/4$ line with TZ_0 characteristic impedance is extended to $3\lambda/4$, preserving coupler functionality while shifting the large inductors into shunt elements. The resulting shunt inductance combines with the shunt capacitance of the horizontal $\lambda/4$ lines to form an effective capacitor, eliminating the large inductors of the TZ_0 line and reducing IT-QHC area and loss. The IT-QHC achieves a simulated voltage gain of 5.3 dB—an 8.3 dB improvement over a conventional QHC—with a simulated image rejection ratio (IRR) > 32 dB across the BLE band.

EDBPF: To realize a BPF, the complex input signal $(x_{\mathrm{re}} + jx_{\mathrm{im}})$ must be convolved with a complex impulse response of $(H_{\mathrm{re}} + jH_{\mathrm{im}})$, which is obtained by frequency-shifting a replica LPF with the desired bandwidth and stopband rejection. This normally requires four AFIR filters to compute $x_{\mathrm{re}}H_{\mathrm{re}}$, $x_{\mathrm{im}}H_{\mathrm{im}}$, $x_{\mathrm{im}}H_{\mathrm{re}}$, and $x_{\mathrm{re}}H_{\mathrm{im}}$. However, in WuRX, and frequency calibration modes, only the USB and LSB envelopes are needed, which can be derived from the subtraction and summation of the first two terms, reducing the required AFIR filters—and their power and area—by a factor of 2. As shown in Fig. 6. (b), the resulting EDBPF achieves comparable image and ACI suppression to a full BPF while maintaining the desired-to-undesired power ratio. Owing to the Hermitian symmetry of the real signal spectrum, both signal and blockers appear mirrored in the image band, which does not affect envelope detection. Similar to [7], each AFIR filter is implemented using a 6-bit unary-weighted transconductance (g_m) DAC, modulated at 16 MHz according to the FIR coefficients. The g_m-DAC output current is then integrated on a capacitor over the 64-tap duration to realize the desired FIR filtering. The AFIR clock can be derived from the LO using frequency dividers or generated by an on-chip RC oscillator, as even a 10^4 ppm inaccuracy introduces only ±5 kHz and ±6.6 kHz shifts in the EDBPF center frequency and bandwidth, respectively.

DCO: A push–pull class-C DCO with series-aiding 8-shaped inductors is adopted for its high current efficiency, and resilience to electromagnetic interferences. A 6+6 resistive-interpolation DAC drives a varactor, achieving approximately 1 kHz/LSB tuning resolution.

IV. Measurement Results

The entire system, fabricated in 40 nm CMOS, occupies 2.15 mm^2 and consumes 730 µW from a 0.85 V supply (see Fig. 7). As shown in Fig. 8 (a)-(d), in WuRX and frequency calibration modes, the receiver transfer function from input to AFIR outputs exhibits 72 dB gain, 25 dB–35 dB IRR, and 40 dB rejection at the adjacent channel. The input return loss (S_{11}) is < -10 dB, and the noise figure (NF) is < 13.6 dB across in-band frequencies and the BLE band. The IIP3 and IIP2 are -23.7 dBm and +10 dBm at the adjacent channel and reach +10 dBm and +60 dBm at $\Delta f/\mathrm{BW_{CH}} = 10$, where $\mathrm{BW_{CH}}$ denotes the BLE channel bandwidth and Δf is the blocker offset frequency from center of the desired channel.

Fig. 9 (a) shows the transient response during frequency calibration with an input GFSK signal of -86 dBm, an initial LO frequency error of -815 kHz, and a lower adjacent-channel blocker 23 dB stronger than the signal (6 dB above BLE specification). The proposed five-point channel-scanning scheme first reduces the frequency error to −110 kHz and places the DCO frequency in the correct locking zone. The FLL then settles within 200 µs, and the DCO OTW is averaged over 512 µs

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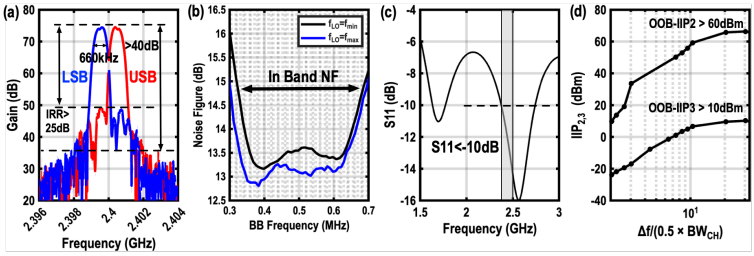


Fig. 8. Measured (a) receiver transfer function from input to EDBPF outputs, (b) noise figure, (c) input return loss, (d) IIP2 and IIP3 in WuRX and frequency calibration modes.

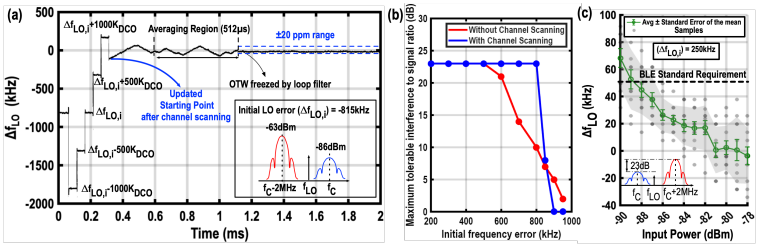


Fig. 9. Measured (a) transient response during frequency calibration; (b) maximum tolerable interference to signal ratio with and without channel-scanning technique; (c) post-calibration frequency error versus input signal power under SIR = -23 dB.

to mitigate frequency noise and temporary variations from 0-1 symbol imbalance and energy detector memory. Hence, as shown in Fig. 9 (b), the channel-scanning method extends the locking range from ±500 kHz to ±830 kHz under -23 dB SIR. Fig. 9 (c) shows that with -23 dB SIR, the post-calibration error meets the ±20 ppm (±50 kHz) BLE requirement for input powers above -86 dBm (16 dB better than the required BLE sensitivity).

In data reception mode, the DCO operates in an open-loop configuration, with measured frequency noise and drift of 5 kHz over the maximum BLE packet duration of 2 ms. The AFIR filters are reconfigured to low-pass mode, yielding a zero-IF receiver with 73.5 dB gain, 40 dB adjacent-channel rejection, and 14 dB NF across the BLE band, as shown in Fig. 10. The receiver achieves a sensitivity of -84 dBm at a bit error rate (BER) of 10^{-3}, while maintaining IIP2 and IIP3 profiles similar to those in WuRX mode. Table I compares our work with prior-art crystal-less BLE receivers. Only this work and [8]—which directly uses the downconverted input signal as the PLL reference—are fully BLE-compliant, but our design burns half the power, achieves lower post-calibration frequency error, and tolerates stronger ACI, enabling efficient crystal-less IoT nodes.

V. Conclusions

This paper presented a 730 μW crystal-less receiver that calibrates the frequency accuracy of an on-chip LC oscillator from ±340 ppm to ±20 ppm within 1.1 ms, tolerating a −23 dB SIR. This is achieved by introducing 1) a FLL that calibrates the oscillator frequency by comparing the energies of the USB and LSB sidebands of the received GFSK signal; 2) an energy-detection bandpass filter for ACI rejection and sideband energy detection; 3) a channel scanning technique to extend the frequency locking range under strong ACIs; 4) an IT-QHC to generate I/Q signals with passive voltage gain.

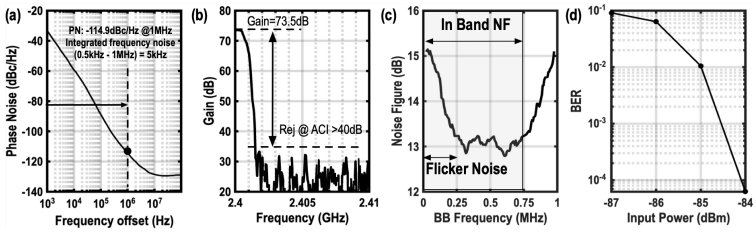


Fig. 10. Measured (a) DCO phase noise, (b) receiver transfer function, (c) noise figure, and (d) BER with open loop DCO.

TABLE I
Comparison with prior crystal-less BLE receivers.

	This work			JSSC '21 [8]			VLSI '19 [9]		TMTT '25 [10]
Freq. Calibration Technique	OTA BLE-sideband energy comparison FLL			OTA BLE-referenced PLL			OTA Zigbee based CRC feedback		OTA CW-referenced PLL
Modes of operation	WuRX	FC#	RX	WuRX	FC	RX	FC	RX	FC
Sensitivity (dBm)	-86	-86	-84	-94	-86	-86	-83.5	-83.5	N/A
Power (μW)	730			1500			1030		2500
NF (dB)	14			12			N/A		N/A
Max DCO initial Freq. error (ppm)	340			400			N/A		N/A
Freq. error after calibration without ACI & with ACI (ppm)	15 20 (SIR = -23 dB)			N/A 20 (SIR = -20 dB)			N/A		60 False lock
Min tolerable SIR for FC mode (dB)	**-23 (2 MHz offset)**			-20 (2 MHz offset)			-28 (5 MHz offset)		+2 (2 MHz offset)
Oscillator PN (FOM) @1MHz offset (dBc/Hz)	-114.9 (-188.7)			-117.1 (-187.6)			-117* (-188)		-116.3 (-185.2)
IQ generation	**IT-QHC**			No I/Q generation			Polyphase RC		No I/Q generation
Filtering Technique	**Mode reconfigurable EDBPF/LPF**			Cascaded biquad			Cascaded IIR		No Filtering
Image Freq. Induced False locking	**No**			Yes			No		Yes
OOB IIP3 (dBm)	**10**			N/A			N/A		N/A
OOB IIP2 (dBm)	**60**			N/A			N/A		N/A
Area [mm²]	2.15 (1.6†)			1.33			3.06 (1.48†)		1.4
Technology [nm]	40			40			65		28

#Frequency Calibration *Estimated from $FOM = PN - 20log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1m}\right)$ †Core area (RF, digital and BB only)

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