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Impact of Quasi-Two-Level Converters on Common-Mode Currents in Inverter-Fed Drive Systems

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***Abstract*—In motor drives, the quasi-two-level (Q2L) operation of a multilevel converter introduces a controllable inter-cell delay between level transitions, enabling shaping of the generated output-voltage spectrum and common-mode voltage (CMV). This article quantifies the impact of Q2L on common-mode currents and presents a simplified harmonic approximation that maps any two-level (2L) SPWM spectrum to its Q2L counterpart via a closed-form, delay-dependent scaling factor that also captures finite $\mathrm{d}v/\mathrm{d}t$. The model supports rapid benchmarking over key design variables, namely the number of switching cells N, inter-cell delay t_d, and rise/fall time t_{rf}, and is accurate in practice for $t_d f_c \lesssim 0.1$, where f_c is the PWM carrier frequency. Experimental validation on a flying-capacitor multilevel inverter operated in Q2L mode, assessed using a DC-side conducted emissions measurement test setup based on the CISPR 25 standard, demonstrates tunable attenuation bands in the low-MHz range and measured reductions of up to 12 dB around 1 MHz when increasing N and appropriately tuning t_d. These results provide simple design rules for targeting frequency bands of concern and indicate that Q2L can materially lower common-mode emissions, and thus required filter size in weight- and volume-constrained applications such as in electric transportation.**

***Index Terms*—Electromagnetic compatibility, harmonic analysis, multilevel converters, pulse width modulation inverters, quasi 2-level (Q2L).**

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I. Introduction

MOTOR drives are key components in many industrial applications. With electrification of transportation, and many energy sectors, the design of motor drives becomes critical, particularly with respect to their efficiency and cost [1], [2]. Multilevel converters have been used for motor drives to improve power density and efficiency, as well as to reduce the current ripple in the machine windings, which can help improve the motor efficiency as well [3]. The most commonly-used multilevel topologies are neutral-point clamped (NPC) based, with diodes or active switches employed for neutral-point clamping operation. However, for five-level or higher output, most topologies employ flying capacitors, either in the DC-side bridges [4], or on the AC-side bridges [5]. These flying capacitors need to be rated for the load current at switching frequency. This is especially problematic in motor drives, where the currents during startup can be more than twice those in normal operation. In such cases, operating the multilevel converters as quasi-two-level (Q2L) converters can allow for smaller flying capacitors as well as take advantage of the performance of low-blocking voltage semiconductor devices. In this article, we consider a two-level (2L) motor drive, which can be replaced by a flying capacitor multilevel (FCML) converter operated in Q2L mode as shown in Fig. 1. The FCML topology is chosen in particular since it is a series-connection of low-voltage devices to effectively block high DC-link voltage and thus, the losses are also distributed equally [6] which can especially be important in high-power applications such as motor-drives.

The Q2L operation of an FCML was first introduced by [7], where the FCML was operated in Q2L mode by switching the series-connected devices synchronously. The flying capacitors and a passive balancing network allow for steady-state balancing of the device voltage and thus, allows to remove snubber circuits conventionally employed during the series connection of semiconductors [7]. However, it is to be noted that during transients, and especially startup, the same considerations that apply to the conventional FCML also apply to the Q2L mode of operation. More details about pre-charge and start-up as well as standby mode of operation can be found in [8], [9]. This makes it a good candidate especially in medium-voltage (MV) applications where series-connection of semiconductors

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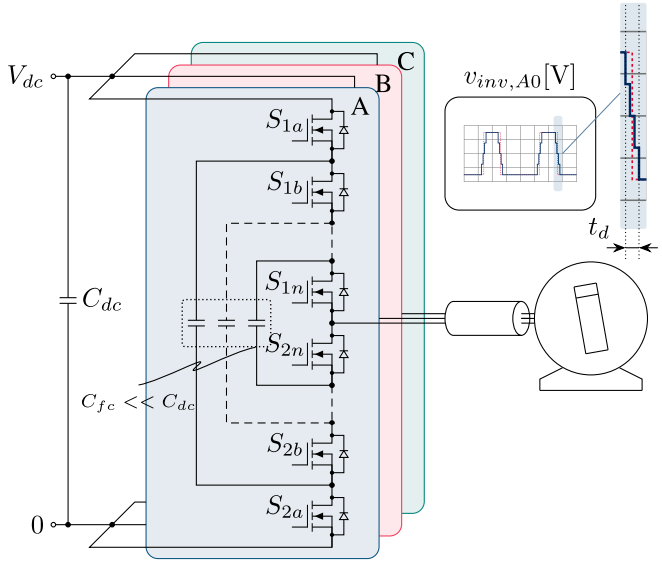


Fig. 1. Quasi-two-level (Q2L) converter with N-switching cells connected to a PMSM through a shielded cable. The output voltage waveform of a single-phase is shown with the stepped output having a time delay t_d for the Q2L shown in blue and the two-level (2L) output shown in red. The flying capacitors are assumed to be relatively small and are for transient voltage balancing.

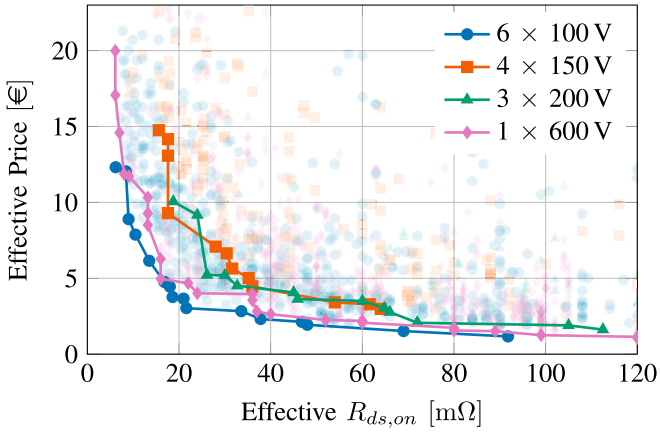


Fig. 2. Comparison of MOSFET prices for different number of series-connected devices and their corresponding effective on-state resistance. The Pareto front is highlighted in bold where it can be observed that the 100 V devices offer the best tradeoff. The data is obtained from Digikey [17] for a minimum order quantity of 5000.

is commonly employed to achieve the high blocking voltage necessary [10], [11]. In case the switching is not synchronous and staggered as shown in Fig. 1, then the switching states need to be modified using control algorithms to allow for the transient voltage balancing of the flying capacitors [10], [12], [13]. These staggered switching modifies the output voltage harmonics of the Q2L which can be used to mitigate common-mode currents in the system [14].

Traditionally, silicon-based (Si-based) insulated gate bipolar transistors (IGBTs) are employed in such applications. The advent of wide-bandgap (WBG) semiconductors is excellent from an efficiency perspective due to their much faster switching speeds compared with the conventional Si-based semiconductors. However, they can increase common-mode emissions in the systems where they are employed [15], [16], resulting in larger common-mode filters, which is critical in weight/size-constrained industries such as transportation. One major advantage of Q2L is the additional degree of control with the time-delay between level transitions, which allows shaping of the generated output voltage harmonics and can therefore reduce common-mode current compared with a classical 2L converter [14].

A significant cost in a power inverter is due to the semiconductors. The impact of Q2L in terms of cost and equivalent on-state resistance is presented in Fig. 2 with the Pareto front highlighted. This comparison is relevant for relatively low-voltage motor drives where MOSFETs are typically employed. This is done to ensure the comparison is fairly done by only comparing MOSFETs with each other and show the impact of utilising low-voltage devices which typically offer excellent performance [18]. From Fig. 2, it can be observed that 100 V devices offer the best price-$R_{ds,on}$ ratio with the 600 V devices following closely after. Although this is a simplistic comparison based solely on the semiconductor cost, this shows the potential of Q2L to improve the price-performance tradeoff during the design of motor drives. In this case, only $R_{ds,on}$ is considered, since it is significant in motor drives. However, for other applications where switching losses are also critical, the tradeoff can be even better due to the better figure-of-merit (FOM) of devices with lower blocking voltage [18].

In addition to semiconductor costs, the implications of the more complex structure should also be explored. There has been significant research into control algorithms for voltage balancing, starting with open-loop algorithms [10], closed-loop implementations [9], [12], [13], [19] as well as thermal power routing [20]. There has also been additional research into employing the Q2L concept in existing multilevel topology, the so-called quasi-three-level (Q3L) operation of the FCML [7], the T-type [21] and the ANPC [22] to allow for the advantage of using low-voltage semiconductors in such topologies and reduce the size of the flying capacitors employed. In addition to the control complexity, simplifying auxiliary functions such as protection have also begun to be explored [23].

This article explores the implications of using Q2L in a motor-drive application. To this end, the contributions of the article are as follows.

1) A scaling factor approximation of the voltage harmonics of Q2L is presented to modify an existing 2L harmonic spectrum to its Q2L counterpart, enabling rapid benchmarking of Q2L against a conventional 2L inverter.
2) The implications of different Q2L operating modes on common-mode emissions are explored in terms of when the harmonics are attenuated and when they remain the same as that of a 2L converter.
3) The impact of Q2L common-mode emissions is verified in a DC-side common-mode emissions test setup based on the CISPR 25 standard [24].

The rest of the article is organised as follows. Section II derives the simplified harmonic approximation of the Q2L generated voltage harmonics. Section III, discusses the tunable

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Q2L parameters and their implications on the voltage spectrum. Section IV presents the experimental verification of the commissioned hardware prototype and states the assumptions. Section V benchmarks the impact of various Q2L operating modes on common-mode emissions. Some scope for future research is included in Section VI and the article is concluded in Section VII.

II. Simplified Approximation for Voltage Harmonics of a Q2L Converter

The voltage harmonics of three-phase three-wire 2L inverters have been extensively studied and derived in the literature [25]. The simplest case to analyse is that of the 2L converter with sinusoidal pulse-width modulation (SPWM) based on the triangular carrier method. The carrier frequency harmonics of such a converter can be derived using the Double Fourier analysis introduced by [26] in communication theory and adapted by [25] for power electronics. By doing the same analysis, the carrier-frequency harmonics of such a converter can be represented as

$$C_{mn,2\mathrm{L}} = \frac{2V_{\mathrm{DC}}}{m\pi} \cdot J_n\left(m\frac{\pi}{2}M\right) \cdot \sin\left([m+n]\,\frac{\pi}{2}\right) \cdot e^{\mathrm{j}n\phi_{\mathrm{X}}} \tag{1}$$

where m is the carrier frequency harmonic number (with $m > 1$), n indexes the sidebands of the carrier frequency with $n \in [-\infty, \infty]$, V_{DC} is the DC-link voltage, $J_n(x)$ is the Bessel function of the first kind, $M = 2V_{\mathrm{AC,pk}}/V_{\mathrm{DC}}$ is the modulation index and ϕ_{X} is the phase-shift of the modulating signal of each phase (where X = A/B/C).

The expression in (1) only provides the harmonic amplitude corresponding to the n^{th} sideband of the m^{th} carrier harmonic of the 2L inverter with SPWM. To find the harmonic amplitude at a certain frequency f, the effects of all the sidebands that contribute to the particular frequency component need to be considered. This is relevant in two cases:

1) When the ratio between the PWM carrier frequency (f_c) and grid fundamental frequency (f_0) (i.e., f_c/f_0) is low, the sidebands of the carrier frequency can overlap causing significant increases in certain sideband harmonics [27].
2) At high frequencies (i.e., $m \geq 50$), the sideband contributions become significant because the harmonic amplitudes decrease at the rate of ∼25 dB/decade (for SPWM) and the Bessel function $J_n(r)$ peaks near $n \approx r$, and thus, their contributions need to be taken into account.

To account for this, the contribution of all sidebands contributing to a given considered frequency needs to be considered. For m carrier harmonics and n sidebands considered, the harmonic amplitude corresponding to each frequency bin can be calculated as

$$C_{2\mathrm{L}}(f) = \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} C_{mn,2\mathrm{L}} \cdot \delta_{f,mf_c+nf_0} \tag{2}$$

where f_c is the carrier frequency, f_0 is the fundamental frequency and, $\delta_{i,j}$ is the Kronecker delta function and is defined as

$$\delta_{i,j} = \begin{cases} 1, & i = j \\ 0, & i \neq j \end{cases}. \tag{3}$$

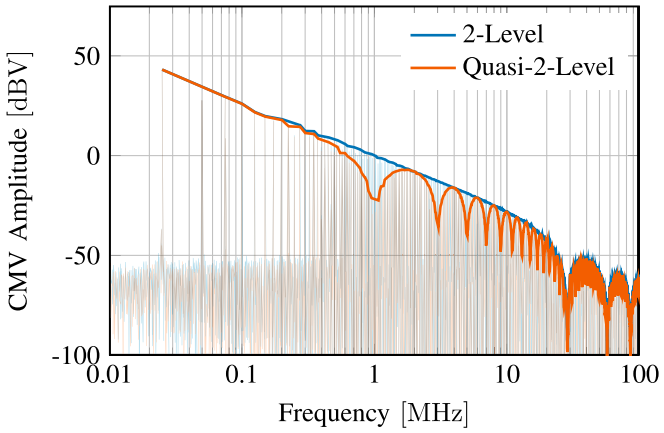


Fig. 3. Common-mode voltage (CMV) harmonics of a two-level converter with $^{\mathrm{d}v}/_{\mathrm{d}t} = 10$ V/ns and a three-level operated as a Q2L converter with effective time-delay of 500 ns and $^{\mathrm{d}v}/_{\mathrm{d}t} = 5$ V/ns. The effect of the Q2L can be seen with the additional zero harmonic amplitude bands introduced at 1 MHz and its corresponding harmonics, which is scaled according to the number of levels, and the effective time delay. The effect of $^{\mathrm{d}v}/_{\mathrm{d}t}$ can be observed at the corner frequency of ∼28.6 MHz and its corresponding harmonics along with steeper harmonic amplitude roll-off.

With the harmonic amplitudes per phase, the common-mode voltage (CMV) harmonics can thus be found as follows:

$$C_{2\mathrm{L,CMV}}(f) = \frac{C_{2L,\mathrm{A}}(f) + C_{2L,\mathrm{B}}(f) + C_{2L,\mathrm{C}}(f)}{3}. \tag{4}$$

However, the effect of $^{\mathrm{d}v}/_{\mathrm{d}t}$ is not captured in the above expressions. To simplify the addition of this effect, the rise-time and fall-time are assumed to be the same. This is not strictly true in practice, and more detailed models as presented in [16] can be utilised, but this assumption allows a simplified analysis. For every frequency bin f and its corresponding harmonic amplitudes $C_{2\mathrm{L}}(f)$ from (2) or (4), the effect of $^{\mathrm{d}v}/_{\mathrm{d}t}$ can be incorporated by scaling them assuming a trapezoidal wave with finite rise/fall-time as [28]

$$C_{2\mathrm{L}(^{\mathrm{d}v}/_{\mathrm{d}t}=\mathrm{finite})}(f) = C_{2\mathrm{L}}(f) \cdot \mathrm{sinc}\,(t_{rf} \cdot f) \tag{5}$$

where $\mathrm{sinc}(x) = \sin(\pi x)/\pi x$ is the normalised sinc function and t_{rf} is the rise/fall time. The effect of (5) can be observed in Fig. 3, where the harmonic amplitudes roll-off at a higher rate (40 dB/decade) compared with the usual ∼25 dB/decade prior to the rise/fall-time corner frequency.

Considering the Q2L converter, a few modifications are required in the analysis. There are N-switching cells in a Q2L converter, which provide $N-1$ steps in the output voltage waveform. These switching cells can be switched synchronously to have an output voltage similar to a 2L converter. However, they can also have a small time-delay introduced between them to have a staggered output voltage as shown in Fig. 1 since only one switching cell is switched at any given instant. The time delay for each switching cell can be incorporated as a delay duty-cycle in addition to the original modulating signal as follows:

$$\mathbf{D_d} = 2 \cdot t_d \cdot f_c \cdot \mathbf{k} \tag{6}$$

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where $\mathbf{D_d}$ is a vector of length N with each element providing the delay-duty cycle corresponding to each switching cell, t_d is the total time delay to switch from 0 to $V_{\rm DC}$ and vice-versa, f_c is the carrier frequency and, $\mathbf{k}$ is a delay distribution vector that is defined as

$$\mathbf{k} = \left\{ k_i \mid k_i = -1 + \frac{2(i-1)}{N-1},\ i = 1, 2, \ldots, N \right\}. \quad (7)$$

Based on this modification of the modulating signal, the output voltage harmonics of a Q2L are modified to be [14]

$$C_{mn,\rm Q2L} = \sum_{k=1}^{N} \frac{2V_{\rm DC}}{m\pi N} \cdot J_n\left(m\frac{\pi}{2}M\right) \cdot \sin\left(\left[m(1+D_{d,k})+n\right]\frac{\pi}{2}\right) \cdot e^{{\rm j}n\phi_{\rm X}} \quad (8)$$

where $D_{d,k}$ is the k^{th} element of $\mathbf{D_d}$. $D_{d,k}$ can be separated out by applying the trigonometric identity: $\sin(A+B) = \sin A \cos B + \cos A \sin B$ to (8)

$$C_{mn,\rm Q2L} = \sum_{k=1}^{N} \frac{2V_{\rm DC}}{m\pi N} \cdot J_n\left(m\frac{\pi}{2}M\right) \left\{ \sin\left(\left[m+n\right]\frac{\pi}{2}\right) \cdot \cos\left(mD_{d,k}\frac{\pi}{2}\right) + \cos\left(\left[m+n\right]\frac{\pi}{2}\right) \cdot \sin\left(mD_{d,k}\frac{\pi}{2}\right) \right\} \cdot e^{{\rm j}n\phi_{\rm X}}. \quad (9)$$

The term D_{dk} has symmetric positive and negative time-delays, and thus, the second term in the summation is cancelled out in (9) and is simplified as

$$C_{mn,\rm Q2L} = \sum_{k=1}^{N} \frac{2V_{\rm DC}}{m\pi N} \cdot J_n\left(m\frac{\pi}{2}M\right) \cdot \sin\left(\left[m+n\right]\frac{\pi}{2}\right) \cdot \cos\left(mD_{d,k}\frac{\pi}{2}\right) \cdot e^{{\rm j}n\phi_{\rm X}}. \quad (10)$$

This can be simplified with (1) as

$$C_{mn,\rm Q2L} = C_{mn,\rm 2L} \cdot \sum_{k=1}^{N} \frac{1}{N} \cos\left(mD_{d,k}\frac{\pi}{2}\right). \quad (11)$$

Substituting $D_{d,k}$ from (6)

$$C_{mn,\rm Q2L} = C_{mn,\rm 2L} \cdot \sum_{i=1}^{N} \frac{1}{N} \cos\left(\pi \cdot k_i t_d \cdot m f_c\right). \quad (12)$$

The expression in (12) can be utilised to obtain the Q2L voltage harmonics if the C_{mn} values of a corresponding 2L inverter are already available. It must be noted that the expression in (12) is valid only when the voltage is distributed equally across all the switching cells. In case of unbalances due to the modulation strategy, this can be taken account by introducing a factor F_k instead of the constant $1/N$ to represent the fraction of voltage contributed by the $k^{\rm th}$ switching cell [20]. However, in normal operation, the t_d and the flying capacitor sizes are chosen to minimise the voltage ripple and thus, maintain relatively equal voltage distribution.

As discussed before, to find the harmonic amplitude corresponding to a given frequency, the effects of all sidebands need to be considered. The contribution of the $\cos(x)$ function is the scaling of the harmonic amplitude which is close to 1 when $mf_c << 2/k_i t_d$, and as the considered frequency comes close to $2/k_i t_d$, the scaling goes to zero. If the delay-time is much smaller compared with the carrier time-period i.e., $t_d << 1/f_c$, then the effective harmonic amplitude at each frequency f can be approximated as

$$C_{\rm Q2L}(f) \approx C_{\rm 2L}(f) \cdot \sum_{i=1}^{N} \frac{1}{N} \cos\left(\pi \cdot k_i t_d \cdot f\right) \quad (13)$$

where k_i is the i^{th} element of the delay distribution vector $\mathbf{k}$ and $f \approx mf_c$, which holds true when the assumption of the small time-delay is true. Equation (13) can be modified for finite ${\rm dv}/{\rm dt}$ as follows:

$$C_{\rm Q2L(\frac{dv}{dt}=finite)}(f) \approx C_{\rm 2L}(f) \cdot {\rm sinc}\left(t_{rf} \cdot f\right) \cdot \sum_{i=1}^{N} \frac{1}{N} \cos\left(\pi \cdot k_i t_d \cdot f\right). \quad (14)$$

The following observations can be made from Fig. 3 and the Q2L harmonic model in (14).

1) The Q2L converter introduces zero harmonic amplitude bands corresponding to the effective delay, which can be observed in Fig. 3 [14].
2) The harmonic peaks of the Q2L correspond to the conventional 2L converter output. Thus, no additional roll-off in the harmonic amplitude is introduced by the Q2L converter.
3) The simplified expression in (13) has an error that varies depending on the time-delay introduced and is shown in Fig. 4 along with the comparison between the FFT and the model for the case with the worst-case error in Fig. 4(a), i.e., $t_d = 4$ μs. It is to be noted that such a high value of t_d is not realistic and is only used in this case to show how the approximation can lose validity. In realistic converter design, t_d is limited since it reduces the highest modulation index as a function of the switching frequency employed for operation as well as reduces the size of the flying capacitors employed [14]. The error is introduced because of the approximation made in deriving (13) where an assumption of $f \approx mf_c$ is made, and thus, some sidebands are not modelled accurately. Given this error, the model is best suited to predict harmonics when the factor $t_d f_c \lesssim 0.1$ for reasonable accuracy.
4) The expression in (13) is not limited to sine-triangle modulation but holds for any modulation scheme used. This is especially useful for benchmarking the impact of Q2L with selective harmonic elimination and/or direct-torque control techniques where the pulse-widths are not necessarily pre-programmed and are commonly implemented in motor drives. With the harmonic amplitudes from a 2L converter, the impact of Q2L can be immediately estimated from the frequency and harmonic amplitude vectors.

III. Q2L Converter Design Considerations

In Section II the modelling of voltage harmonics of a Q2L converter based on 2L operation was discussed. During the

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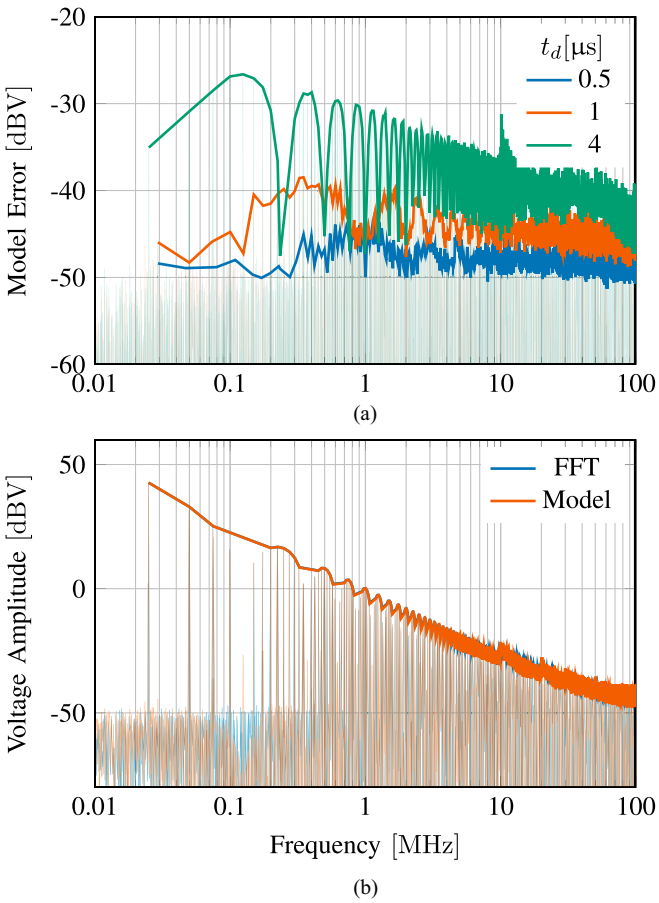


Fig. 4. (a) Error of the model in (13) compared to the FFT for increasing time-delays of the Q2L converter in dB V. The error is observed to increase with time-delays since the error introduced in the model by the assumption that $f \approx mf_c$ depends on $t_d << 1/f_c$ and increases the error at a lower harmonic. In this case, the carrier frequency $f_c = 25$ kHz, the modulation index is 0.8, and the number of switching cells $N = 2$ with instantaneous rise/fall-time. (b) Harmonic voltages of the FFT compared with the model in (13) for the worst case of $t_d = 4$ µs. It can be observed that the error is primarily in the sidebands due to the assumption of $f \approx mf_c$ being less true. However, the envelope is still representative of the spectrum.

TABLE I
OPERATIONAL PARAMETERS OF THE Q2L

Parameter	Symbol	Value
DC-link voltage	V_{DC}	350 V
Modulation index	M	0.8
Fundamental frequency	f_0	50 Hz
Carrier frequency	f_c	25 kHz
Rise/fall-time	t_{rf}	35 ns

design, it is also important to consider the system-level impact of utilising Q2L converters. This section provides the trade-offs in selecting key parameters in the Q2L. The operational parameters utilised are specified in Table I.

A. Number of Switching Cells

The number of switching cells utilised matters not only from cost and efficiency perspectives, but also for the harmonic

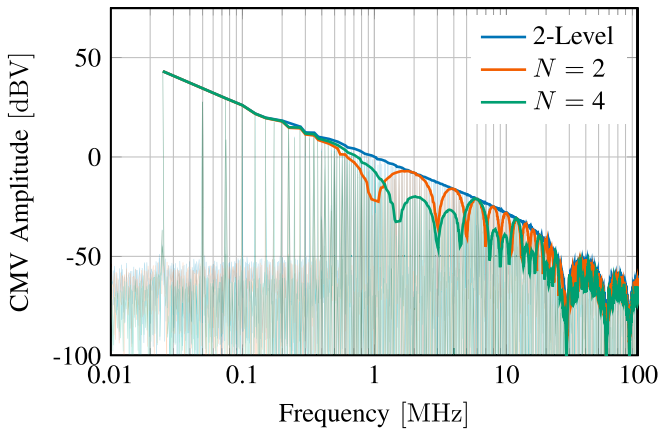


Fig. 5. Effect of increasing the number of switching cells (N) with constant time-delay, $t_d = 500$ ns on the CMV harmonic amplitudes. The harmonic amplitudes have additional attenuation at harmonics of the time-delay. However, the peak amplitudes before the rise/fall-time frequency still remain the same as that of a 2L converter.

attenuation achieved. With a constant time-delay of 500 ns introduced, the CMV harmonic amplitudes for different numbers of switching cells utilised are shown in Fig. 5. The effect of the time-delay can be seen in the low MHz range due to the chosen delay-time, with additional zero harmonic amplitude regions introduced. For a Q2L with $N = 2$, the zeros at multiples of the time-delay harmonics can be observed and the peak remains the same as that of the 2L converter. For Q2L implementations with a higher number of switching cells, the effect of adding multiple cosines as shown in (14) is evident, with multiple peaks lower than those of a 2L converter.

The major frequencies affected by the Q2L scale as a function of the number of switching cells, N as follows:

$$f_k = k \cdot \frac{N-1}{N} \cdot \frac{1}{t_d}, \qquad k \in \mathbb{R}_{>0} \tag{15}$$

where k is the harmonic that is modified due to Q2L and the amplitude at these frequencies is defined by

$$C_{\mathrm{Q2L}}(f_k) = \begin{cases} C_{\mathrm{2L}}(f_k), & k \in \{N, 2N, 3N, \dots\} \\ 0, & k \in \mathbb{R}_{>0} \setminus \{N, 2N, 3N, \dots\}. \end{cases} \tag{16}$$

where the '\' operator signifies exclusion of those harmonics from the set.

Thus, from (16) it can be observed that this frequency strongly influences the voltage harmonics of the converter, and thus can be used as a simplified guideline in selecting a suitable time-delay. It should also be observed that the peak amplitude in all cases remains the same as that of the 2L converter, and thus it can be concluded that Q2L helps attenuate certain lower-frequency harmonics, while the frequency harmonic at which the 40 dB/decade roll-off occurs remains the same as shown in Fig. 5 due to the assumption of a constant rise/fall time.

B. Time-Delay

Together with the choice of the switching cells, the time-delay incorporated is an important consideration. Factors

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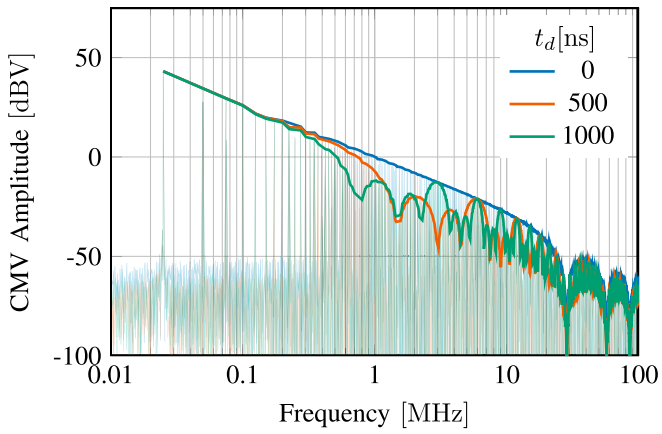


Fig. 6. Effect of increasing the time delay, t_d in a Q2L with four switching cells ($N = 4$). Increasing the delay time reduces the harmonic where the attenuation begins, however, this also affects the flying capacitor voltage ripple, in turn affecting its size.

that limit the introduced time-delay include the flying capacitor size and the maximum duty-cycle for a given switching frequency [14]. Fig. 6 shows the effect of increasing delay time. It can be observed that the attenuation shifts to lower frequencies with increasing delay-time. This must be traded off against the allowable voltage ripple on the flying capacitors, and consequently the flying capacitor size. Additionally, if the system impedance is known, the delay-time can be tuned as a traded-off to reduce common-mode currents, by introducing zero CMV harmonic amplitude at the frequencies where the system impedance is lowest. Since the number of switching cells remains the same, the 40 dB/decade roll-off occurs at the same frequency.

In addition to the harmonic impact of the time-delay, it is important to consider that the minimum pulse-width achievable is reduced due to the staggered switching. This limits the maximum modulation index achievable for a given switching frequency as follows [14]:

$$M_{\max} \leq 1 - 2 \times t_d \times f_c \tag{17}$$

where $M_{\max}$ is the maximum modulation index achievable. An extensive discussion on this matter is available in [14] and must be taken into account during the Q2L design.

This section has introduced the design parameters of a Q2L converter and their implications for the CMV harmonic spectrum. In a practical system, the common-mode impedance plays a major role in the amount of common-mode currents introduced. To this end, a practical setup is considered and the DC-side common-mode emissions of a Q2L converter are measured to demonstrate the effectiveness of Q2L in modifying the harmonic emissions of the converter, especially in the low- MHz band.

IV. Experimental Operation of the Q2L

To verify the effectiveness of the Q2L in attenuating harmonics of interest, an experimental setup was constructed. The setup is as shown in Fig. 7 and, the measurement equipment details are provided in Table II. Key considerations for this experimental setup are provided below.

TABLE II
Measurement Equipment

Equipment	Part Number
Differential Current probe	Micsig CP1003
Differential Voltage probe	Micsig DP10007
RF Current probe	FCC F-33-2
Oscilloscope	Keysight DSO-X 3024A
Spectrum Analyzer	Siglent SVA 1015X

1) The hardware prototype has four switching cells i.e., $N = 4$. In this article, $N = 2$ is the operation of the same prototype with two adjacent switching cells driven by the same signal using jumpers on the board.
2) A three-phase $R - L$ load with $R = 50\ \Omega$ and $L = 1$ mH per phase was mounted on a plate to emulate the chassis of the motor. Although not fully representative, it allows for a reliable setup to benchmark the converter for different N and t_d in open-loop.
3) A shielded cable 2 m in length was used to connect the inverter to the load. This better reflects practice, considering the parasitic capacitance of the shielded cable can exceed that of the motor in long-cable cases [29].
4) The chosen switching frequency of 25 kHz is relatively high for a motor-drive system, mainly due to load constraints. However, it should not affect the experiment because the time-delay t_d is sufficiently small, so its effect lies in a frequency band well above the switching harmonics. In a real setup, the harmonic amplitudes would be lower while maintaining the same effect on the high-frequency bands.
5) A PLECS RT-box was used to control the hardware for rapid prototyping.
6) An open-loop balancing algorithm was implemented to balance the flying capacitor voltages by varying the applied switching sequence order. Further details can be found in [10], [19].
7) A dead-time of 2 μs was implemented to allow for the open-loop balancing algorithm to work reliably in the maximum delay-time condition. This delay can be reduced by using closed-loop control with flying capacitor voltage measurements for which various implementations are available in [9], [12], [13], [14]. This also affects the harmonic spectrum, particularly above 10 MHz due to the different rise/fall-time caused by the soft-switching (one of the turn-ON or turn-OFF is always soft-switched in an inverter depending on the current direction).

Experimental waveforms are shown in Fig. 8. The measured rise-time is approximately 10 ns. Fig. 8(a)–(c), show operation with synchronous switching ($N = 1$), as a three-level converter ($N = 2$), and as a five-level converter ($N = 4$), respectively, with a time-delay of 500 ns. It can be observed that voltages and currents exhibit lower high frequency noise for $N = 4$ operation, owing to greater harmonic attenuation, compared

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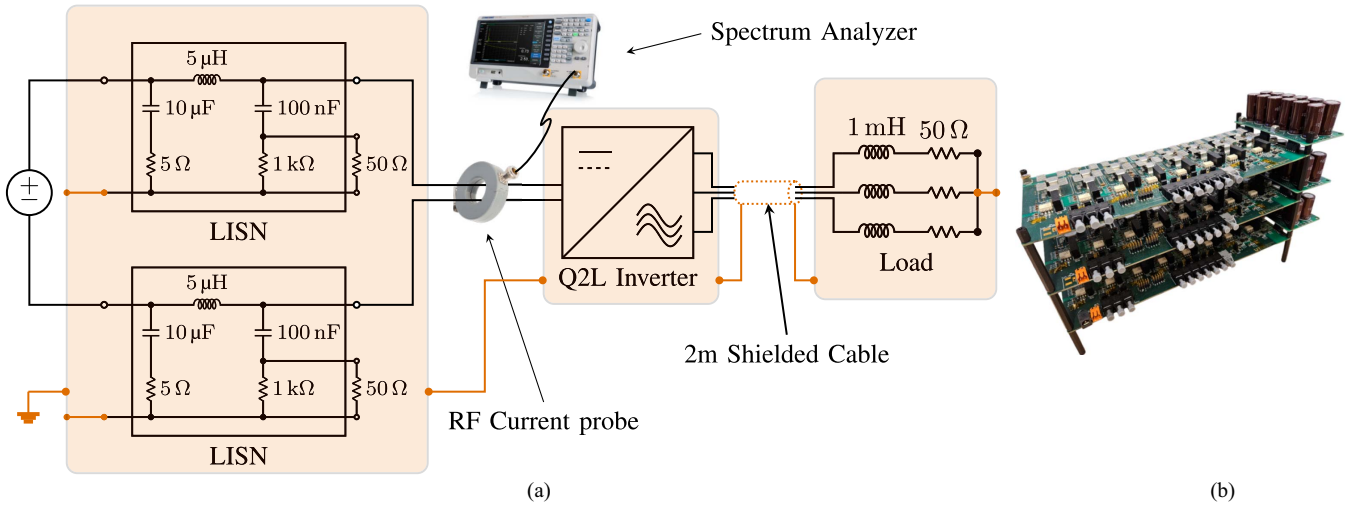


Fig. 7. (a) Schematic of the experimental setup is shown. The copper boxes signify the copper plates used to provide the ground plane for the LISNs and simulate the chassis for the inverter and the load. The common-mode emissions are measured to comply with CISPR-25, with a DO-160 LISN (which modifies the response below 30 kHz). (b) Experimental hardware prototype is shown, which is a five-level FCML converter that is operated as a Q2L. The flying capacitors are made of only MLCC capacitors since the chosen delay time (t_d) is relatively small to allow for an acceptable voltage ripple on the flying capacitors. This prototype can be switched between a full five-level operation ($N = 4$), three-level operation ($N = 2$) or 2L operation ($N = 1$) by utilising jumpers to synchronise the gate-signals of the semiconductors.

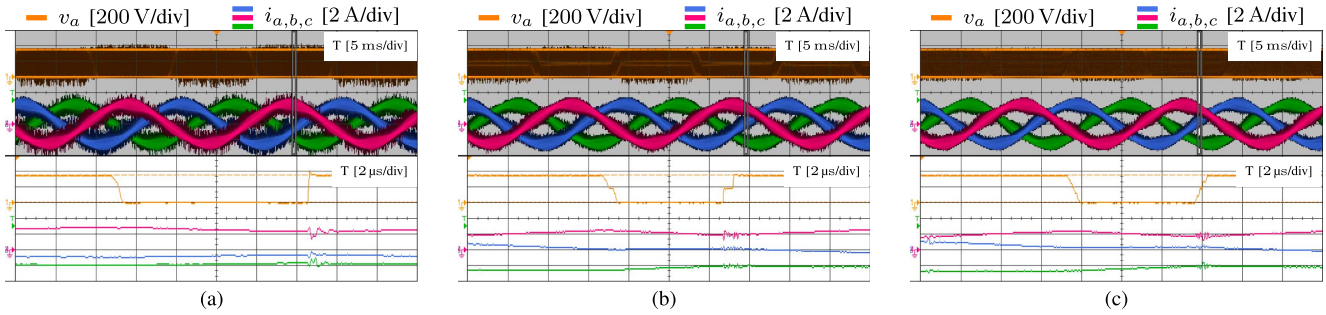


Fig. 8. Experimental waveforms of the: (a) 2L operation of the converter i.e., $t_d = 0$ ns. The Q2L operation of the converter is shown in (b) and (c) with $t_d = 500$ ns for $N = 2$ and $N = 4$ respectively. The reduction of high-frequency noise in the currents can be observed due to the longer delay times due to the attenuation of high-frequency harmonics by the Q2L operation.

with $N = 2$ and 2L operation. This is due to the attenuation of certain voltage harmonics as observed in Fig. 5.

With the converter operation verified, the DC-side emissions are measured to benchmark the impact of Q2L against 2L operation.

V. DC-Side Common-Mode Emissions

The converter is operated in various modes to benchmark the impact on common-mode emissions. The benchmark is performed by measuring the common-mode current using an RF current probe as shown in Fig. 7, mimicking the CISPR-25 current-based method [24]. The common-mode current measurements are taken with the FCC F-33-2 RF current probe connected to the Siglent SVA 1015X spectrum analyzer through a Tekbox TBFL1 transient limiter to provide input protection. The LISN output ports are terminated with 50 Ω to provide the correct impedance on the output ports.

The LISNs used are DO-160-compliant, which have an additional 10 μF input capacitance that modifies the response below 30 kHz. However, between 150 kHz and 30 MHz, the response is similar to that of a CISPR-25-compliant LISN. The setup is not fully compliant with the standard, but provides a sufficiently stable impedance for a fair benchmark of the converter's operation.

The converter is operated primarily in $N = 2$ and $N = 4$ modes, i.e., three-level or five-level outputs. Each of these modes are benchmarked against the 2L operation of the converter to show the harmonic attenuation of the Q2L for different time-delays.

A. Three-Level Operation ($N = 2$)

The three-level operation of the converter can be observed in Fig. 9. Similar to the voltage harmonics plot in Fig. 6, the attenuated harmonic shifts to a lower frequency band as the delay-time increases. Since the common-mode impedance of the system is not necessarily linear, shifting the zero harmonic amplitude band to lower frequencies does not necessarily imply

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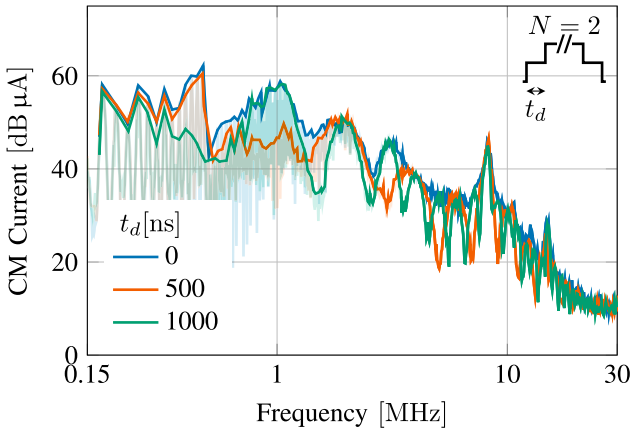


Fig. 9. DC-side common-mode emissions of the Q2L with three-levels i.e., $N = 2$ with varying delay times is shown. It can be observed that increasing time delay alone does not directly reduce the harmonic attenuation. This is because the impedance of the system also matters and thus, the Q2L needs to be tuned such that the zero harmonic amplitude band is introduced at the frequency where the impedance is the lowest.

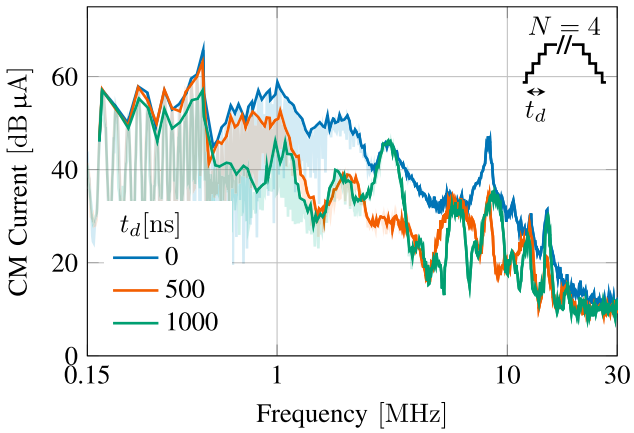


Fig. 10. DC-side common-mode emissions of the Q2L with five-levels i.e., $N = 4$ with varying delay times is shown. Compared to the $N = 2$ operation, the zero harmonic amplitude bands are also modified, as well as additional attenuation is introduced in more bands as shown in Fig. 5.

lower common-mode emissions. As shown in Fig. 6, the Q2L still has the same peak harmonic amplitude as the 2L operation, and this can also be observed in the common-mode emissions, especially near 1 MHz where the operation at $t_d = 1$ µs exhibits the same response as the 2L operation.

B. Five-Level Operation ($N = 4$)

The five-level operation creates additional attenuation in certain bands compared with the three-level operation, as observed in Fig. 5. The same effect can be observed in the common-mode emissions as shown in Fig. 10. In this case, due to the additional attenuation, the peaks around 1 MHz are attenuated for $t_d = 1$ µs relative to the three-level operation. The additional attenuation offers another degree of flexibility in the choice of the delay-time for harmonic attenuation.

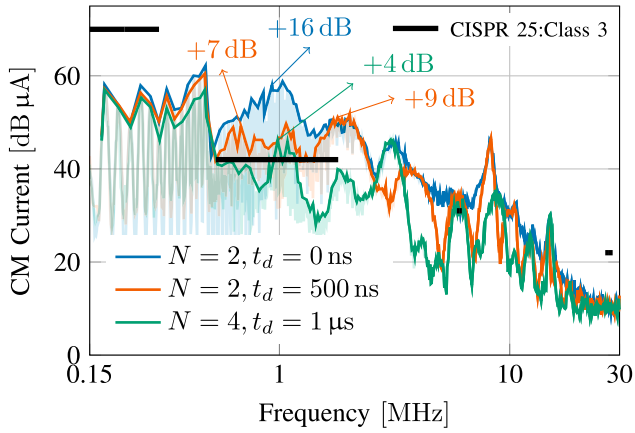


Fig. 11. Optimum common-mode emissions of the Q2L in comparison with 2L operation of the converter along with CISPR-25 Class 3 limits and the additional attenuation required for each operation. In the range of 1 MHz, the Q2L can provide significant attenuation with a reasonable delay time. This delay time can also be modified online to ensure optimum operation of the converter.

C. CISPR-25 Compliance

The optimum emissions of both the three-level and five-level operations are compared with the reference levels in CISPR-25: Class 3 [24] in Fig. 11. CISPR-25 provides various limits depending on the type of equipment and the affected bands, with corresponding limit values. This comparison is not intended as a compliance check; rather, it shows the attenuation that can be achieved with a Q2L converter if the limits are known for certain bands.

It can be observed that the 2L operation would require a 16 dB reduction in harmonic amplitude at 1 MHz. This requirement decreases by 7 dB for the three-level operation and 12 dB for the five-level operation. This allows for a much smaller filter size since the size of the filter directly depends on the attenuation required at a certain frequency band. Furthermore, in practice the impedances can change in complex systems due to the addition of various equipment in these DC-buses. The Q2L allows the low-emission band to be shifted online, unlike passive filters which need to be manually inserted in the system (unless more complex active filters are employed). This is an advantage of the Q2L over conventional 2L operation in terms of the harmonic performance, in addition to the better performance due to the low-voltage semiconductor devices employed.

D. Q2L Harmonic Model for Common-Mode Emissions

The harmonic model presented in (13) can also be applied to common-mode emissions. This is valid since the system has only one common-mode voltage source and the impedance is constant, thus, the common-mode currents should also scale according to the factor in (13) as per (18)

$$I_{CM}(f) = \frac{V_{CM}(f)}{Z_{CM}(f)} \tag{18}$$

where $I_{CM}(f)$, $V_{CM}(f)$ and $Z_{CM}(f)$ are the common-mode current, voltage and impedance corresponding to a particular frequency f. The result of the model can be observed in Fig. 12.

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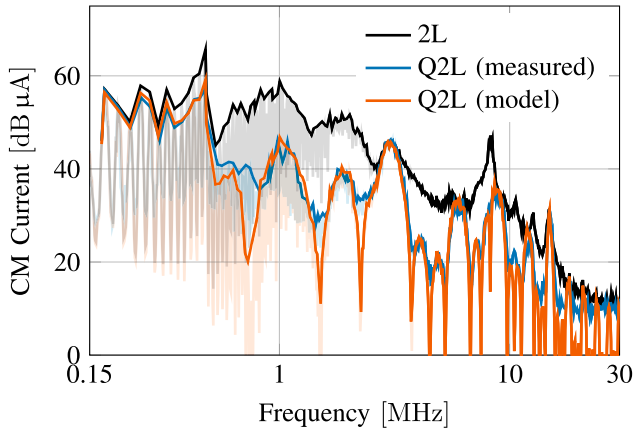


Fig. 12. Comparison of the model in (13) with the measurement for the same operating point. The reference 2L waveform utilised in the model is also shown. It can be observed that the envelopes of the model and measurement correlate well except for the zero harmonic amplitude bands. This is because the hardware prototype does not have perfectly symmetrical turn-ON/OFFS and thus, the harmonics do not perfectly cancel out which is evident in the comparison.

Although the model is an approximation, it predicts the envelope of the Q2L quite accurately. The main issue is the zero harmonic amplitude bands, which are not truly zero due to imperfect cancellation of the voltage harmonics in the hardware prototype. To make the model work better, one option is to introduce a floor of -20 dB relative to the harmonic peak, which can help compensate for this effect.

Overall, the model can be used for rapid analysis of the impact of a Q2L converter on the common-mode emissions in a system. In more complex systems, it is essential to model the common-mode impedances using different techniques such as those presented in [29], [30], [31], [32]. Using the common-mode impedances, the effect of Q2L can be incorporated into the inverter's CMV source using (13), and the resulting common-mode currents can be predicted (18). This allows for the superposition of multiple CMV sources and their combined effect on the common-mode current.

VI. Future Outlook

This work has primarily focussed on the harmonic performance of the Q2L in comparison with the 2L. However, there is quite some scope for further research that are listed below.

1) In this study, we benchmarked the hardware for common-mode currents and their mitigation. However, the same can also be applied to study the impact of Q2L on the insulation of machines and further build upon [10].
2) Validation of the approximation for Selective-Harmonic elimination based methods can be useful for implementation of Q2L in motor drives.
3) The Q2L fits in between the 2L and the ML converters in several parameters as shown in Table III. However, a comprehensive benchmark of the Q2L with 2L and ML converters in terms of efficiency and power density while including the filter volume is an important direction to identify the overall impact of Q2L.

TABLE III
Comparison of 2L, Q2L, and ML With Constant Current THD

Parameter	2L	Q2L	ML
Carrier Frequency	f_c	f_c	f_c/N for PSCPWM
Harmonic mitigation	N.A.	Eliminated as per (16)	Reduced by$(3 \times N)$dB
FC voltage ripple	N.A.	$\propto t_d$ [Order of ns]	$\propto 1/f_c$ [Order of kHz]

4) The Q2L with staggered switching can be used as a building block for so-called CMV elimination techniques. With the relatively shorter steps in comparison to a 2L bridge, the common-mode currents caused due to misalignment in such methods can be mitigated.
5) Since the Q2L modifies the harmonics in the so-called EMI spectrum, spread-spectrum based techniques can be used to additionally modify the supraharmonics of the converter.

VII. Conclusion

This work quantified how a quasi-two-level (or Q2L) operation shapes the output-voltage spectrum and common-mode voltage of motor-drive inverters. A simplified harmonic model was derived that maps any two-level voltage spectrum to its Q2L counterpart via a delay-dependent scaling, with a finite-$^{\mathrm{d}v}/_{\mathrm{d}t}$ extension. The study shows that the proposed model is accurate in practice when $t_d f_c \lesssim 0.1$, enabling rapid benchmarking with 2L converters.

Hardware results on a flying-capacitor multilevel inverter validated the analysis: introducing inter-cell delay and increasing the number of switching cells N created tunable attenuation bands in the low-MHz range and yielded measured reductions of up to $\sim$12 dB around $\sim$1 MHz. Importantly, Q2L does not raise/lower the pre-corner frequency peak amplitudes, rather, it redistributes energy and introduces zero harmonic amplitude bands whose locations scale with N and t_d, indicating potential to shrink common-mode filters when complying to applicable standards for a given application.

From these results, practical guidance follows:

1) keep $t_d f_c \lesssim 0.1$ for model fidelity and acceptable flying-capacitor ripple;
2) tune t_d so that the zero harmonic amplitude bands align with frequencies where the system CM impedance is low;
3) use higher N for extracting better performance from semiconductors with lower blocking-voltage and obtain additional harmonic attenuation at certain intermediate frequencies between the zero harmonic amplitude bands; and
4) account for finite (and possibly asymmetric) rise/fall times and dead time, which affect the corner frequency and lead to imperfect cancellation at the zero harmonic amplitude bands.

Overall, the approach offers a lightweight means to co-optimise modulation and hardware for EMI in weight/volume-constrained drives. Future work will validate the model for

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alternative modulation schemes, and couple it with identified CM impedance networks for complex installations.

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