29.2 A Cryo-CMOS Controller with Class-DE Driver and DC Magnetic-Field Tuning for Color-Center-Based Quantum Computers

Luc Enthoven*[1], Niels Fakkel*[1], Hans Bartling[2], Margriet van Riggelen[2], Kai-Niklas Schymik[2], Jiwon Yun[2], Eftychia Tsapanou Katranara[2], René Vollmer[2], Tim Taminiau[2], Fabio Sebastiano**[1], Masoud Babaie**[1]

[1]Delft University of Technology, Delft, The Netherlands, [2]QuTech, Delft, The Netherlands
*Equally Credited Authors (ECAs); **Equally Credited Authors (ECAs)

2024 IEEE International Solid-State Circuits Conference (ISSCC) | 979-8-3503-0620-0/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISSCC49657.2024.10454348

Color-center quantum bits (qubits), such as the Nitrogen-Vacancy center (NV) in diamond, have demonstrated entanglement between remote (>1.3km) qubits and excellent coherence times [1], all while operating at a few Kelvins. Compared to other qubit technologies typically operating at mK temperatures, the higher operating temperature of NVs enables scalable 3D integration with cryo-CMOS control electronics [2], provides significantly more cooling power, and removes the interconnect bottleneck between the qubits and the electronics in prior art [3-5]. Yet, no cryo-CMOS controller for NV-based quantum computers (QC) has been demonstrated.

In a scalable NV-based QC (Fig. 29.2.1), a chip hosting the NV qubits and the photonic circuitry is 3D-integrated with a cryo-CMOS chip [2]. A permanent magnetic field (B_0) biases the qubits and roughly sets the qubits' Larmor frequency (f_0). In this scheme, optical signals with waveguides are used for initialization, readout, and entanglement, whereas the cryo-CMOS controller drives the AC coil, generating oscillating magnetic fields perpendicular to B_0 for qubit control. Thanks to the NV's remote-entanglement capabilities, the qubits can be conveniently organized in identical unit cells that are kept small to maximize scalability, thus requiring corresponding area-efficient cryo-CMOS. With a ~1 mm spacing between unit cells, the crosstalk of neighboring NV's coils is negligible. Consequently, frequency spacing, i.e., FDMA, is not required, allowing each unit cell to operate at the same f_0, thereby reducing the total system complexity and power by sharing only a single frequency generator.

However, two main challenges must be addressed to realize this QC architecture: (1) compared to other qubits, the coils that couple the microwave signals to the qubits are further away, requiring significantly larger currents (>10mA$_{pk}$) from the AC controller, and (2) the inhomogeneity of the permanent magnetic field causes variability in f_0 (up to 20 MHz) among the unit cells, leading to inefficiency of the cryo-CMOS controller. This work addresses both challenges by (1) introducing a class-DE switching amplifier that delivers large currents to a low-impedance AC coil via a series resonator, and (2) compensating the inhomogeneity in f_0 (with an accuracy <16kHz) using a DC current regulator that locally tunes the DC magnetic field by driving a DC coil.

Since a large AC coil current enables fast qubit gates and the AC controller is very close to the qubits, 50Ω matching and load driving are omitted in this work. To maximize the generated AC magnetic field, a series resonant tank is preferred over its parallel counterpart (Fig. 29.2.2), as the inductor current is Q (resonator's quality factor) times higher for the same voltage across the driving transistor, which is limited by reliability. Therefore, a voltage-mode driver with a series resonant tank is chosen.

Using a typical class-D as a voltage-mode driver in the AC controller is inefficient, since the parasitic capacitances of the large transistors need to be charged and discharged each cycle, and crowbar currents may occur due to simultaneous conduction of switches (Fig. 29.2.2, top-right). A class-E topology would resolve the former problem by using the transistors' shunt capacitance to achieve zero voltage switching (ZVS). However, it requires a large choke inductor and its theoretical current efficiency, defined as the ratio of the coil current ($I_{coil,AC}$) to the driver DC supply current ($I_{driver,DC}$), is relatively low (~2.86). To improve the power and current efficiency, this work utilizes a class-DE topology, which drives the input of the amplifier with 25% duty-cycle pulses to avoid crowbar currents and uses the parasitic capacitance of the transistors together with added shunt capacitors $C_{S1,2}$ to achieve ZVS. Compared to class-D amplifiers, the shunt capacitors provide the coil current for 50% of the time, thus doubling its theoretical current efficiency to 2π. To control the qubit X/Y-gates, a 2b phase-demultiplexer selects the quadrature clocks generated from an external clock (f_{clk}), which are then converted to 25% pulses by a cascaded AND structure. The duration of qubit-gates is controlled by a 7b programmable counter running at $f_{clk}/2$.

To tune each qubit's Larmor frequency f_0, the DC current regulator in Fig. 29.2.3 locally adjusts the DC magnetic field by running a DC current ($I_{coil,DC}$ up to 10mA) through a low–resistance coil ($R_{coil,DC}$ ~1Ω) close to the NV. As the generated field is directly proportional to the current, the power dissipation can only be reduced by lowering the supply voltage. Using transistors in saturation (Fig. 29.2.3) would make the circuit robust against supply and $R_{coil,DC}$ variations, but would require excessive headroom. Transistors in triode would allow for a lower V_{DS} and hence require less power, but would suffer from worse supply rejection. As an alternative, this work uses a triode H-bridge supplied with a low voltage (~50mV), which is combined with a current regulation loop to achieve both robustness and low power dissipation.

The current I_{DAC} is mirrored from M_3 to $M_{4a/b}$. Although M_3 and $M_{4a/b}$ work in triode, the feedback loop consisting of A_{fb} and $M5_{a/b}$ ensures an accurate current ratio $I_{coil,DC}/I_{DAC}=W_{M4a/b}/W_{M3}$ by setting $V_{ref}=V_{set}$. Transistors M_3 and $M_{4a/b}$ are nominally sized for 1000× current gain, such that I_{DAC} can be generated with low current levels (0-12μA) without degrading noise performance. Limiting the infidelity due to detuning places tight requirements on the frequency accuracy (Δf_0<2kHz); hence, I_{DAC} is generated with a coarse ($IDAC_c$) and fine ($IDAC_f$) DAC to achieve LSB=420pA, as required in the future for strong coil-to-qubit coupling. Due to the larger mismatch at cryogenic temperatures (CT) [6], missing codes are prevented by range overlaps, which can be compensated during the start-up qubit calibration. Switches $M_{4a/b}$ are optimized for power, area, and noise, since a lower R_{on} contributes a lower voltage drop, but also increases the area and amplifies A_{fb}'s input-referred voltage noise. Finally, $M_{4a/b}$ and $M_{5a/b}$ set the polarity of $I_{coil,DC}$, thereby doubling the tuning range of f_0 for the same $I_{coil,DC}$.

To extend the output-current range, the voltage range at the gate of $M_{5a/b}$ is maximized by adopting a 2-stage folded-cascode with a rail-to-rail common-source output stage for A_{fb}. Chopper-stabilization avoids A_{fb}'s offset limiting the range of $I_{coil,DC}$ and 1/f noise affecting the qubit coherence. The resulting chopping ripple (250kHz) is reduced by trimming A_{fb}'s offset via a digitally selectable input pair, lowering the upmodulated offset, and by using a switched-capacitor notch filter (SC-filter) with a quadrature clock. All switches used for chopping and filtering are thick-oxide transistors, preventing improper mid-rail switching at CT due to increased V_{th}.

Both AC controller and DC current regulator have been fabricated in a 40nm CMOS process and characterized at room temperature (RT) and 4.2K (Fig. 29.2.4). A magnetic-field probe located ~20μm above an on-chip test coil ($L_{test,AC}$=2.28nH) in a cryogenic probe station measures the AC controller's performance. At 2.7GHz, the AC controller reaches a magnetic flux density of 2.17 (2.05)G, corresponding to an extrapolated current $I_{coil,AC}$ of 30.7 (28.9)mA$_p$, while $I_{driver,DC}$ is 10.7 (13.4)mA from a 1.1V supply at 4.2K (RT). Over the 2.6-to-3.0GHz range, an SNR of >47 (>48)dB for a 5MHz bandwidth is achieved. The DC current regulator is characterized using a dipstick setup with liquid helium. $I_{coil,DC}$ is measured on an external resistor $R_{coil,DC}$=1Ω with $V_{H\text{-}bridge}$=50mV and V_{DD}=1.1V. The DC current regulator, including the H-bridge, dissipates 906 (812)μW with chopping enabled and can set currents up to 12.5 (10.5)mA at 4.2K (RT). The PSD at 10Hz improves from 2400 (460)fA^2/Hz to 305 (25)fA^2/Hz when activating chopping, while $I_{coil,DC}$ has a DC PSRR of -87.4 (88.5)μA/V versus $V_{H\text{-}bridge}$ and 297 (58)μA/V versus V_{DD}.

To demonstrate functionality, the cryo-CMOS chips have been integrated with a NV center qubit (Fig. 29.2.7). The ensemble is placed in a Montana cryostat with optical access and cooled to <4.5K. Permanent magnets bias the qubit at f_0=2.66GHz. Two thin gold coils, L_{AC} and L_{DC}, are patterned on diamond: L_{AC} (~2.4nH) is directly bonded to the AC controller, whereas L_{DC} is bonded to a bias-T, which combines the signals from the DC current regulator and the RT electronics, used for comparison. Fig. 29.2.5 shows a Rabi oscillation using both the RT setup and the AC controller, both yielding similar results. The Rabi frequency (f_R) of the AC controller is plotted versus the driver's DC supply current and shows that a maximum f_R=2.5MHz can be achieved with $I_{driver,DC}$=6.5mA. In this case the entire AC controller consumes 16.8mW. The DC current regulator achieves a tuning range of +/-8MHz for f_0 using currents up to 20mA with $V_{H\text{-}bridge}$=100mV, increased to compensate for the larger $R_{coil,DC}$ due to the bias-T. Lastly, by using both chips, and keeping the driving frequency of the AC controller fixed, f_0 is calibrated for the maximum contrast of the Rabi oscillation by sweeping the DC-regulator's digital input (D_{DC}), highlighting the functionality of the proposed system.

Compared to state-of-the-art cryo-CMOS controllers (Fig. 29.2.6), the cryo-CMOS controller is the first targeting color centers, with the AC controller demonstrating a more effective way of generating high AC current levels with respect to prior cryo-CMOS controllers, and with no comparable work for the DC current regulator to the authors' knowledge. Although 3D integration will facilitate further power savings by reducing the parasitic losses and improving the coil-to-qubit coupling, the reported experimental performance combined with the few-Watt cooling power readily available in 4K refrigerators enables the cryo-CMOS control of hundreds of unit cells, thus advancing scalable color-center-based quantum computers.

Acknowledgement:
We would like to thank Fujitsu Limited for funding; Z. Y. Chang from TU Delft; N. Alberts, R. Robe, T. Hiep, J. Mensingh and O. Benningshof from Qutech.

References:

[1] S. Pezzagna et al., "Quantum computer based on color centers in diamond," *Applied Physics Review*, Feb. 2021.
[2] R. Ishihara et al., "3D Integration Technology for Quantum Computer based on Diamond Spin Qubits," *IEDM*, Dec. 2021.
[3] J. Yoo et al., "34.2 A 28-nm Bulk-CMOS IC for Full Control of a Superconducting Quantum Processor Unit-Cell," *ISSCC*, pp. 506-507, Feb. 2023.
[4] D. J. Frank et al., "A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology," *ISSCC*, pp. 360-361, Feb. 2022.

Authorized licensed use limited to: TU Delft Library. Downloaded on March 26,2024 at 12:01:29 UTC from IEEE Xplore. Restrictions apply.

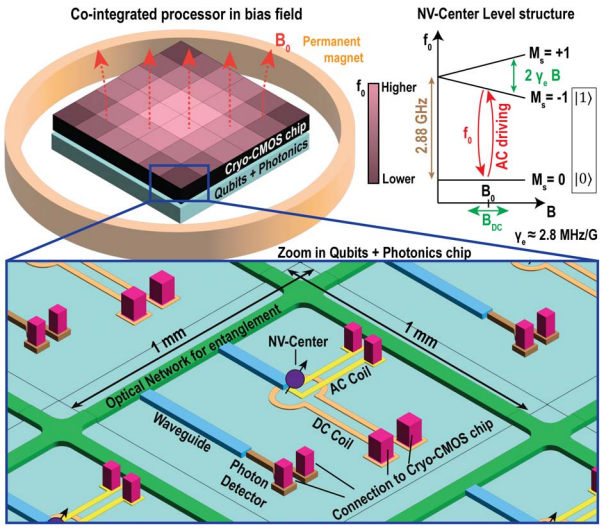


Figure 29.2.1: Modular quantum computer based on NV-centers with AC and DC coils connected to the 3D-integrated cryo-CMOS chip. The inhomogeneity of the permanent magnetic field B_0 (top-left) induces a shift in the Larmor frequency f_0 (top-right) to be compensated in each individual module.

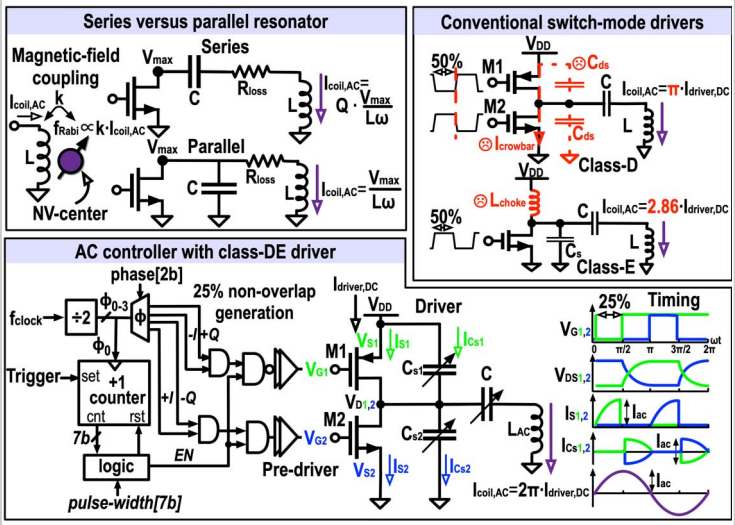


Figure 29.2.2: Comparison between series and parallel tank to maximize coil current (top-left); Issues associated with class-D and class-E switched-mode amplifiers (top-right); Block diagram of the AC controller, including the proposed class-DE current driver and its waveforms (bottom).

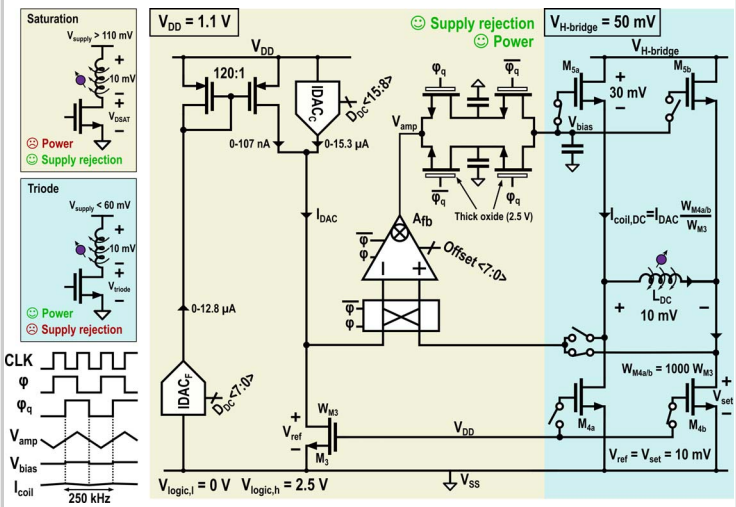


Figure 29.2.3: To tune the qubit Larmor frequency f_0, the DC current regulator exploits a triode-biased H-bridge and a chopped regulation loop to achieve low power and robustness to supply variation. For the H-bridge, voltage drops for $I_{coil,DC}$=10mA, R_{coil}=1Ω and R_{4b} =1Ω are annotated.

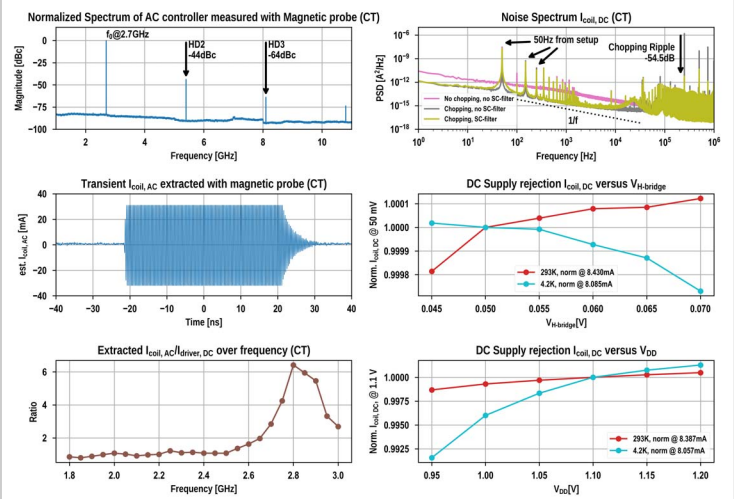


Figure 29.2.4: Measured spectrum of $I_{coil,AC}$, $I_{coil,AC}$ transient waveform and $I_{coil,AC}/I_{driver,DC}$ over frequency of the AC controller at cryogenic temperature (CT) (left); Measured PSD of $I_{coil,DC}$, supply rejection of $I_{coil,DC}$ versus $V_{H\text{-}bridge}$ and V_{DD} of the DC current regulator at CT (right).

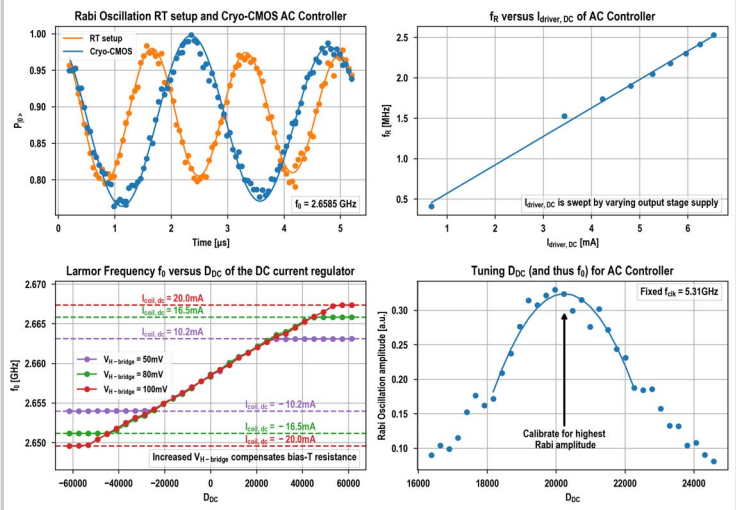
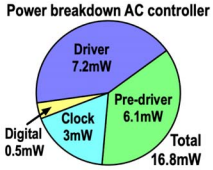


Figure 29.2.5: Rabi oscillation (top-left); Rabi frequency (f_R) vs driver DC current ($I_{driver,DC}$) of the AC controller (top-right); Tuning of Larmor frequency (f_0) with DC current regulator (bottom-left); Using both chips, calibrating f_0 for largest Rabi oscillation amplitude by sweeping D_{DC} (bottom-right).

AC controllers	This work	[3] ISSCC 2023	[4] ISSCC 2022	[5] ISSCC 2021	Patra et al. ISSCC 2020	RT electronics
Qubit type	NV	Transmon	Transmon	Spin	Spin & Transmon	NV
Qubit temperature	4.5 K	20 mK	20 mK	20 mK	20 mK	4.5 K
Impedance [Ω]	<1	50	50	50	50	50
Cryo-CMOS temp. [K]	4.5	3	3	3	3	N.A.
AC driver Class	DE	A(B)†	A(B)†	A	A	A
Frequency range [GHz]	2.6-3	4-8	4.5-5.5	11-17	2-15	0.7-6
Maximum I_{AC} [mAp]	30.1	N.A.	0.6*	4.0*	1.1*	1000
SNR [dB]	>47	N.A.	N.A.	>44	48	N.A.
Rabi frequency [MHz]	2.5	91‡	23.5‡	N.A.	1.2	>50
Active Area [mm²]	0.092	7#	1.6	~4	4	N.A.
Technology	40-nm Bulk	28-nm Bulk	14-nm FinFET	22-nm FinFET	22-nm FinFET	N.A.
Power per qubit under active control	16.8 mW	<4 mW	23 mW	90 mW*∞	192 mW*	>200W

DC current regulator	This work	
Ambient temperature [K]	4.2	300
I_{range} [mA] (R_{coil} = 1 Ω)	± 12.5	± 10.5
I_{step} [nA]	310	341
DC PSRR $V_{H\text{-}bridge}$ [µA/V]	-17.5	167.7
DC PSRR V_{DD} [µA/V]	297	58
PSD @10Hz [pA²/Hz]	0.46	2.40
Active Area [mm²]	0.13	
Technology	40-nm Bulk	
Total Power P_{tot} [µW]	906	812
$P_{H\text{-}Bridge}$ (50mV) [µW]	625	525



†Derived from schematic, depends on bias point
* Assuming P_{out} with 50Ω
‡ Based on reported gate duration
# Active area not explicitly mentioned
▾FDM allows simultaneous control of 2 qubits
∞Estimated

Figure 29.2.6: Benchmark of the proposed AC controller with prior art, and performance of the DC current regulator.

Authorized licensed use limited to: TU Delft Library. Downloaded on March 26,2024 at 12:01:29 UTC from IEEE Xplore. Restrictions apply.

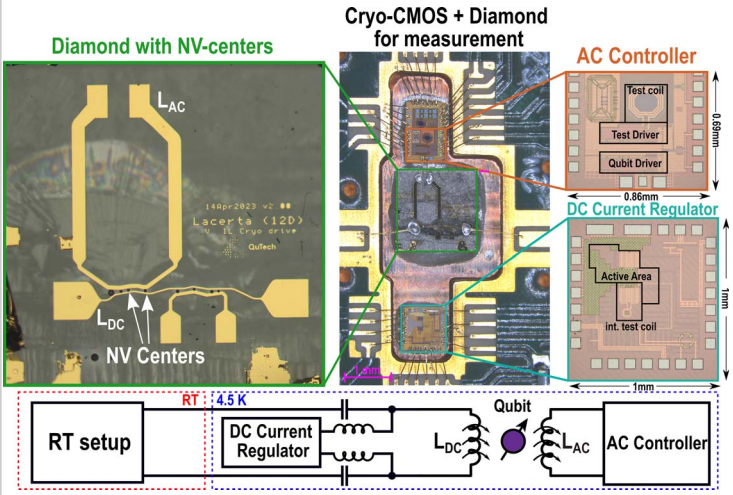


Figure 29.2.7: Integrated Cryo-CMOS and diamond sample used for qubit measurements. Two striplines, L_{DC} and L_{AC}, are used; L_{DC} is bonded to a bias-T, which combines the DC current regulator with RT electronics, used for comparison; L_{AC} is directly bonded to the AC driver.

Additional References:
[5] J. S. Park et al., "A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22nm FFL FinFET technology," *ISSCC*, pp. 208-209, Feb. 2021.
[6] P. A. Hart et al., "Characterization and Modeling of Mismatch in Cryo-CMOS," *JEDS*, pp 263-273, Feb. 2020.

Authorized licensed use limited to: TU Delft Library. Downloaded on March 26,2024 at 12:01:29 UTC from IEEE Xplore. Restrictions apply.

979-8-3503-0620-0/24/$31.00 ©2024 IEEE