TU Delft

A CLASS-D AMPLIFIER ARCHITECTURE TO COMPENSATE FOR THE INSTABILITY PROBLEM DUE TO THE LC FILTER VARIATION

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Zhuohui Fu: A Class-D amplifier architecture to compensate for the instability problem due to the LC filter variation (2022)

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Abstract **- Class D audio amplifier is widely used in many electronic applications such as automobiles, laptops, and mobile phones. However, electromagnetic interference (EMI) generated by Class-D audio amplifiers frequently requires an external LC filter for suppression. The LC filter itself causes significant nonlinearity. Hence, feedback after LC is widely used to suppress this nonlinearity. Nevertheless, component tolerance in practical LC components causes instability problems in the feedback-after-LC Class-D amplifier. This thesis presents a class-D amplifier that suppresses LC filter nonlinearity by 40 dB at least and calibrates the variation of the cut-off frequency (f_{LC}) of the LC filter between 70kHz and 200kHz. This is implemented in a differential architecture, where the inner loop and outer loop ensure high in-band loop gain and stability, and the unity gain frequency is calibrated by a variable gain amplifier (VGA). This circuit is built in the 180-nm BCD process, achieving -108dB~-126dB total harmonic distortion (THD) after compensating for different LC cut-off frequencies.**

Index Terms **– Class-D amplifier, feedback-after-LC filter, LC filter calibration, nonlinearity compensation, total harmonic distortion (THD).**

Contents

1. Introduction

1.1 Class-D Amplifier

Class-D amplifiers (CDAs), as shown in Fig. 1, are amplifiers in which the output stages operate as switches, and not as linear gain devices as in other amplifiers. The pulse-width modulator processes the input audio and triangle wave to generate a switching waveform, and the switching waveform is filtered by an LC filter to drive the loudspeaker. CDAs can achieve high efficiency (usually up to 90% or higher) since the output transistors are switching in the linear region. Moreover, the LC filter ideally has no power dissipation. Hence, the main power losses are due to the on-resistance and gate charge of the output driver, and transition loss. Therefore, the CDA is widely used in many electronic applications such as automobiles, laptops, and mobile phones.

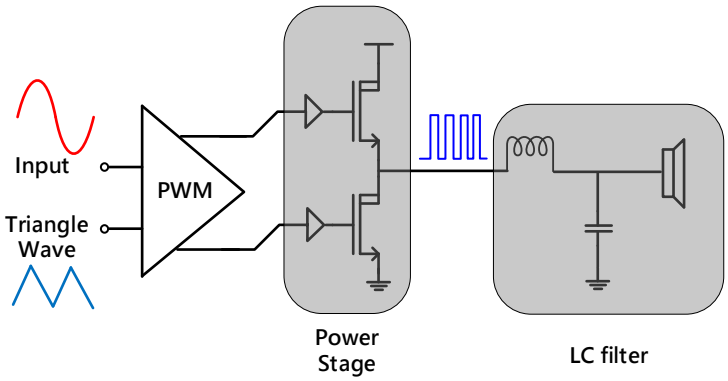

Fig. 1. Block diagram of a basic class-D amplifier.

Although CDAs are superior to linear amplifiers in terms of power efficiency, the output stage often suffers from distortion due to non-ideal switching due to deadtime, finite rise/fall time, and power efficiency. Moreover, they often require an external LC filter to filter out the high-frequency components due to switching to meet certain electromagnetic interference (EMI) standard [1].

To suppress the distortion and supply sensitivity of the output stage, a feedback-before-LC filter CDA can be used [16], as shown in Fig. 2. The nonlinearity of the output stage is suppressed by the loop filter with a high loop gain.

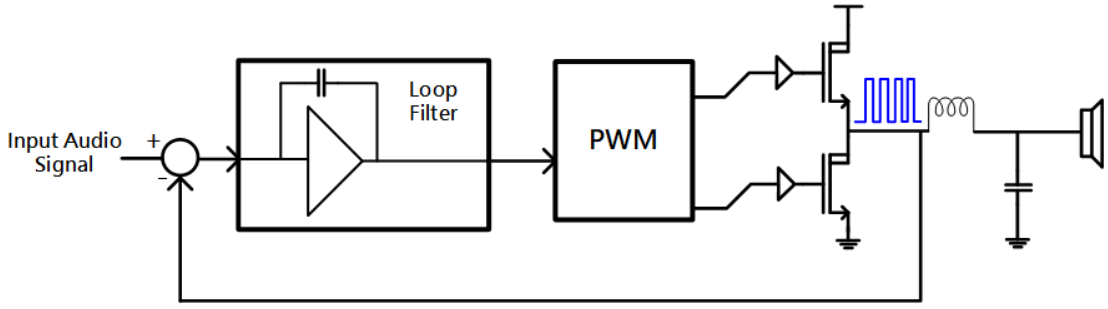

Fig. 2. The block diagram of feedback before LC filter CDA.

1.2 LC filter nonlinearity

However, the LC filter also causes significant nonlinearity to the CDA because of the nonlinearity of capacitors and inductors, including LC filter components' DC bias dependency. According to [2], the distortion of inductors and capacitors can be modeled by the equation (1) and (2) [2] respectively:

$$THD_L \sim \frac{f_{IN}}{f_{LC}} \cdot \frac{P_{out}}{6R_L I_{SAT}^2} \tag{1}$$

$$THD_C \sim \left(\frac{f_{IN}}{f_{LC}}\right)^2 \cdot \frac{P_{out} R_L}{2V_{SAT}^2} \tag{2}$$

where f_{LC} is the cut-off frequency of LC filter, f_{IN} is the input frequency, P_{out} is the output power, R_L is the load resistor, I_{SAT} is the saturation current of the inductor and V_{SAT} is the saturation voltage of the capacitor.

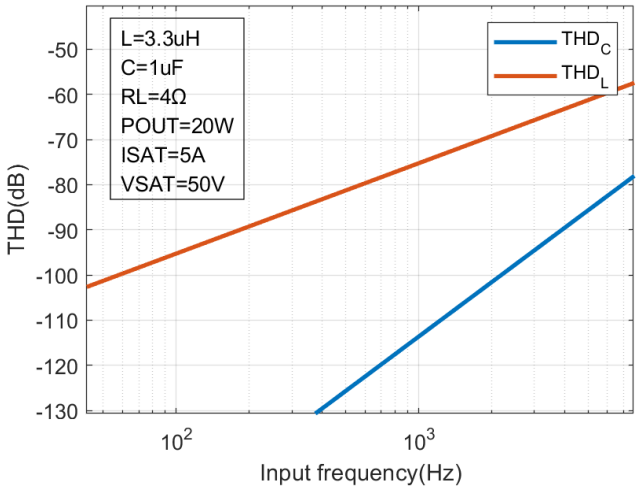

Fig. 3. The THD of inductors and capacitors versus input frequency

Based on these two equations, the plots of THD versus the input frequency are shown in Fig. 3. It is obvious that the distortion of inductors contributes most and I_{SAT} dominates the nonlinearity of inductors due to the square term. Furthermore, when the saturation current is only 3.6A (the peak output current), the THD is only -60dB. Hence, according to TABLE 1-I, the THD of each inductor is measured in [11], a very high-linearity LC filter is desired for CDAs, but high cost and large area become problems.

TABLE 1-I
Selected inductors for the CDAs

		
Part Number	7443340330	FDSD0420-H-3R3M=P3
Dimensions(mm)	8.4x7.9x7.2	4.2x4.2x2
Cost (each)	€2.14	€0.5
THD	-102dB	-60dB

Source: Farnell

1.3 LC filter nonlinearity suppression

The practical inductance and capacitance vary with respect to DC bias which causes nonlinearity. To suppress the nonlinearity, the negative feedback after LC filter CDAs are proposed [5]-[10]. At the first glance, the feedback point can be moved from the input of the LC filter to the output of the LC filter as shown in Fig. 4. The LC filter is incorporated in the feedback loops. Hence, the nonlinearity of the LC filter is suppressed by the loop filter.

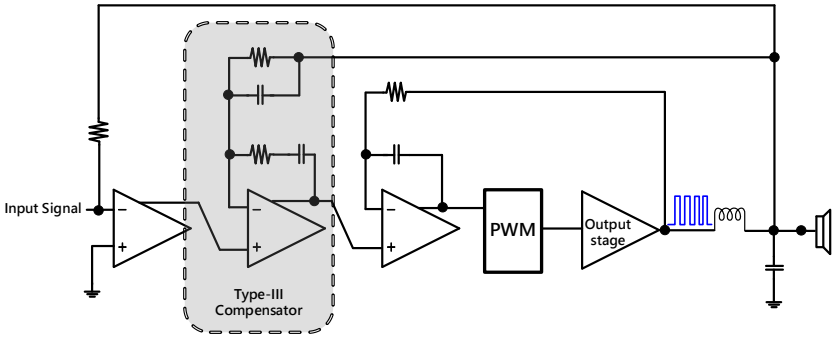

Fig. 4 The block diagram of feedback after LC filter CDA [18]

However, the LC filter introduces two complex poles, causing 180 degrees phase shift. Together with the pole introduced by the integrator, the loop will not be stable. To make the loop stable, the type-III compensator is implemented in the loop filter [18]. Nevertheless, the loop unity gain frequency would depend on the LC cut-off frequency. Since there are manufacturing tolerance and DC bias dependencies on the practical inductors and capacitors, the LC filter cut-off frequency can deviate from a nominal value and may push the unity gain frequency of closed-loop CDAs above $\frac{f_{PWM}}{\pi}$ (switching frequency), leading to instability in a single feedback path after the LC filter [2].

1.4 Prior Arts Feedback-after-LC architectures

For fixed PWM frequency CDAs design, there are basically two types of feedback-after-LC CDAs: digital feedback and analog feedback loop. Reference [3] proposes a digital feedback structure, as shown in Fig. 5.

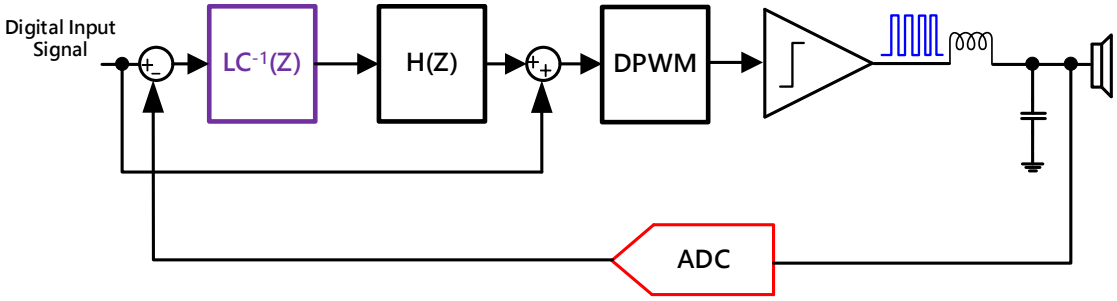

Fig. 5. The block diagram of digital feedback after LC filter CDA [3]

A fifth-order digital loop filter is implemented to achieve over 50dB loop gain around the LC filter at 20kHz. In this structure, a second-order LC compensation filter is used to cancel the LC filter's poles to maintain stability. However, the ADC in this architecture is sensitive to latency and needs high performance. Also, the mismatch between the LC filter and the LC compensation filter affects the stability of the whole loop, especially for a small unity gain frequency (100kHz). Hence, the digital filter coefficients need to be calibrated for each LC filter.

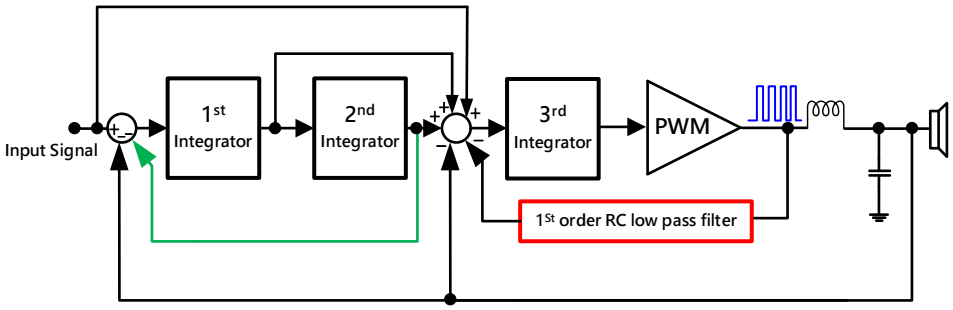

Fig. 6. The block diagram of feedback after the LC filter with inner loop feedback before the LC filter CDA [4]

Paper [4] proposed the analog feedback-after-LC architecture, shown in Fig. 6. This architecture uses the inner loop to stabilize ±30% variation of LC filter concerning DC bias dependencies of practical inductors and capacitors and manufacturing tolerance. According to Table 1-I, one -60dB-THD inductor is used in the LC filter, so to achieve -100dB THD at LC output, at least 40dB loop gain around the LC filter at 20kHz is required to suppress this nonlinearity. The outer loop implements a resonator thanks to the local feedback highlighted in green, to boost the loop gain. In this structure, 1.2MHz loop bandwidth is achieved, enabled by a 4.2MHz PWM frequency.

1.5 Proposed foreground calibration

However, ±30% tolerance of the LC filter in [4] is insufficient for the variation of capacitors and inductors, taking into account manufacture tolerance and component variations due to dynamic factors such as temperature and DC biasing. Hence, this thesis proposes a foreground calibration approach to compensate for the LC variation due to manufacturing tolerance. Therefore, the ±30% tolerance can be used to adapt to the dynamic LC variations. The circuit first measures f_{LC}, and then VGA is adjusted to compensate for the variation of the LC filter. In this design, f_{LC} calibration range is 70~200kHz, while the target THD is below -100dB. The details regarding the calibration are given in the following sections.

According to datasheets, the typical manufacturing tolerance of 3.3μH inductors and 1μF capacitors are ±30% and ±10% respectively. This tolerance has ±26% variation on f_{LC} of the LC filter. Hence, this variation already consumes 87% tolerance of the inner loop (±30%). Besides, DC dependencies of the inductors and capacitors are -12% and -25% respectively, which has +a 24% variation on f_{LC}. As a result, DC dependency and manufacturing tolerance can make the loop unstable. Hence, it is necessary to calibrate the manufacturing tolerance of capacitors and inductors. According to the manufacturing tolerance in TABLE 1-II we calibrate 70kHz~124kHz f_{LC} range in our design. In addition, to extend the tolerance capability of the circuit as much as possible, we eventually chose 200kHz f_{LC} as the upper bound considering the instability problem, which will be explained in Section II. When f_{LC} goes lower, the VGA gain error will exceed the requirement which will be explained in Section II. Therefore, a 70kHz lower bound is chosen in our design consideration. The consideration for the calibration range is illustrated in the following section.

TABLE 1-II

Selected Inductors for the Class-D amplifier

Inductors	XAL1010-332MED	FDSD0420-H-3R3M=P3
Dimension (mm)	10 x 10 x 11.3	4 x 4 x 2
I_{sat}	**27.4A**	**3.7A**
Cost	€ 5,62	€0.66
DC dependency(3A)	**-3%**	**-12%**
Manufacturing tolerance	**±20%**	**±30%**
THD	**/**	**-60dB**

TABLE 1-III

Selected Capacitors for the Class-D amplifier

Capacitor	CGA8P3X7T2E105K250KA	C0805C105K3RACTU	GRM21BR71C105KA01
Dimension (mm)	**4.5x3.5x2.5**	**2x1.25x1.25**	**2x1.25x1.25**
Voltage Rating DC	**250V**	**25V**	**16V**
Cost	€ 1,20	€0.204	€0.19
DC dependency(14.4V)	**-1%**	**-25%**	**-25%**
Manufacturing tolerance	**±10%**	**±10%**	**±10%**

Source: Murata

In this thesis, based on TABLE 1-II and 1-III and the above illustration, f_{LC} varies ±24% due to DC dependency, and [4] can tolerate ±30%. As a result, the total error of calibrating f_{LC} should be kept below ±6%. Such that the ±30% variation tolerance offered by [4] can be sufficient for the dynamic variations of the LC. In addition, the inaccuracy requirement for f_{LC} measurement is ±3% and for VGA gain is ±3%.

In our design, we will perform a foreground calibration to detect the LC filter cut-off frequency, and according to this information, we then vary the loop filter design such that the CDA will be stable for the actual f_{LC}. The targeted calibration range is 70kHz ~ 200kHz f_{LC}. Moreover, to ensure good LC filter nonlinearity suppression, sufficient loop gain must be obtained. Based on TABLE II, a loop gain around the LC filter of 40dB is needed to achieve -100dB THD.

The output stage used in this work is based on that proposed in [4], as shown in Fig. 7. It is a 3-level H-bridge, and each half-bridge can produce 3 output levels: PVDD, PVDD/2, and PVSS. In phase 1, M8, M5, M1 and M3 are turned on resulting in PVSS output. In phase 2, M6,M7, M2 and M4 conduct to give PVDD output. In phase 3, M1~M4 are on to output half PVDD. The advantage of this output stage compared to a 2-level output stage is significant EMI reduction by introducing the extra output level. The load capacitor C_{CM} of the voltage regulator changes oscillation frequency. Hence the ratio of the capacitor is obtained by measuring the charging time. This is illustrated in Section II. f_{LC} deviations are calibrated by VGA. The corresponding VGA gains can fix the zero frequency provided by the inner loop, therefore ensuring the unity gain frequency is robust to manufacturing tolerance.

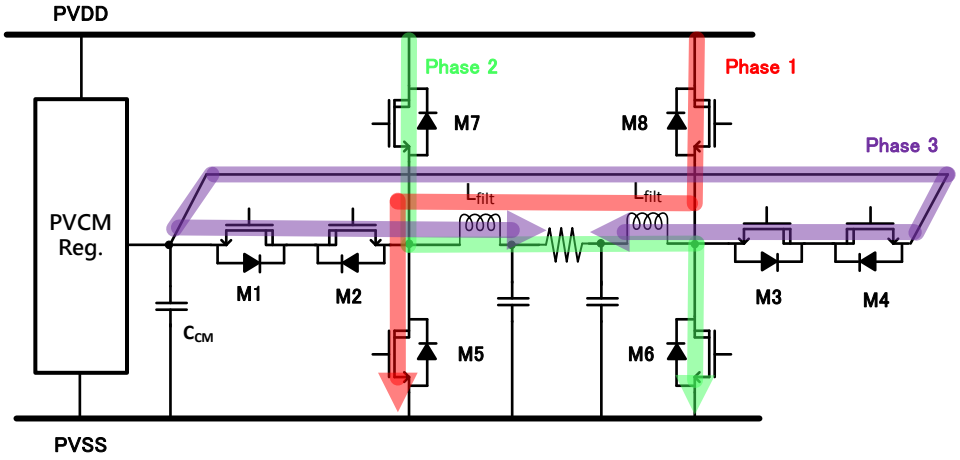

Fig. 7. Circuit topology of the output stage.

This thesis is organized as follows. Section II illustrates the system-level design and the entire calibration operation of this architecture. Section III describes the circuit implementation. Section IV presents simulation results, and Section V gives conclusions.

2. Architecture Overview

This thesis is based on a prior design which will be described first, followed by the proposed CDA design.

2.1. Prior art feedback-after-LC CDA insensitive to the LC variation

2.1.1. Inner loop architecture

The feedback-after-LC architecture with an inner loop is shown in Fig. 8 [4], which consists of an inner loop and an outer loop. The inner loop incorporates the first-order RC low-path filter and bypasses the feedback loop FB_0 at high frequencies.

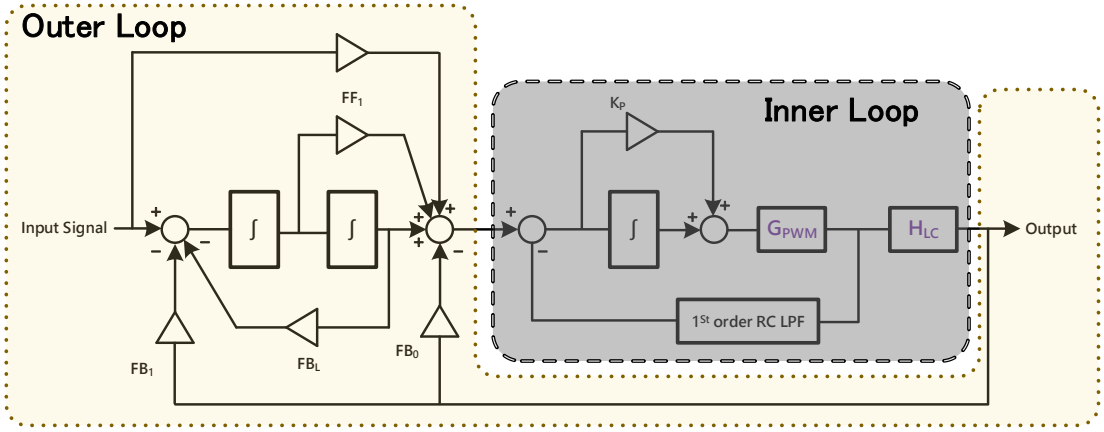

Fig. 8. Complete block diagram of the inner loop class-D amplifier. [4]

The inner loop has three primary functions. Firstly, it provides a zero to compensate for the LC filter 180 degrees phase shift, ensuring the stability of the whole loop. Secondly, it fixes the unity gain frequency around the output stage to meet the PWM stability criteria ($f_{UG}<\frac{f_{PWM}}{\pi}$) [2]. As shown in Fig. 9, it is the loop gain around the output stage under LC spread, the inner loop is highlighted in the green path. The third function is to suppress the output-stage nonlinearity by providing the loop gain, which makes THD lower than -100dB.

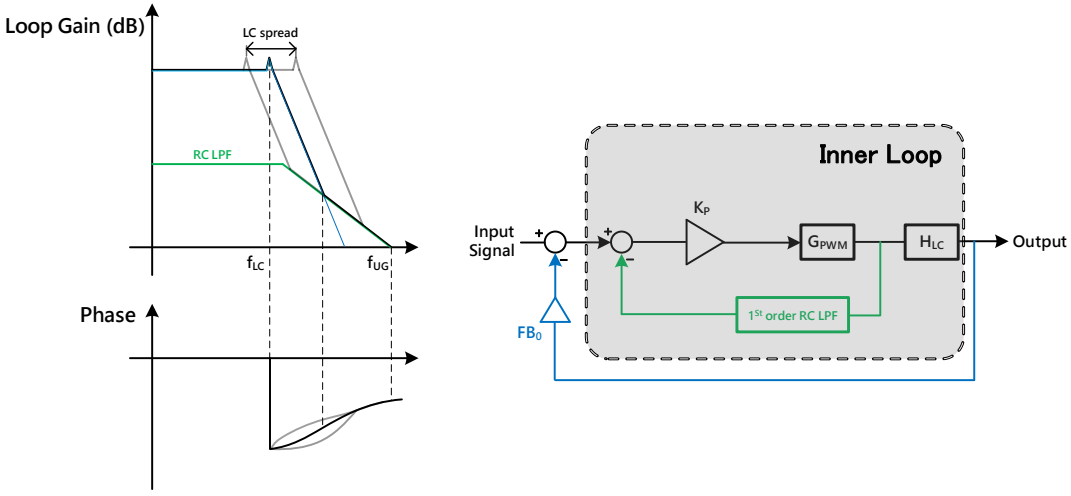

Fig. 9. Loop gain and phase around the output stage without the integral path

For simplicity, the integrator is ignored temporarily, as shown in Fig. 10, since it only 0affects the low-frequency part.

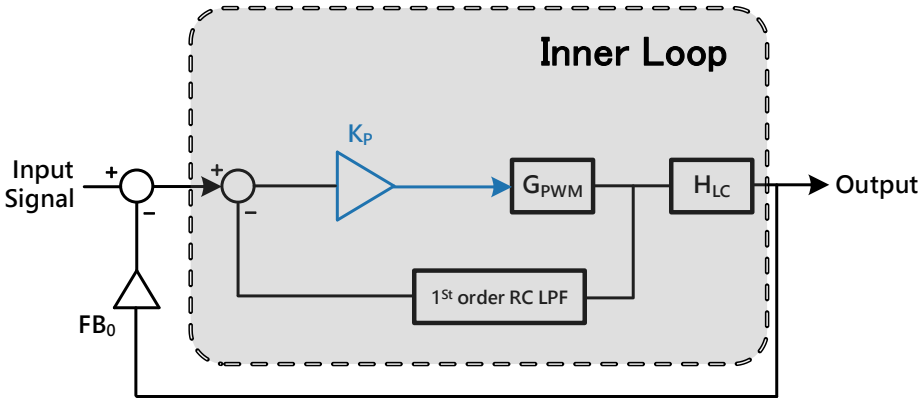

Fig. 10 Block diagram of the inner loop without integral path

Hence, the closed-loop gain of the inner loop can be expressed as follows:

$$H_{CL,inner}(s) = \frac{K_P \cdot G_{PWM}}{1 + H_{RC} \cdot K_P \cdot G_{PWM}} \tag{3}$$

where K_P is the proportional gain in the forward path, G_{PWM} is the equivalent gain of PWM and output stage (the ratio of power supply of output stage and peak amplitude of triangle-wave) and $H_{RC}(s) = (\frac{1}{1+\frac{s}{\omega_{RC}}})$ is the gain of RC 1st order path.

As a result, the unity gain frequency around the output stage is given by (4)

$$\omega_{UG} = 2\pi f_{UG} = K_P \cdot G_{PWM} \cdot \omega_{RC} \tag{4}$$

where $\omega_{RC}$is the corner frequency of RC first order path, f_{UG} is the unity gain frequency around the output stage. Hence, equation (3) can be re-written as equation (5):

$$H_{CL,inner}(s) = \frac{\omega_{UG}}{\omega_{RC}} \cdot \frac{s + \omega_{RC}}{s + (\omega_{UG} + \omega_{RC})} \tag{5}$$

We can find that the inner loop transfer function behaves as a lead compensator: a low-frequency zero ω_{RC} and a high-frequency pole $\omega_{UG} + \omega_{RC}$. The bode plot of the inner loop is shown in Fig. 11, which shows how the ω_{RC} influences the loop gain and phase shift. A higher ω_{RC} gives lower phase compensation but higher loop gain. Hence the closed inner loop can be used to compensate for the phase shift by the LC filter.

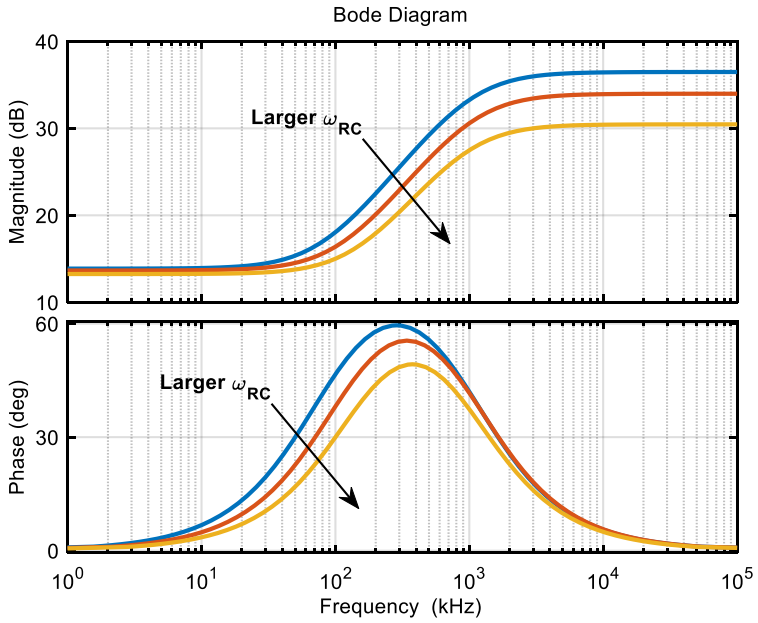

Fig. 11. Closed-loop gain of inner-loop

The loop transfer function around the LC filter is expressed as follows:

$$H_{outer}(s) = FB_0 \cdot H_{CL,inner}(s) \cdot H_{LC}(s) \tag{6}$$

where $H_{LC}(s)$ is the transfer function of the LC filter. Fig. 12 illustrates how the closed inner loop affects the loop gain and phase shift around the LC filter. From Fig. 12, the smaller ω_{RC} gives a higher closed inner loop gain. Hence there is a trade-off between the phase margin and in-band loop gain by changing ω_{RC} and FB_0. This is the first function of the inner loop.

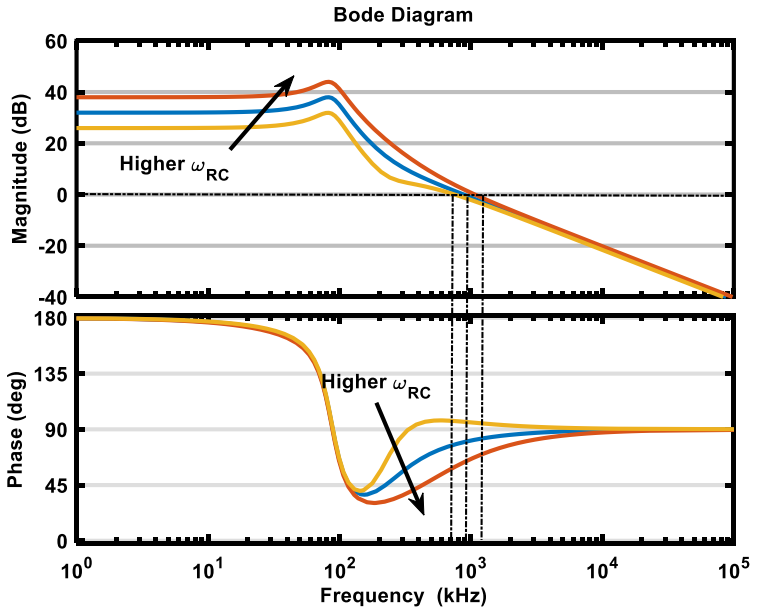

Fig. 12. loop gain around the LC filter with different ω_{RC}

Besides, the inner loop can suppress the nonlinearity around the output stage by implementing a proportion-integral path shown in Fig. 13, a proportional path and an integral path are in parallel, forming a dc pole and a high-frequency zero.

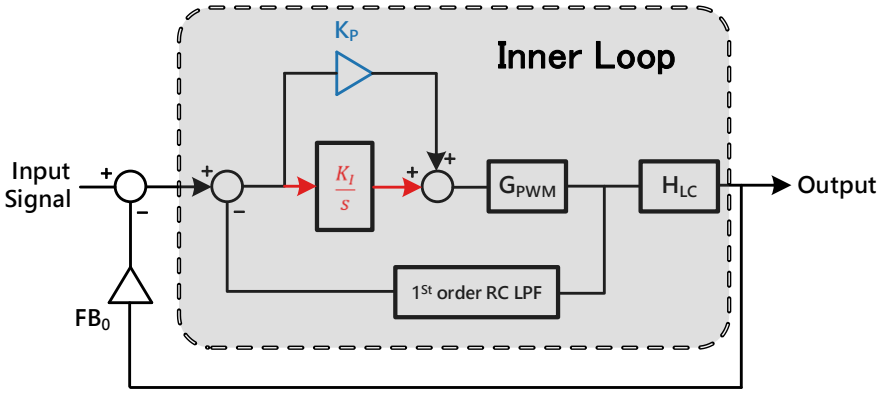

Fig. 13. Circuit diagram of the inner loop with integral path

Hence equation (3) can be expressed as follows:

$$H_{CL,inner}(s) = \frac{G_{PWM} \cdot H_{PI}(s)}{1 + G_{PWM} \cdot H_{PI}(s) \cdot H_{RC}(s)} \tag{7}$$

where $H_{PI}(s)$ is the transfer function of PI compensator $\frac{sK_P+K_I}{s}$. The zero in the PI path coincides with the pole in the RC first-order feedback path to ensure that there is no phase lag due to ω_{RC} and $\frac{K_P}{K_I}$. Hence equation (5) can be modified as follows:

$$H_{CL,inner}(s) = \frac{G_{PWM} \cdot (sK_P + K_I)}{s + G_{PWM} \cdot K_I} \tag{8}$$

The ω_{RC} is cancelled by the zero in the PI path. Hence the closed loop transfer function remains a lead compensator. Moreover, the RC components are the same type for ω_{RC} and PI path, which ensures that this pole-zero cancellation is not influenced by process corners and temperature. Then the unity gain frequency around the output stage is given by:

$$\omega_{UG} = 2\pi f_{UG} = K_I \cdot G_{PWM} \tag{9}$$

where K_I is the gain of the integral path. K_I consists of on-chip RC components, and the capacitor can be adjusted by one-time trim capacitors [11],[12]. As a result, the unity gain frequency is fixed and insensitive to the LC spread.

2.1.2. Outer loop architecture

The loop gain around the LC filter is insufficient with only the inner loop, as the close loop gain of the inner loop is still relatively low as shown in Fig.12. Hence, the outer loop provides 2 additional stages to boost in-band loop gain, as shown in Fig. 14 [4].

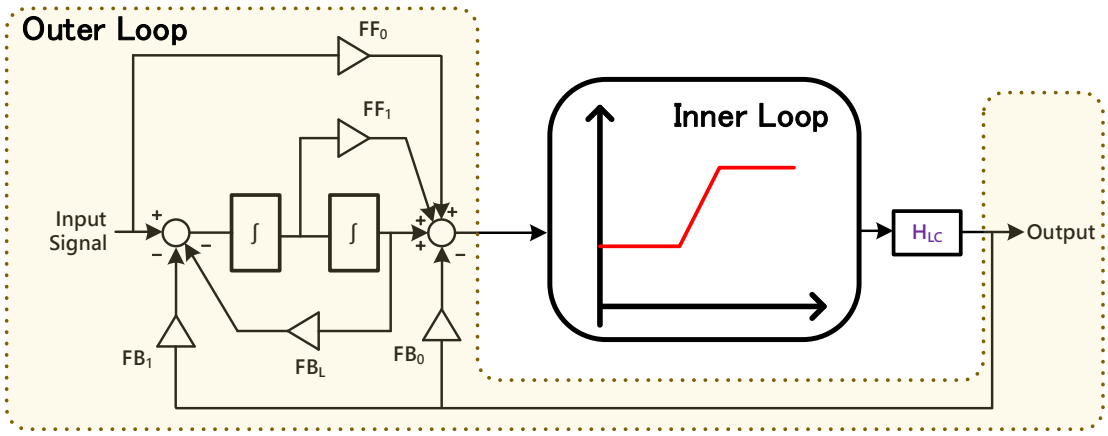

Fig. 14. Block diagram of the outer loop class-D amplifier.

The feedforward path FF_0 reduces the output swing of the second integrator and FF_1 reduces the output swings of the first integrator by feeding the output forward, and one zero is implemented by FF_1. Besides, FB_0 path also implements another zero to compensate for the phase shift due to the integrators. The two zeros are further from the origin to provide a higher in-band loop gain, and zeros closer to the imaginary axis could pull the LC poles further to the left half-plane [17].

However, the quality factor of the two zeros cannot be too high since that of the closed loop poles will be high, which causes ringing issues. Q is chosen to 1 to balance stability and in-band loop gain. The local feedback path FB_L forms a resonator with the two-stage integrators, it could maximize the average in-band loop gain.

2.2. Propose feedback-after-LC CDA architecture

2.2.1. Foreground Calibration

The foreground calibration operation is shown in Fig. 15, which is the one-time calibration. Hence the calibration is before CDA works. It has 2 stages: f_{LC} measurement stage and VGA programming. The system measures f_{LC} firstly, and then according to the loop-up table, VGA is adjusted to the specific gain, which ensures unity gain frequency variation stays near 1.2MHz and robust to $\pm 30\%$ LC tolerance. However, the unity gain frequency may be pushed above $\frac{f_{LC}}{\pi}$ without the VGA compensation.

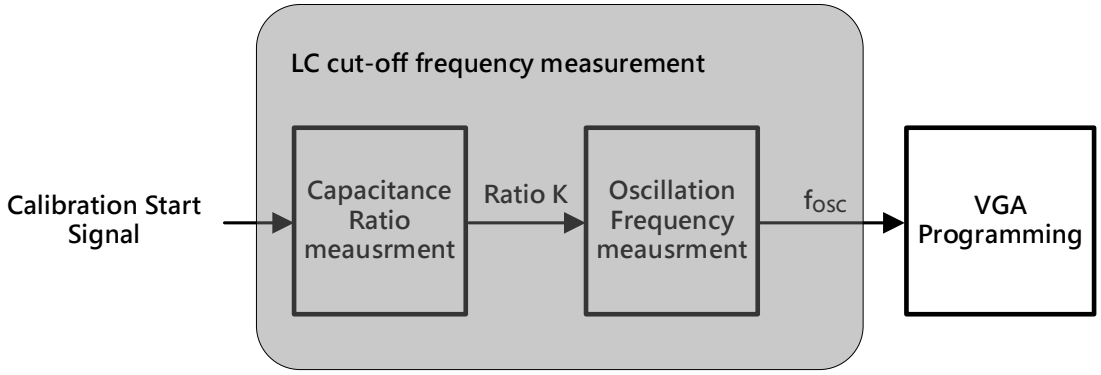

Fig. 15. Calibration operation diagram

Fig. 16 shows the loop gain around the output stage after adjusting the corresponding gains of VGA for the different f_{LC}. After compensation, the zero-frequency provided by the inner loop is fixed. Therefore, there is almost no extra phase shift after compensating. Furthermore, the unity gain frequency is still dominated by the inner loop and the LC tolerance stays at $\pm 30\%$.

However, it is impossible to measure f_{LC} without any error, and this measurement inaccuracy also causes the VGA gain error. As a result, this error also consumes part of the LC tolerance of the inner loop.

As we mentioned in Section I, the calibration error cannot exceed 6%. Hence f_{LC} measurement inaccuracy is designed to be below 3%, and VGA gain error below 3%.

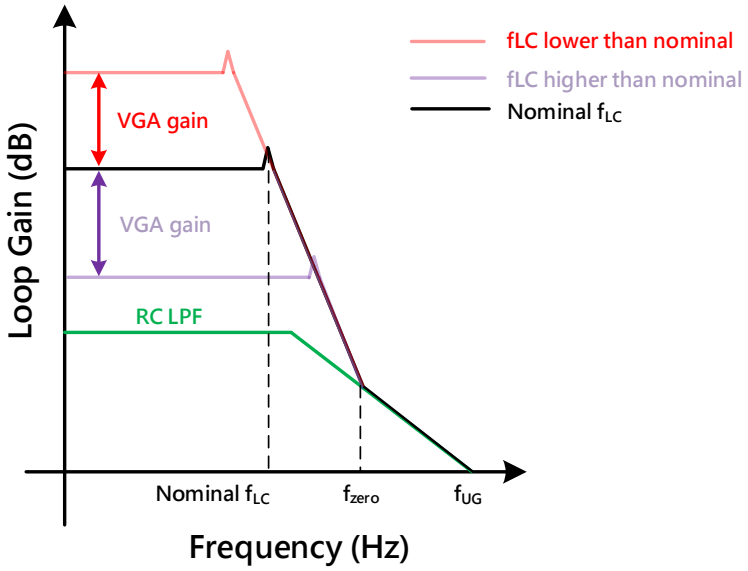

Fig. 16. Loop gain around the output stage

2.2.2. Loop filter structure

The VGA is added into this loop to compensate for the variation of the LC filter, which is shown in Fig. 17. The green highlighted block is implemented as a VGA.

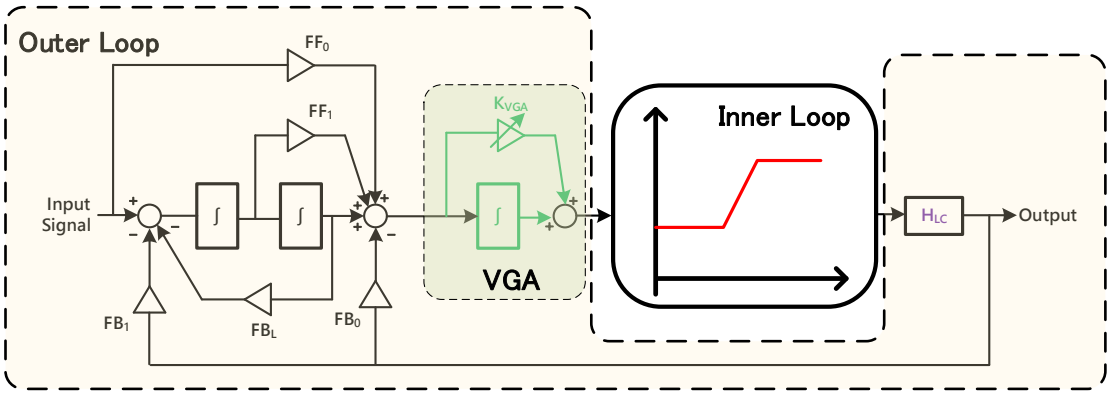

Fig. 17. Complete block diagram of the proposed class-D amplifier

The variable gain is realized by changing the ratio of the resistors R_{FV} and R_V, and also a feedback capacitor C_{FV} is added to it to form an integral-proportion path, which boosts the loop gain around the LC filter over 40dB at 20kHz, shown in Fig. 18.

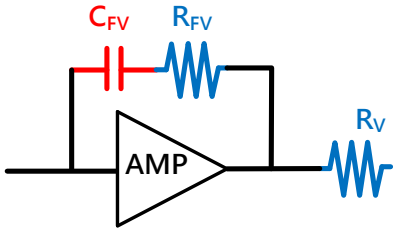

Fig. 18. Block diagram of Variable Gain Amplifier

The reason we add the feedback capacitor to VGA is that after programming the VGA for the 200kHz f_{LC}, the loop gain around the LC filter is insufficient (30dB) without the feedback capacitor because there is -16dB loop gain degradation when programming for 200kHz f_{LC}, this gain degrades both loop gains around LC filter and output stage directly, as shown in Fig .19. The red curve is loop gain with 200kHz f_{LC}. However, when f_{LC} is lower than the nominal frequency (87.6kHz), the loop gain is boosted by the VGA gain.

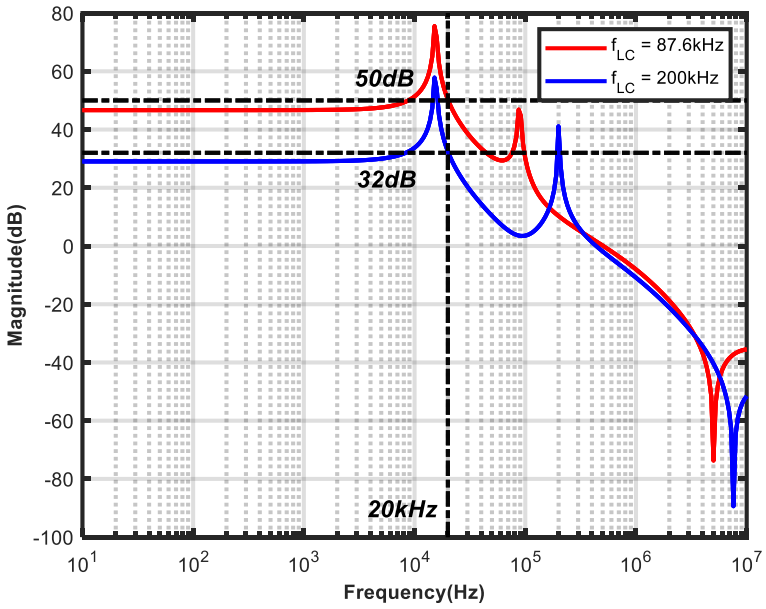

Fig. 19. Loop ground around the LC filter degraded by VGA

After adding the integration capacitor, the average loop gain around the LC filter is boosted to 40dB at 20kHz by decreasing this capacitance shown in Fig. 20.

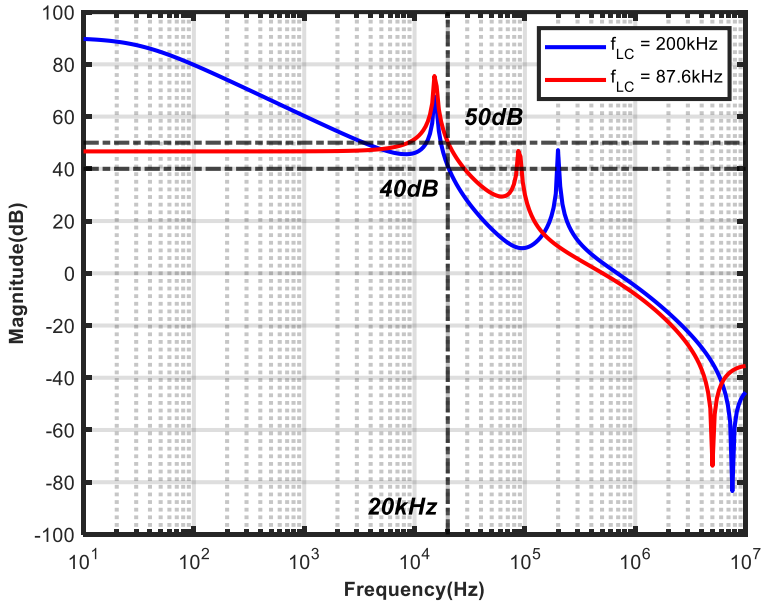

Fig. 20. Loop ground around the LC filter with an integral capacitor

However, the zero cannot be made too low since the phase margin will be degraded. Fig. 21 shows the bode plot of the closed loop gain of VGA, it shows that the smaller zero gives a lower gain but a higher phase compensation. Hence, there is a trade-off between loop gain and phase margin.

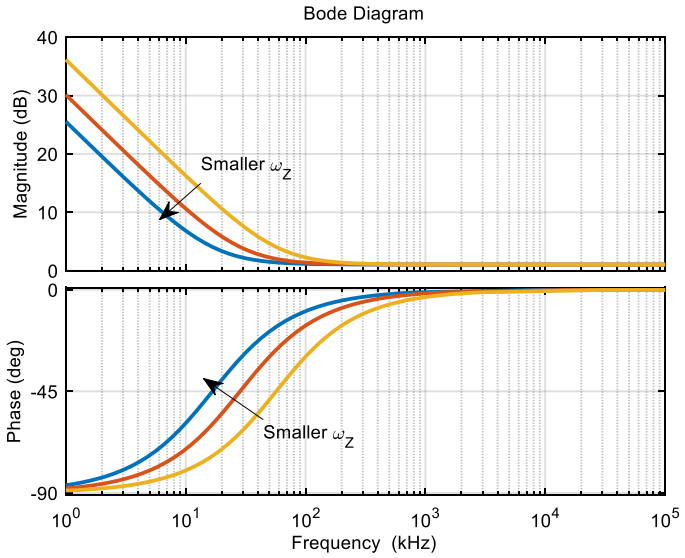

Fig. 21. Close-loop gain of variable gain amplifier

2.2.3. The LC Cut-off frequency calibration range

The proposed architecture should be robust to 70~200 kHz f_{LC} with corresponding VGA programming. For the 200kHz upper bound, the limiting factor is stability. The loop gain around the LC filter is plotted in Fig. 21. There is a concavity between the peak (LC resonant and in-band resonant points) which is highlighted in the red point. This red point will be lower than 0dB when f_{LC} is around 250kHz because of the degradation of low VGA gain. Hence the unity gain frequency is defined at this point.

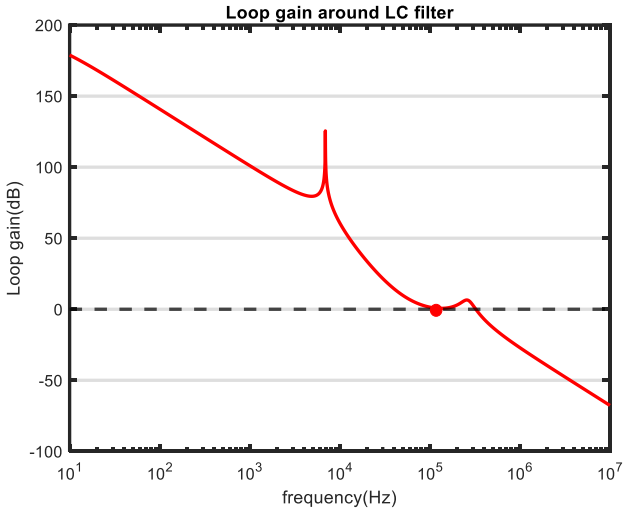

Fig. 22. Loop gain around LC filter after compensation with 200kHz f_{LC}

For the lower bound of the calibration range, f_{LC} varies to 70kHz due to manufacturing tolerance. When the lower bound range is lower to extend more tolerance, the VGA gain error will exceed 3the % accuracy requirement as mentioned in Section I. Considering the manufacturing tolerance of the LC filters,

the lower bound of the calibration range is 70kHz. Eventually, the calibration range for f_{LC} variation is 70kHz~200kHz.

2.2.4. Calibration operation

This calibration is a one-time adjustment, and it can calibrate the variation due to manufacturing errors. There will not be any calibrations after this CDA is working normally. The nominal f_{LC} is 87.6kHz in this CDA [4]. During the calibration, there are no loudspeakers or input signals.

Fig. 23 shows the simplified foreground calibration schematic. The voltage regulator (PVCM Reg.) provides 7.2V DC voltage to the output stage. Hence, we reuse PVCM Reg. to make the LC filters oscillate through the output stage. After the LC filers are discharged to 0V, the output stage is turned on to connect PVCM Reg. to the LC filter. Therefore, the LC filter starts to oscillate. However, the load capacitor C_{CM} is in series with C_{filt} through MN1 and MN2, resulting in oscillation frequency changes. The oscillation frequency ($f_{LC\_changed}$) changes as follows. Hence, the capacitance ratio between C_{CM} and C_{filt} needs to be measured before oscillating.

$$f_{LC_{changed}} = \frac{1}{2\pi\sqrt{L(C_{filt}||C_{CM})}} \tag{10}$$

The whole calibration operation has two stages, shown in Fig. 15, capacitance ratio measurement stage, f_{LC} measurement stage and VGA programming.

In the first stage, also shown in Fig. 23 C_{filt} and C_{CM} are the LC filter capacitor and load capacitor of the voltage regulator which provides 7.2V DC voltage to the LC filters. Hence the PVCM load capacitor C_{CM} is in series with C_{filt}, which changes the oscillation frequency. Hence the ratio of C_{CM} and the C_{filt} is measured to calculate f_{LC} with oscillation frequency. At the oscillation measurement stage, the mid-rail power supply voltage is connected to the LC filter, as a result, the LC filter starts to oscillate. And then five oscillation cycles' period is measured by the digital counters considering the accuracy requirement because the oscillation amplitude is too small to give the required accuracy, which will be illustrated in Section III. After the ratio and oscillation frequency are known, f_{LC} can be calculated, and then VGA is programmed to the gain we need

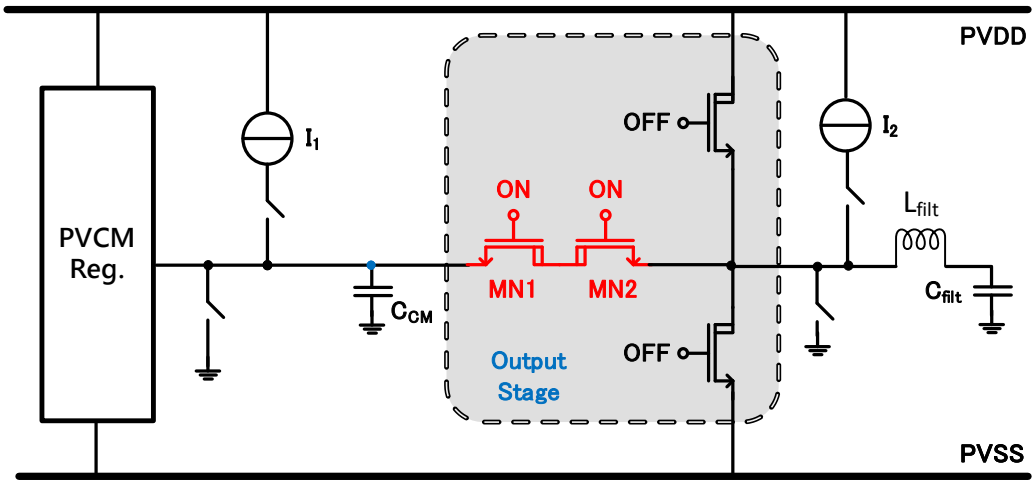

Fig. 23. Simplified capacitance ratio measurement circuit

In our calibration system, the two finite-state machines control each calibration operation. Signal 'CAL' determines whether calibration is on. When calibration is on, which means 'CAL' is high, the calibration starts once the reset signal is pulled up. Fig. 24 shows the states, the green highlighted states are the capacitance ratio measurement, and the right-half states are the f_{LC} measurement. These states are processed by orders, which are illustrated as follows.

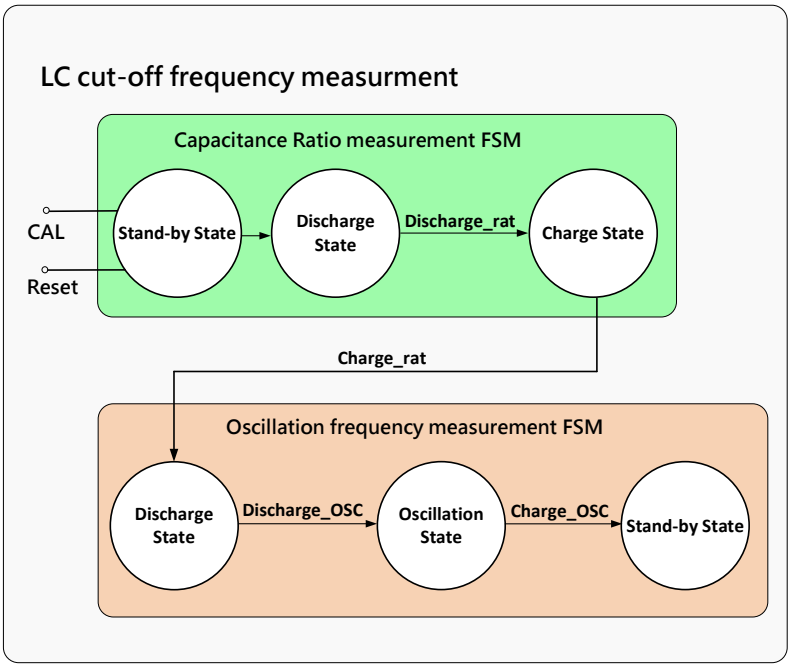

Fig. 24. Progress diagram of the two finite state machines

The complete capacitance measurement circuit is shown in Fig. 25, a 7.2V output voltage regulator (PVCM) and output stage of the CDA are re-used. The current sources I1 I2 and I3 will be on to charge the three capacitors. Switches DN1, DN2, and DN3 discharge the capacitors when they are on. V_a is high when discharge is done and V_b is high when the charge is done. And the digital counters measure the

oscillation period in 4.2MHz clock frequency, which will be illustrated in Section III.

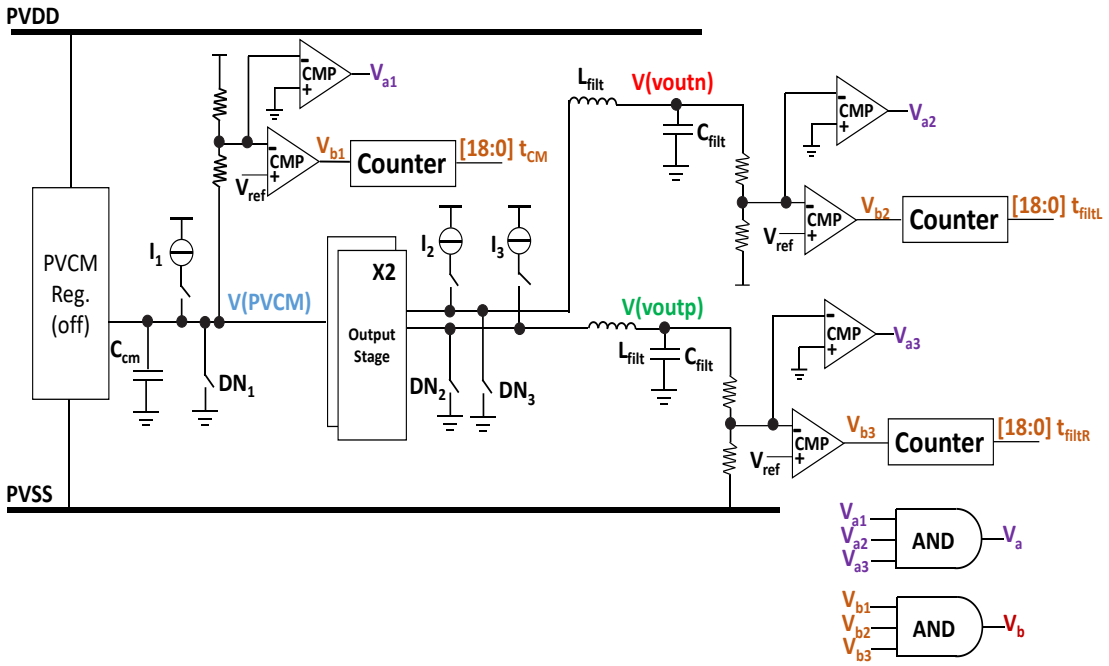

Fig. 25. The complete capacitance measurement circuit

The f_{LC} measurement circuit is shown in Fig. 26. The oscillation waves are compared with the reference voltage through a 7:1 resistor divider, and the reference voltage is the PVCM output voltage divided by a 7:1 resistor divider as well. And then the comparators (CMP) output square waves in oscillation frequency which are measured by the counters.

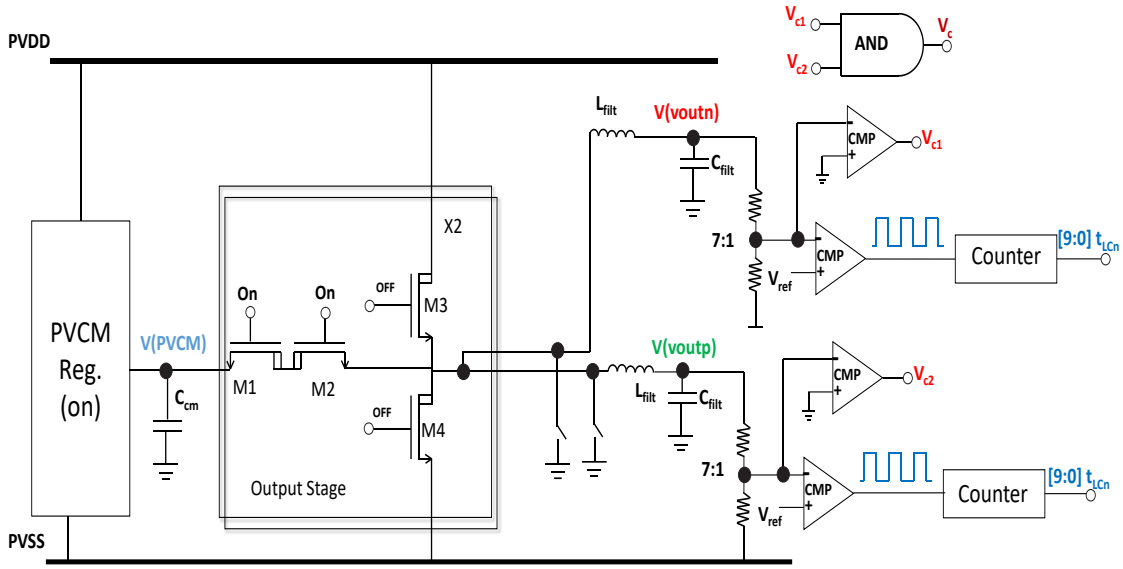

Fig. 26. The oscillation frequency measurement circuit

Fig. 27 shows the waveforms of V(voutn), V(voutp) and V(PVCM) in Fig. 19 and Fig. 20 during the whole calibration process. In this calibration, C_{CM} is $6\mu F$ considering the stability of PVCM. The nominal capacitance and inductance are $1\mu F$ and $3.3\mu H$.

To verify if the system can calibrate the LC filters with a mismatch, we add a 30% mismatch between the capacitors and inductors. As a result, the two filter capacitors are $0.7\mu F$ and $1.3\mu F$ respectively and the two filter inductors are $2.2\mu F$ and $4.4\mu H$ respectively. The calibration process is illustrated as follows.

After the whole system is power-on, the global reset signal is pulled up manually. Hence the C_{CM} and C_{filt} are discharged to 0V. Once discharging is done, the current source I1, I2 and I3 start to charge them to 1.8V and the charging time of the 3 capacitors are measured by the digital counters. Hence capacitance ratio measurement is completed. After that, the voltages on the LC filters are discharged until PVCM outputs a stable 7.2V voltage. This voltage is connected to the first LC filter by M1 and M2, as a result, the first LC filter starts to oscillate and the digital counter measures the 5 oscillation periods, and then the LC filter is discharged again. After discharging is done, the second LC filter is connected to the 7.2V and oscillates, and then the f_{LC} of the second LC filter is measured by the digital counter.

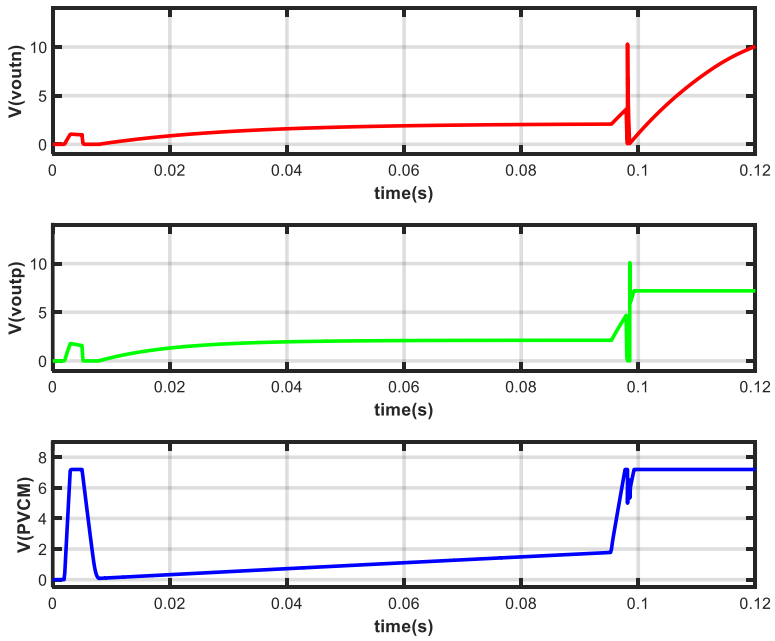

Fig. 27. The whole calibration waveforms

Fig. 27 is zoomed in, as shown in Fig. 28. The PVCM outputs 7.2V voltage finally during start-up. This waveform is the start-up of Fig.19. V(voutn) and V(voutp) which are the voltage on the LC filter is charged to 2.2V roughly since M1 and M2 are off during start-up and only the leakage current charges them during start-up.

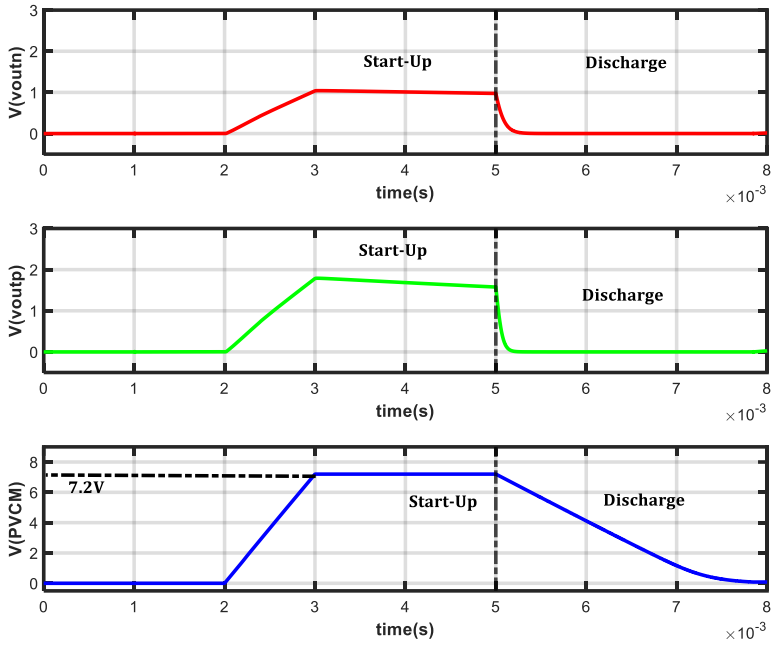

Fig. 28. The waveform at start-up

After discharging on the LC filter and C_{CM} is finished, the ratio measurement starts, as shown in Fig 29. This waveform is from Fig. 25. $t_{cn}[18:0]$, $t_{cp}[18:0]$ and $t_{CM}[18:0]$ are digital outputs, showing how many 4.2MHz clock cycles. Hence, we can obtain the time when C_{CM} and the two C_{filt} are charged to 1.8V from 0V.

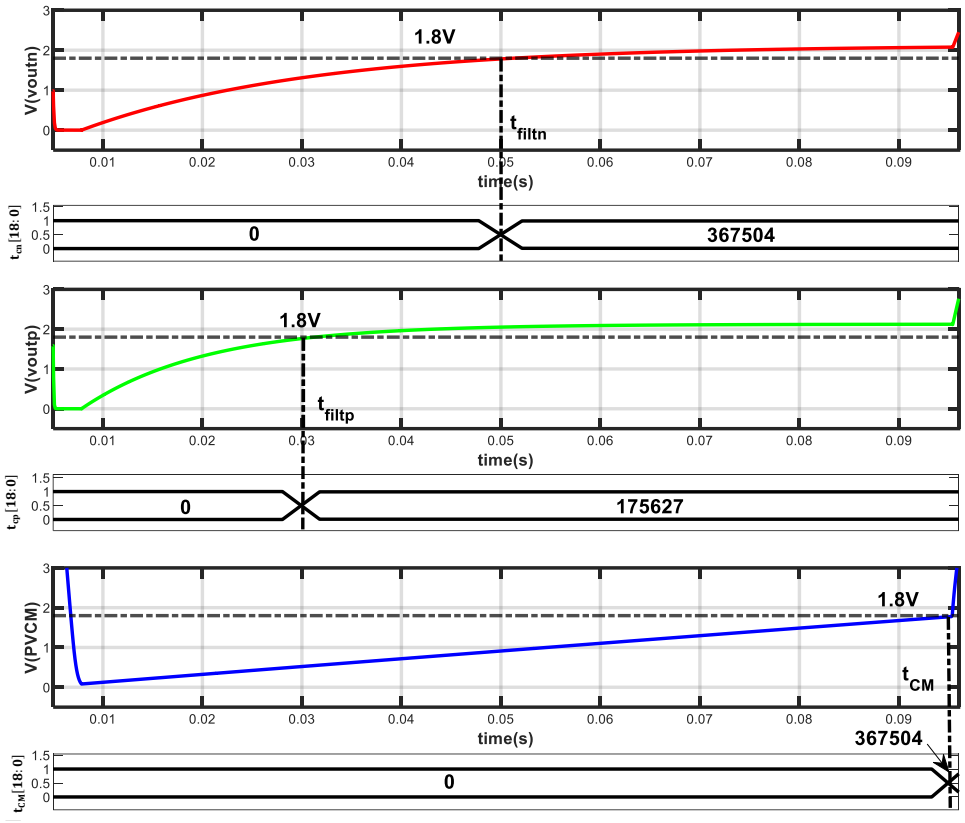

Fig. 29. The waveform at capacitance ratio measurement

V(voutn) and V(voutp) are not increasing linearly during charging because the resistors of the feedback-after-LC path and the resistors dividers are in parallel with the filter capacitors. The model of the resistors and capacitors can be simplified in Fig. 30.

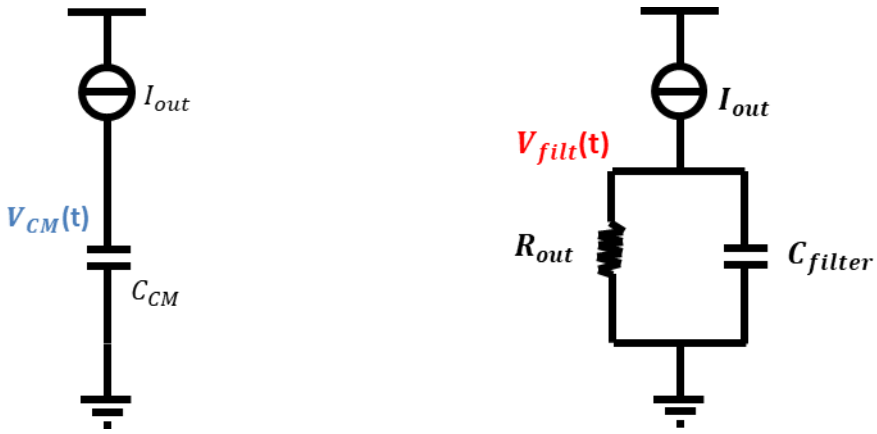

Fig. 30. The simplified model of the capacitor in LC filter and C_{CM}

Hence the voltage on the C_{filt} is expressed as equation (11), and the voltage on C_{CM} is expressed as equation (12).

$$V_{filt}(t) = R_{out}I_{out} \cdot \left(1 - e^{-\frac{t_{filt}}{R_{out}C_{filter}}}\right) \tag{11}$$

$$V_{CM}(t) = \frac{I_{out}}{C_{CM}} \cdot t_{CM} \tag{12}$$

Where Rout is the equivalent parallel resistance at the output of LC filters, I_{out} is the charge current provided the current sources I1, I2 and I3, t_{filt} and t_{CM} are the charging time on C_{filt} and C_{CM} respectively when the voltage is charged to 1.8V. The R_{out} is 23k ohm and I_{out} is 120uA. Therefore, the voltage on 0.2uF~1uF C_{filt} is an exponential wave. As a result, the capacitance ratio is defined as follows:

$$\frac{C_{CM}}{C_{filt}} = \frac{t_{CM}}{t_{filt}} \cdot \frac{R_{out}I_{out} \cdot ln\left(1 - \frac{1.8}{R_{out}I_{out}}\right)}{1.8} \tag{13}$$

When capacitance ratio measurement is done, the PVCM regulator is turned on. However, the circuit cannot go into the next state directly because PVCM needs a 1.5ms settling time, V(PVCM) shows the settling in Fig. 31. After PVCM is stable, the circuit goes to f_{LC} measurement state.

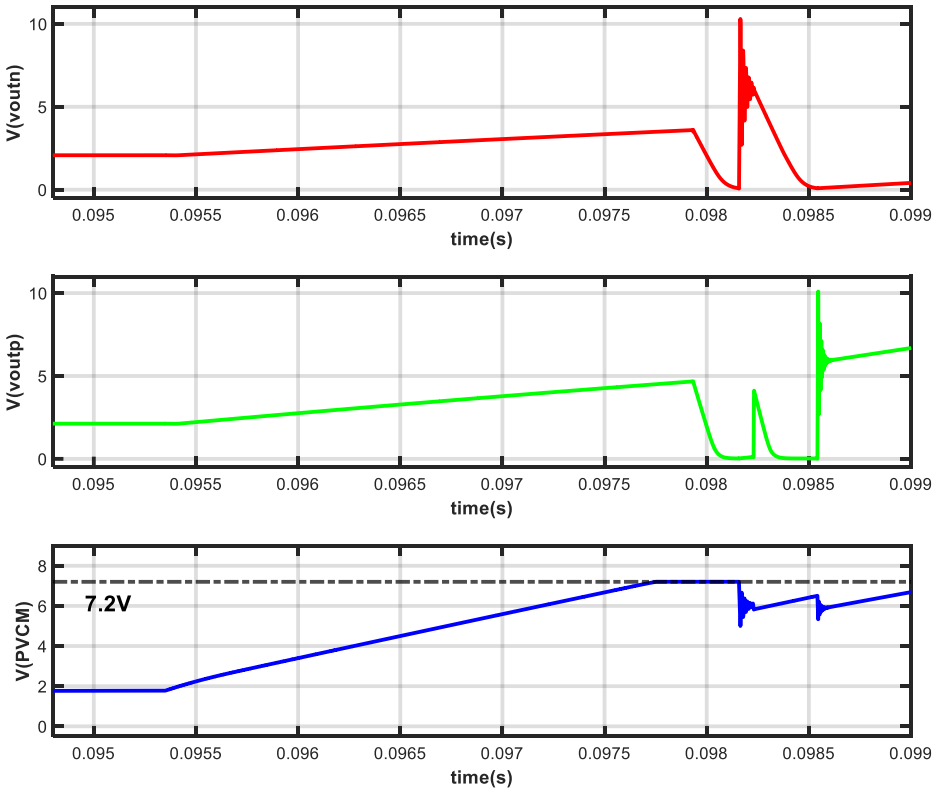

Fig. 31. The PVCM is settling waveforms

At the first state of f_{LC} measurement, the voltages on both LC filters are discharged to 0V as shown in Fig. 32 and then the first LC filter is connected to the PVCM through MN1 and MN2, and then V(voutn), which is the output of it, starts to

oscillate. After the first LC filter finishes oscillating, the second LC filter starts to be discharged and oscillates as well. The oscillating cycles by the two LC filters are compared with a reference voltage in the comparators to generate the digital signals, and the 10-bit digital counters measure five periods with a 4.2MHz clock signal. $t_{filtn}[9:0]$, $t_{filtp}[9:0]$ are the digital outputs.

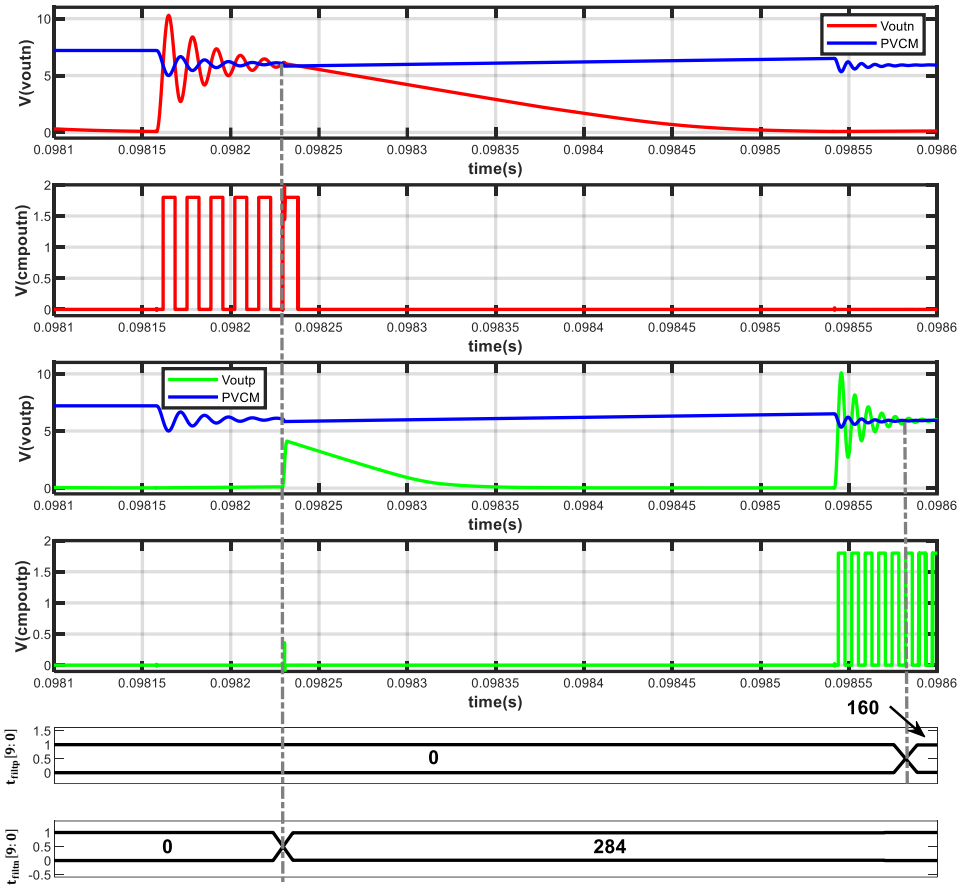

Fig. 32. The oscillation waveforms

2.2.5. Variable gain amplifier programming

After the counters measure the time, we can calculate how much gain the VGA should be adjusted. The practical LC components always have a mismatch, so we have to calculate the f_{LC} for each LC filter with 2 measured times t_{LCn} and t_{LCp}. The oscillation frequency of both LC filters can be calculated by the equation (14) and (15), where f_{osc_R} and f_{osc_L} are the oscillation frequency of each LC filter.

$$f_{osc_L} = 4.2MHz \times \frac{5}{t_{LCn}} \tag{14}$$

$$f_{osc_R} = 4.2MHz \times \frac{5}{t_{LCp}} \tag{15}$$

We can obtain f_{LC} of each LC filter by equations (16) and (17):

$$f_{LC_L} = f_{osc_L} \times \sqrt{\frac{K_1 + 1}{K_1}} \tag{16}$$

$$f_{LC_R} = f_{osc_R} \times \sqrt{\frac{K_2 + 1}{K_2}} \tag{17}$$

where K_1 and K_2 are the ratios between C_{filt} and C_{CM}. After knowing f_{LC}, the LC product of each LC filter $(LC)_L$ and $(LC)_R$ can be calculated by f_{LC} expression ($f_{LC} = \frac{1}{2\pi\sqrt{LC}}$).

With the two LC products, an equivalent LC transfer function can be expressed as:

$$H_{LC}(s) = \frac{\left(\frac{1}{s^2(LC)_L + 1} + \frac{1}{s^2(LC)_R + 1}\right)}{2} = \frac{1}{s^2(LC)_{tot} + 1} \tag{18}$$

The equivalent f_{LC_tot} is also known.

$$f_{LC_{tot}} = \frac{1}{2\pi\sqrt{(LC)_{tot}}} \tag{19}$$

Eventually, the gain programmed in VGA is expressed as:

$$\text{VGA } Gain\ (dB) = \log_{10}\frac{f_{LC_{nom}}}{f_{LC_{tot}}} \cdot \frac{40dB}{dec} \tag{20}$$

where f_{LC_nom} is the nominal LC cut-off frequency.

3. Circuit implementation

3.1. Loop filter

Fig. 33 shows the circuit schematic of the loop filter with the VGA. The loop filter is fully differential with active RC integrators. The loop bandwidth is near 1.2MHz. Hence the OTA phase margin should be larger than 50 degrees across the process corners, and peak loop gain is designed to be above 70dB, and the unity gain frequency in OTA of VGA is near 15MHz.

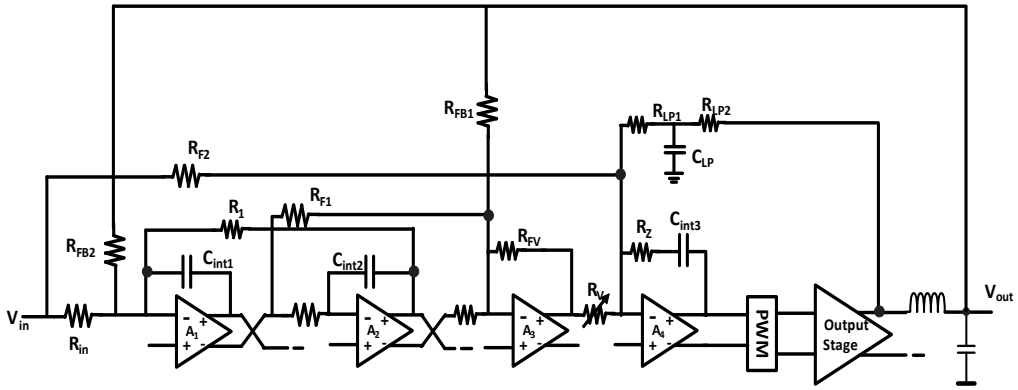

Fig. 33. Circuit implementation of the loop filter

The capacitors of the loop filter are constructed as 2-bit switchable banks in order to realize the target RC time constants following a one-time calibration of the foreground, as shown in Fig. 34. The b[1:0] are2-bit switchable banks and the C_{div} is the one-seventh of nominal capacitance, therefore nominal capacitance is 7 times C_{div}. When capacitors have +20% variation, b[1:0] are disconnected resulting in six C_{div}. Hence, the capacitance connected in the integrator is 7.2 times C_{div}. Similarly for, -20% variation, the capacitance after trimming is still 7.2 times C_{div}. Consequently, regardless of the process variation, the tolerable frequency range for the f_{LC} can be centered on the nominal frequency of 87.6 kHz.

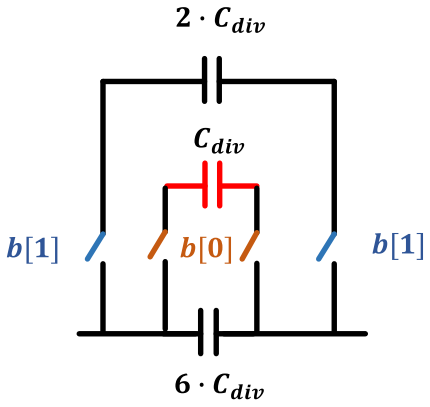

Fig. 34. One-time calibration

The third integrator (VGA) processes the difference between the output of the first, and second integrators and the feedback-after-LC signals. A two-stage

feedforward compensated OTA is reused in the VGA as well as in other integrators, the schematic of it is shown in Fig. 35.

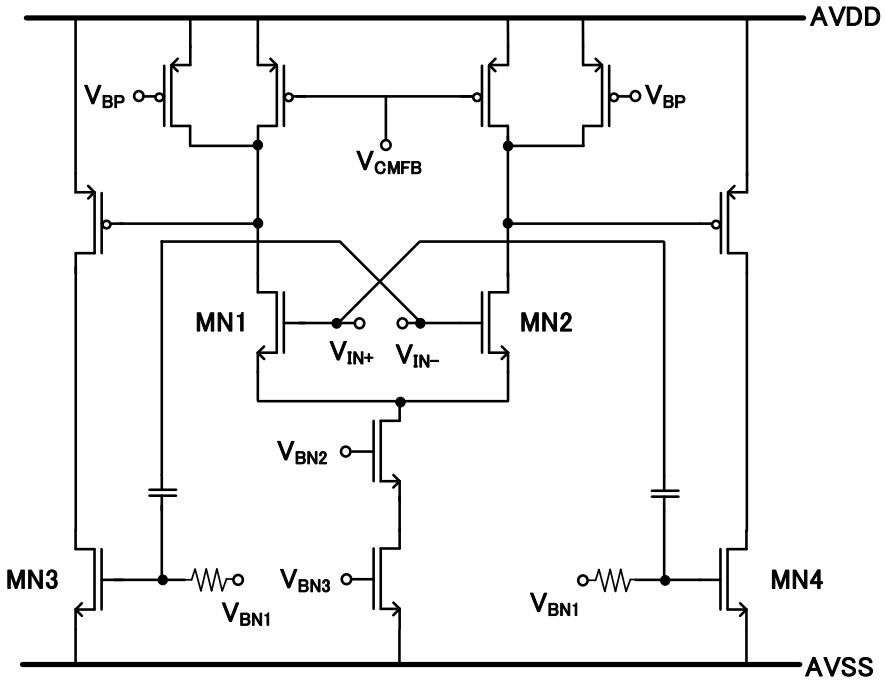

Fig. 35. Circuit implementation of two-stage feedforward compensated OTA used in the loop filter

The input is ac-coupled to output by MN3 and MN4 in the output stage [14][15]. This OTA utilizes the feedforward path to compensate for the phase shift due to the forward path, as shown in Fig. 36,

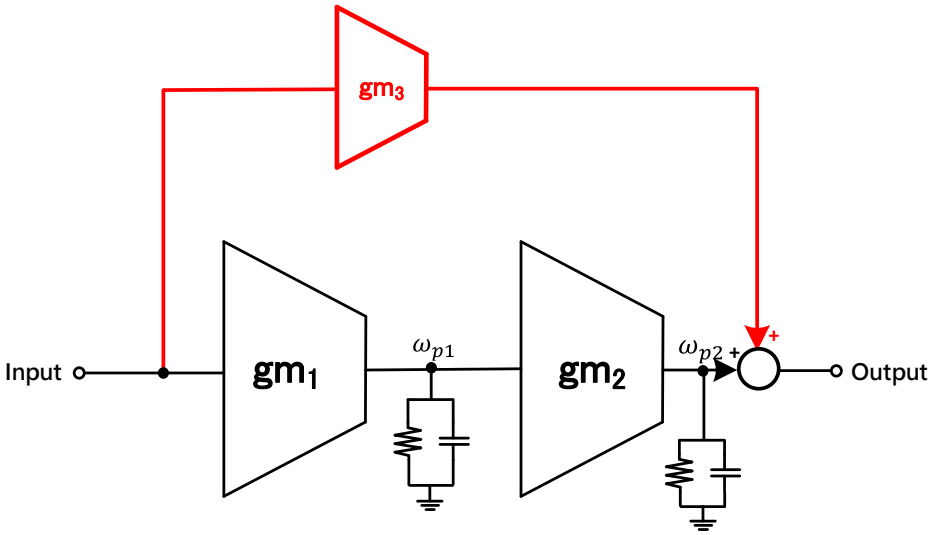

Fig. 36. Block diagram of the two-stage amplifier

The feedforward path is gm3 and the 2-stage forward path goes through gm1 and gm2. The closed-loop gain plot is shown in Fig. 37, gm3 forms the high-frequency path (red) to provide a zero and forward path gm1 and gm2 (black) is the high-gain path. Compared to two-stage Miller compensated OTA, this OTA does not need to

charge a miller compensated capacitor. Hence it is able to achieve extra loop gain at the PWM frequency without increasing the power consumption.

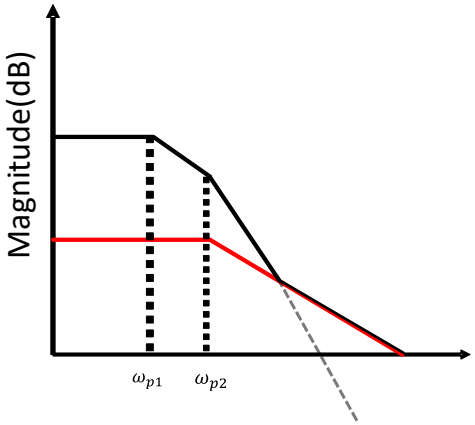

Fig. 37. The closed-loop gain of the two-stage amplifier

Fig. 38 shows the loop gain with the feedback network, and these phase margins over the five process corners are all above 50 degrees, and the unity gain frequency is near 15MHz.

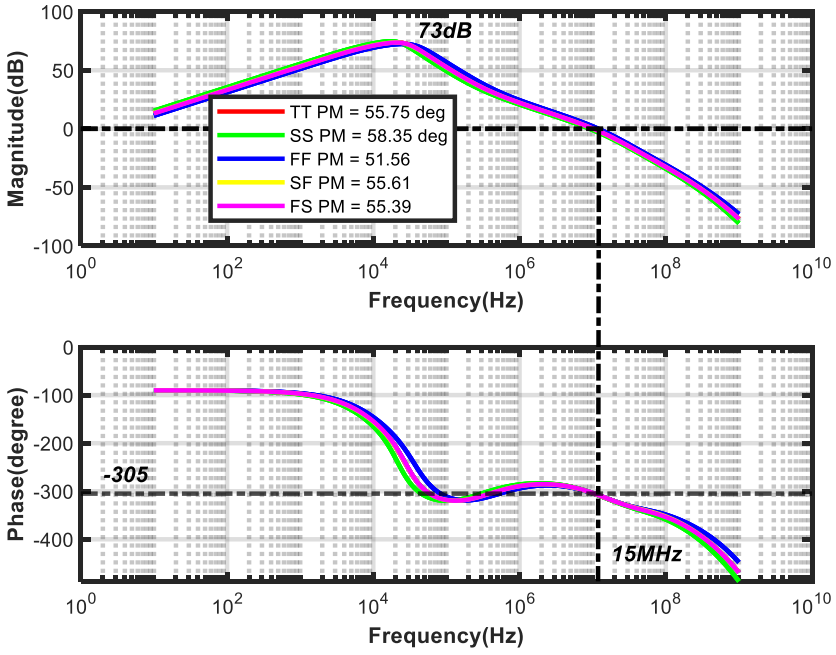

Fig. 38. The loop gains of the two-stage amplifier

3.2. VGA gains programmability

The variable gain is realized by a programmed resistor R_V and R_V is a binary weighted array, as shown in Fig. 39. The complementary switches are employed to control the total resistance of R_V.

As we discussed in Section II, the gain error of VGA should be lower than 3%. As a result, the on-resistance of the switches is $0.2\ k\Omega$ and the nonlinearity should be below -50dB since the loop gain around the output stage is 70dB.

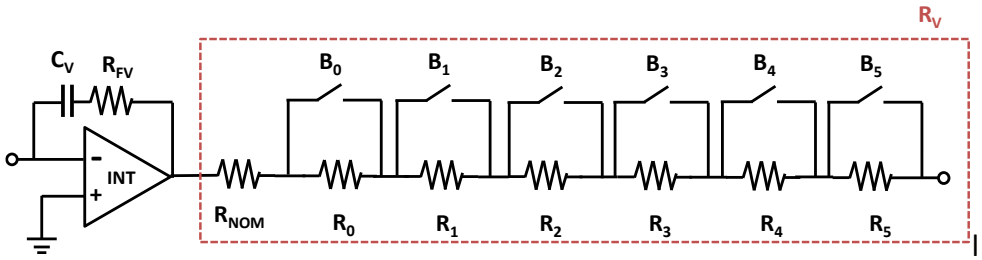

Fig. 39. The variable gain amplifier circuit implementation

According to the simplified equation (20), we know that VGA gain is determined by f_{LC}. Hence the quantization error consumes the LC tolerance achieved by the inner loop. As mentioned in section I, the whole calibration error can only have less than 5% LC tolerance to satisfy the PWM criteria. Hence only 3% tolerance is given for quantization, as a result, 6-bit R_V is implemented in VGA which consumes 2.5% LC tolerance due to quantization error.

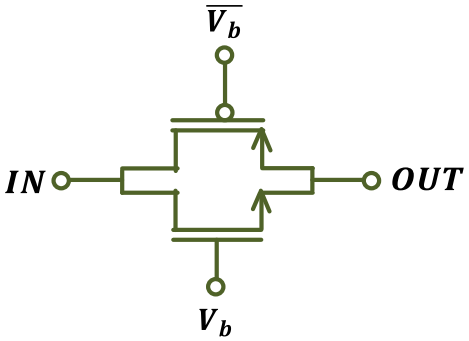

Fig. 40. Complementary switch

As mentioned above, the complementary PMOS-NMOS switch is implemented, as shown in Fig. 40. Over the input voltage range, it increases the overall conductance resulting in a lower time constant and the switch conductance is more linear compared to the single PMOS or NMOS switch. However, the on-resistance influences the accuracy of programming gain because it is in parallel with each resistor. The nonlinearity of switches can be suppressed by the loop gain around the output stage (70dB at least), which relaxes the linearity performance of switches. As a result, -60dB THD of the switches is achieved to keep THD at the output below -100dB, as shown in Fig. 41.

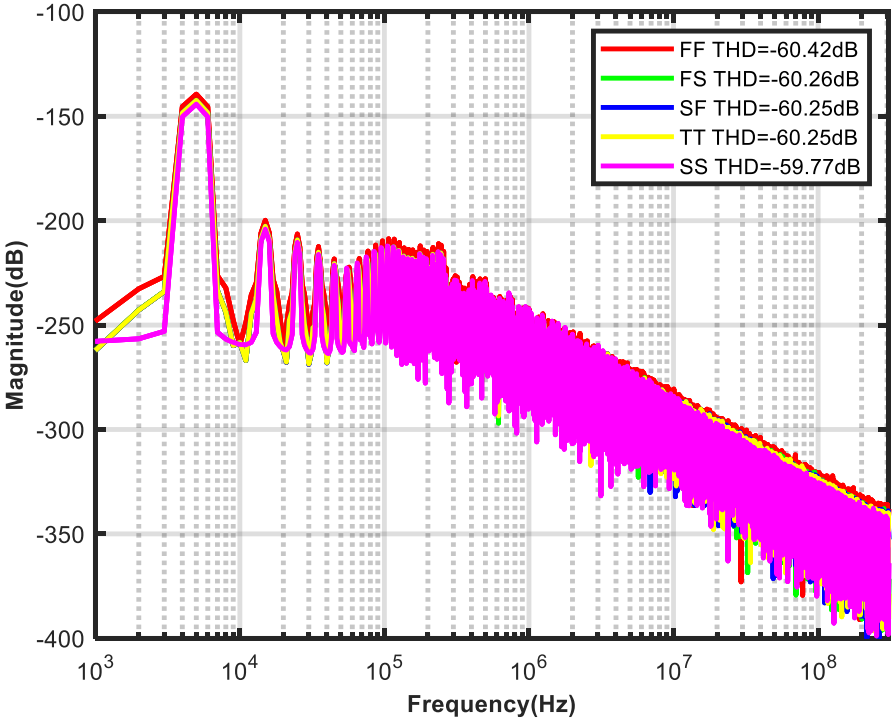

Fig. 41. Output spectra of the complementary switches

Besides, a 0.5% gain error is realized in $0.2k\Omega$ on resistance by choosing 10um/0.18um PMOS and 5um/0.18um NMOS.

3.3. Comparator

The performance of comparators generating oscillation square-wave in f_{LC} measurement circuit influences the f_{LC}measurement inaccuracy. According to the above description, there is only 3% LC tolerance left for the f_{LC} measurement inaccuracy, including capacitance ratio measurement inaccuracy. Hence, we arrange 2% for oscillation measurement accuracy and 1% for capacitance ratio measurement inaccuracy.

The three-stage comparator with a two-stage inverter buffer is shown in Fig. 42, the input transistors are implemented by PMOS, which allows 0V comparison. The comparator's delay and kick-back noise limit the measurement accuracy. The comparator delay is determined by the speed of the comparator. The lower length of the input transistors and the higher bias current would give a lower delay.

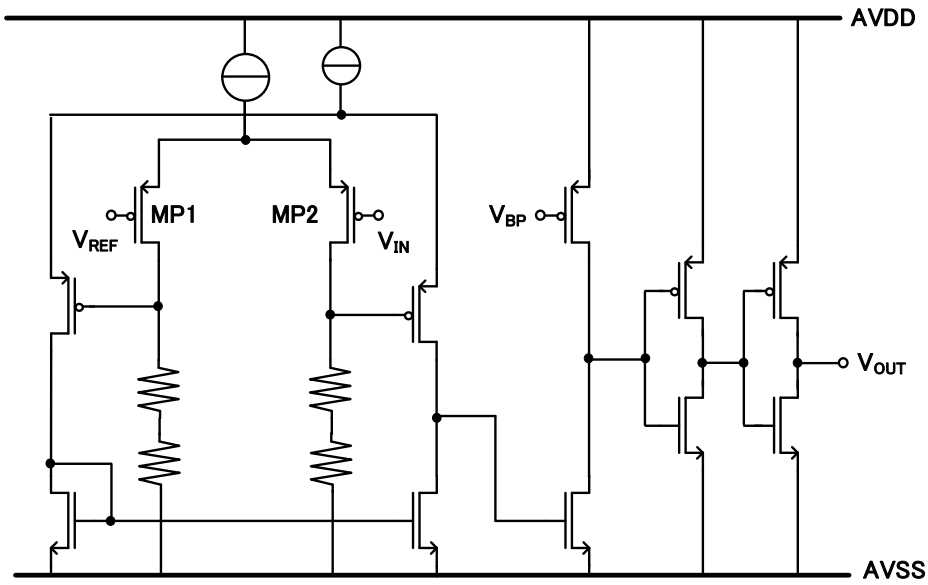

Fig. 42. Three-stage comparator

However, when the input signals cross the reference voltage, there is a sharp voltage change at the output as well as the drain of MOS, which leads to a large change in input signals by drain-gate capacitors. As a result, the comparator switches several times during the transition. As shown in Fig. 43, this is the simulaiton waveforms of kickback effect with transient noise when the input signal crosses the reference voltage. The output switches 5 times. Hence, this effect degrades the accuracy of f_{LC} measurement significantly. To mitigate the kickback effect, the comparator speed cannot be too high. Eventually, to meet the 2% inaccuracy requirement, the input transistors are sized to compromise speed with kickback noise.

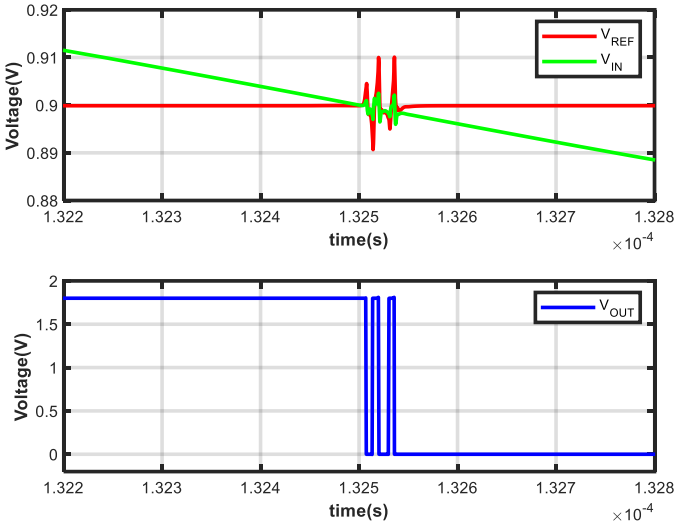

Fig. 43 Effect of kickback noise waveform

The requirement of comparator offset is only determined by the difference between the sixth oscillation cycle and the reference voltage to ensure five oscillations cycles can be measured by digital counters because offset does not affect the inaccuracy.

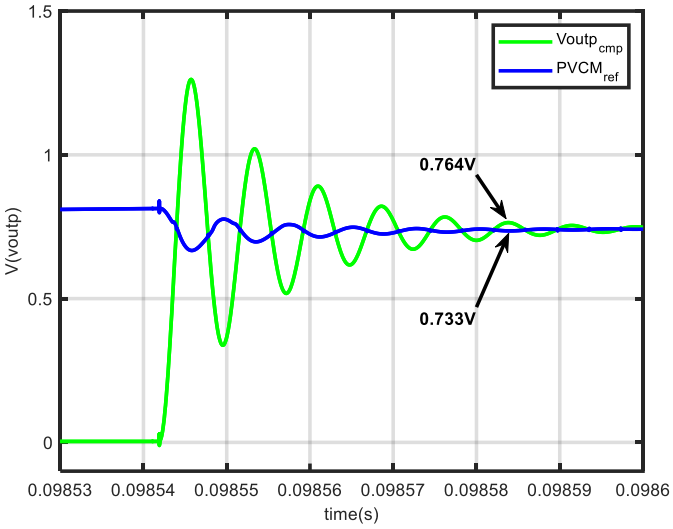

Fig. 44. The difference between the sixth oscillation cycle and the reference voltage

As shown in Fig. 44, this difference is 30mV and the offset can be easily designed to be lower than it. We finally designed a 4.2mV offset and the offset of the Monte Carlo simulation shown in Fig. 45.

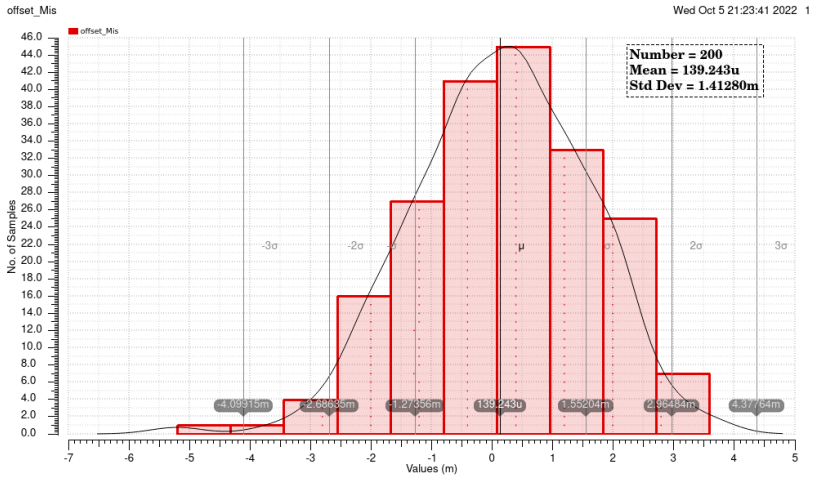

Fig.45. Monte Carlo simulation of comparator offset

3.4. Current sources

The current source provides $120\mu A$ to C_{filt} and C_{filt} to ensure that the voltage can be charged above 1.8V and the mismatch current is lower than $10\mu A$ according to the gain error requirement. The current sources schematic is shown in Fig. 46.

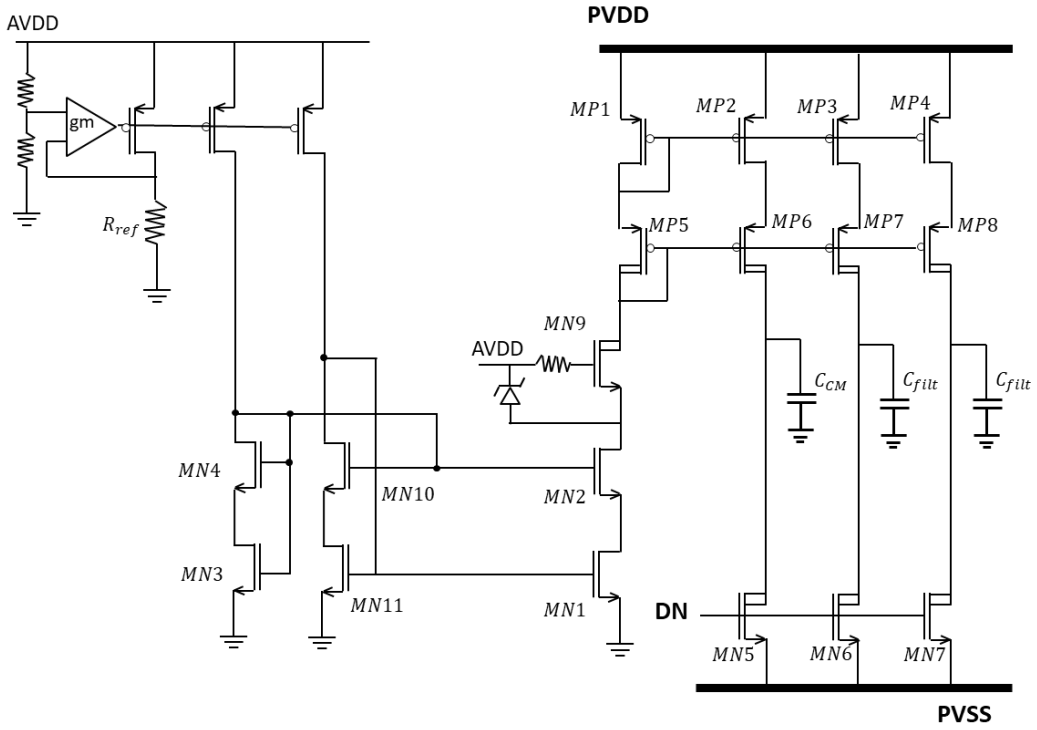

Fig. 46. The current sources in the capacitance ratio measurement circuit

It charges the C_{CM} and C_{filt} to obtain the ratio between them. Due to C_{CM} and C_{filt} in series, the f_{LC} can be calculated by equation (21),

$$f_{osc} = \frac{1}{2\pi\sqrt{L \cdot C_{filt}}} \cdot \sqrt{\frac{K+1}{K}} \tag{21}$$

where f_{OSC} is the measured oscillation frequency and K is the ratio.

As mentioned in Section II, the parallel resistors with C_{filt} make the voltage-time response on C_{filt} differ from it on C_{CM}, equation (22) and equation (23) describe the difference.

$$V_{filt}(t) = R_{out}I_{out} \cdot \left(1 - e^{-\frac{t_{filt}}{R_{out}C_{filter}}}\right) \tag{22}$$

$$V_{CM}(t) = \frac{I_{out}}{C_{CM}} \cdot t_{CM} \tag{23}$$

where R_{out} ($18k\Omega$) is the total parallel resistance, I_{out} is the charging current, t_{CM} and t_{filt} are the charging time when voltages on C_{CM} and C_{filt} are charged to 1.8V from 0V respectively, $V_{filt}(t)$ and $V_{CM}(t)$ are the time response of C_{filt} and C_{CM}.

Hence, the ratio of C_{CM} and C_{filt} is expressed as equation (24):

$$\frac{C_{CM}}{C_{filt}} = \frac{t_{CM}}{t_{filt}} \cdot \frac{R_{out}I_{out} \cdot ln\left(1 - \frac{1.8}{R_{out}I_{out}}\right)}{1.8} \tag{24}$$

1.8V in this equation is AVDD, we can make this term $\frac{1.8}{I_{out}}$ is sensitive to power supply variation. Hence the current should be designed to be proportional to the AVDD despite AVDD's variation. As a result, the current sources are designed as follows. The reference current is generated by the reference resistor R_{ref} by imposing $\frac{2}{3}$ AVDD voltage on it. As a result, the current is proportional to AVDD, as shown in Fig 13. Moreover, according to (3-1) the voltage on C_{filt} converges to $R_{out}I_{out}$. Hence It is designed to $120\mu A$ to ensure that this voltage can be charged above 1.8V.

In this current source shown in Fig. 47, MN1~MN6 forms the cascode current sources and MN9 is implemented as 36V NMOS to protect the low-voltage MOS. The C_{filt} and C_{CM} are discharged by MN5, MN6 and MN7 when DN is high. And the gate is pulled down to turn off the current source.

Furthermore, the mismatch between the three output branches determines the capacitance ratio inaccuracy. Hence, to minimize the mismatch and cost, the high-voltage PMOS cascodes MP6, MP7 and MP8 cascode the low-voltage PMOS MP2, MP3 and MP4. As mentioned above, 1% f_{LC} measurement inaccuracy due to capacitance ratio accuracy is required. Hence the proportion of mismatch current in output current should not be larger than 6% for 6uF C_{CM}.-In our case, the Monte Carlo simulation result for the current mismatch is only 0.6% as shown in Fig. 47. It almost does not cause errors to f_{LC} measurement inaccuracy (<0.1%).

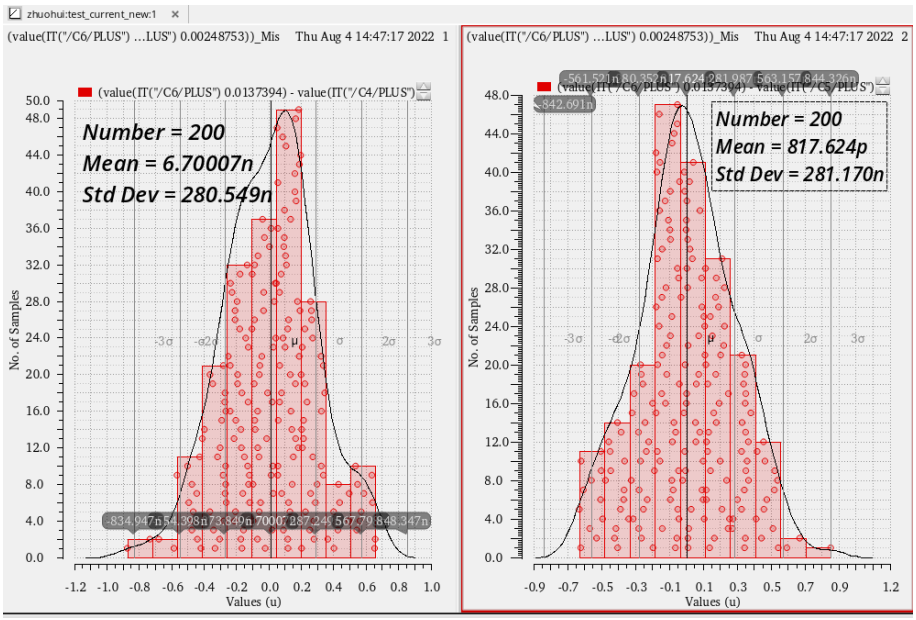

Fig. 47. The mismatch current in the current source

4. Simulation Results

The whole circuit is built in a 180-nm BCD process. The output stage employs a 14.4-V supply. The loop filter and PWM operate with a 1.8-V supply.

The loop filter schematic is shown in Fig. 33, and f_{LC} measurement circuit is shown in Fig. 25 and Fig. 26. The simulation process is shown in Fig. 48. During the simulation, the system first outputs f_{LC} between 70kHz and 200kHz by digital counters and then we simulate the stability and linearity of the system after adjusting the loop filter over temperature and process corners. In addition, the input signal and loudspeaker don't exist during f_{LC} measurement but only in linearity simulation after the measurement.

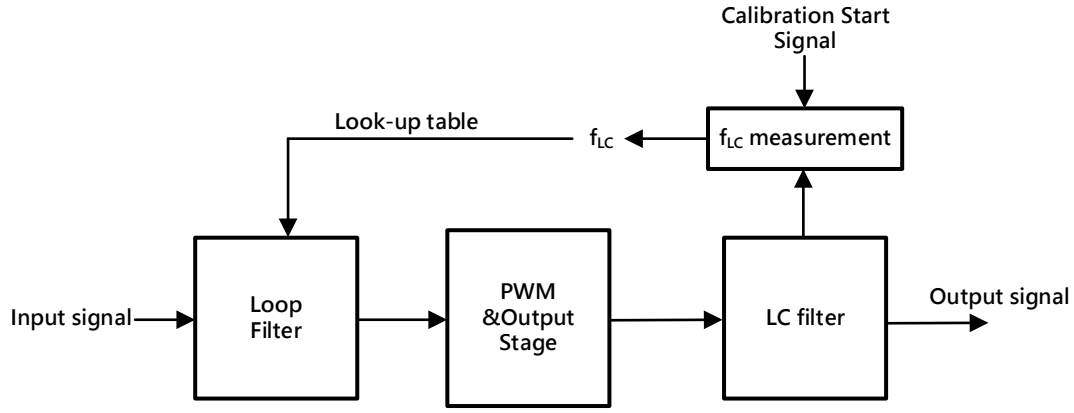

Fig. 48. The simulation process of the system.

4.1. LC cut-off frequency measurement accuracy

Table 4-I and 4-II show f_{LC} measurement error, it achieves 0.7% best error and 1.83% worst inaccuracy with 30% mismatch over process corners and temperature. The first row of the table is the nominal f_{LC}, so based on the nominal capacitance and inductance, we add +30% and -30% mismatch from the nominal capacitance and inductance to the two LC filters respectively. As a result, the LC values is (1±30%) times the nominal values for each simulation. The simulation temperature is 25℃ in TABLE 4-I and 120℃ in TABLE 4-II.

TABLE 4-I

LC cut-off frequency measurement error (temp. 25℃)

f_LC / kHz	87.6k	100k	120k	140k	160k	180k	200k
Inaccuracy of ratio (SS)	0.93%	1.53%	1.4%	1.2%	1.11%	1.56%	1.6%
Inaccuracy of ratio (FF)	0.82%	0.63%	0.7%	1.1%	1.03%	0.75%	1.2%
Inaccuracy of ratio (TT)	0.91%	1.3%	1.21%	0.89%	0.99%	1.22%	1.14%

TABLE 4-II
LC cut-off frequency measurement error (temp. 120°C)

f_LC / kHz	87.6k	100k	120k	140k	160k	180k	200k
Inaccuracy of ratio (SS)	1.23%	1.22%	0.89%	1.17%	1.31%	1.34%	1.83%
Inaccuracy of ratio (FF)	1.12%	1.41%	0.98%	1.63%	0.82%	1.43%	1.65%
Inaccuracy of ratio (TT)	1.11%	1.22%	1.36%	1.47%	0.97%	1.62%	1.43%

4.2. LC filter Nonlinearity suppression

The audio performance simulation is with 5kHz input and 8-ohm load, the PWM frequency is 4.2MHz. Nonlinearity due to DC dependency of the LC filter is modelled in our design. To estimate the magnitude of LC filter nonlinearity, THD before the LC filter is simulated, which contains the pre-distortion to the feedback path. Fig. 48 shows the output spectrum and time domain waveform before the LC filter, it contains waveforms between 70~200kHz f_{LC} LC filters over temperature and process corners. THD is from -75dB to -91dB. We can see worst THD is still lower than -75dB with a maximum -25% DC variation.

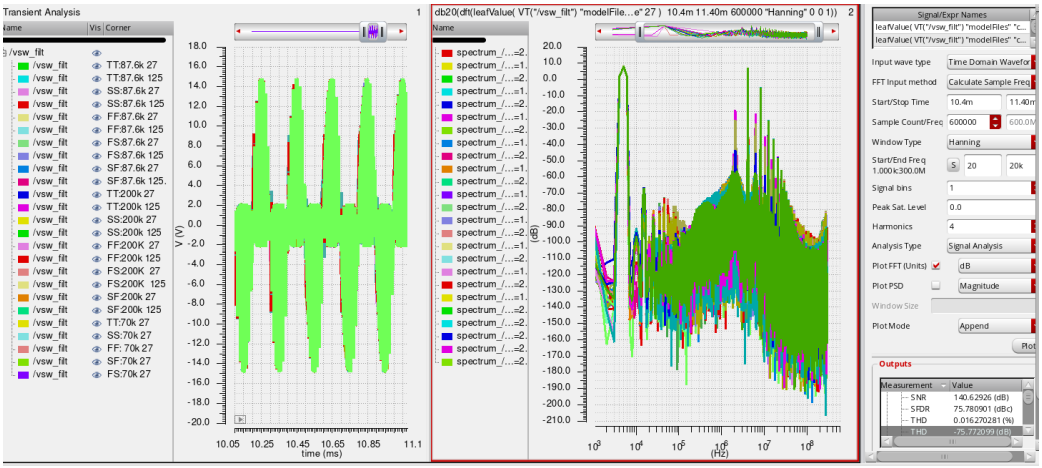

Fig. 48. The spectra and waveforms before the LC filter

Our design is able to calibrate the f_{LC} from 70kHz to 200kHz LC filters. THD+N at the output is also simulated. Fig. 49 shows the output of the LC filter spectrum and the output waveforms after programming VGA. This design achieves -108dB for worst THD and -126dB for best THD.

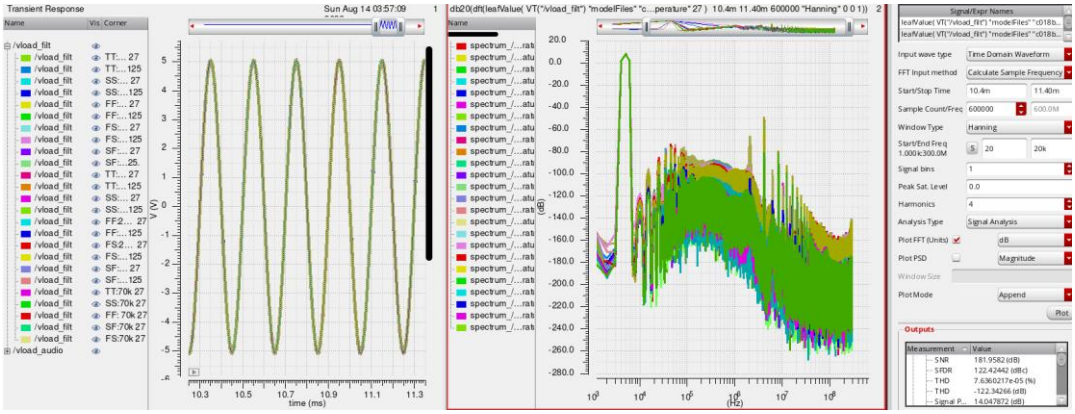

Fig. 49. The spectra and waveforms after the LC filter

4.3. LC filter variation compensation

To Verify the robustness to f_{LC} varied between 70kHz and 200kHz, the bode plots of the system are shown in Fig. 50 and Fig. 51. The phase margin is above 38 degrees. And the maximum unity gain frequency is 1.18MHz which still meets the PWM criteria.

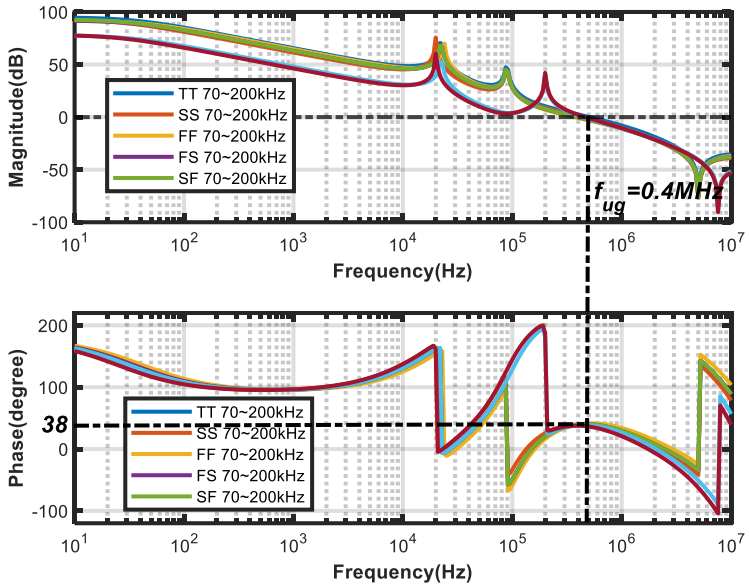

Fig. 50. The loop gain and phase around the LC filter

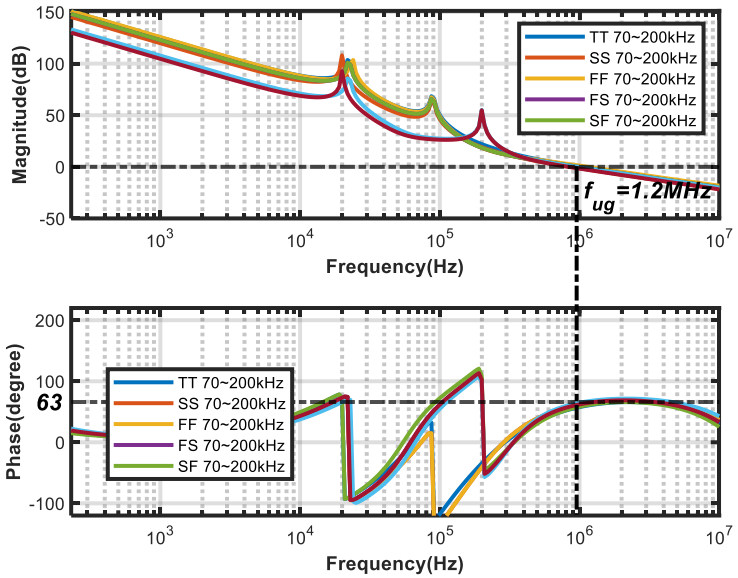

Fig. 51. The loop gain and phase around the output stage

5. Conclusion

A structure to calibrate the LC filter variation is proposed with a differential analog-input class-D amplifier with feedback after the LC filter. A variable gain amplifier compensates the LC spread after measuring f_{LC}. It is also robust to f_{LC} varied from 70kHz to 200KHz after programming VGA. It is implemented in a 180-nm BCD process and achieves −108-dB THD and 40-dB suppression of LC filter nonlinearity at least.

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