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Towards bifacial silicon heterojunction solar cells with reduced TCO use

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Abstract

Reducing indium consumption, which is related to the transparent conductive oxide (TCO) use, is a key challenge for scaling up silicon heterojunction (SHJ) solar cell technology to terawatt level. In this work, we developed bifacial SHJ solar cells with reduced TCO thickness. We present three types of In_2O_3-based TCOs, tin-, fluorine-, and tungsten-doped In_2O_3 (ITO, IFO, and IWO), whose thickness has been optimally minimized. These are promising TCOs, respectively, from post-transition metal doping, anionic doping, and transition metal doping and exhibit different opto-electrical properties. We performed optical simulations and electrical investigations with varied TCO thicknesses. The results indicate that (i) reducing TCO thickness could yield larger current in both monofacial and bifacial SHJ devices; (ii) our IWO and IFO are favorable for *n*-contact and *p*-contact, respectively; and (iii) our ITO could serve well for both *n*-contact and *p*-contact. Interestingly, for the *p*-contact, with the ITO thickness reducing from 75 nm to 25 nm, the average contact resistivity values show a decreasing trend from 390 mΩ cm^2 to 114 mΩ cm^2. With applying 25-nm-thick front IWO in *n*-contact, and 25-nm-thick rear ITO use in *p*-contact, we obtained front side efficiencies above 22% in bifacial SHJ solar cells. This represents a 67% TCO reduction with respect to a reference bifacial solar cell with 75-nm-thick TCO on both sides.

KEYWORDS
bifacial solar cell, silicon heterojunction solar cell, TCO reduction, transparent conductive oxide (TCO)

1 | INTRODUCTION

Silicon heterojunction (SHJ) solar cells have exhibited high efficiencies above 25% in both academia and industry.[1,2] Key challenges to be addressed in the upscaling process are the cost and the relative scarcity of certain utilized materials, such as indium, silver, and bismuth.[3,4]

Indium is widely used in the transparent electrodes of SHJ devices. For the purpose of reducing indium consumption, basic strategies include (i) use of In-free transparent electrode (TE), including In-free transparent conductive oxide (TCO) such as aluminum-doped zinc oxide (AZO),[5–7] and other TE material such as graphene[8]; (ii) reduction of the TCO thickness; (iii) development of *TCO-free* SHJ devices (extreme case). For the AZO use in (i), challenges may lie in low carrier mobility and stability issues,[9–11] and the promise of non-traditional TE material use still needs to be tested and developed. For (iii), proof-of-concept TCO-free SHJ solar cells have been demonstrated,[12] but efforts have been hampered from the passivation deterioration and contacting problems.[12–14] For instance, a thick thin-film silicon layer was reported to reduce the passivation deterioration, but it accompanies additional optical loss due to the parasitic absorption from the thin-film silicon layer[12]; titanium (Ti) was reported to maintain a low contact resistance between silicon layer and metal, but Ti can easily react with thin-film silicon layer and depassivate the solar cell.[13] The issues remain to be tackled in the future. Besides, it is still an open question whether *TCO-free* design could potentially give optimal device performance. Moreover, a TCO layer is practically needed to act as a barrier layer against Cu diffusion during plating processes.[15,16] To circumvent these limitations, we focus on the solution with reducing TCO use in SHJ solar cells.

From the optical point of view, front and rear TCO layers function as anti-reflection coating (ARC) and back reflector (BR) layers, respectively.[17] However, parasitic free carrier absorption (FCA) from both sides TCOs is unavoidable, which is directly proportional to the carrier density.[18] The use of a thinner TCO layer could considerably reduce FCA. However, the functions of ARC and BR are weakened. As for the ARC purpose, an additional optical capping layer (OCL), such as MgF_2,[19] SiO_x,[9,20,21] SiN_x,[12,17] and TiO_x,[22] could be utilized to reach an optimal light in-coupling. It has been well proven that as compared with a SHJ device counterpart with only TCO layer acting as ARC at illumination side(s), the device with a double layer anti-reflection coating could produce an even higher current output[23] and meanwhile potentially improve the device stability.[9] Besides, considering the BR loss when reducing rear TCO use in SHJ solar cell, Holman et al.[24] and Cruz et al.[21] have reported that implementing an OCL between the rear TCO and the full-area rear metal could quench optical losses in the near-infrared wavelength range. Nevertheless, in order to find out what are the minimal TCO thicknesses for different TCOs to maintain/reach good optical responses at device level, an elaborate study on both sides TCO/OCL optimizations with varied TCOs remains to be carried out.

Meanwhile, the optical optimization should be addressed without detrimentally affecting the electrical performance of the device.[25] It is known that a high quality wafer absorber could itself provide substantial lateral transport of majority carriers.[26] However, for efficient utilization of absorber's lateral transport, very low contact resistances in the vertical directions are essential.[27] In general, for the monofacial SHJ solar cells, the electrical problem exists at the TCO/doped silicon layer interfaces, where carrier transport barrier forms mainly due to the work function differences between TCO and doped silicon layers.[13,28,29] The work function defines the difference between the energy of the vacuum level and the Fermi level, which changes with the carrier density (N) in specific TCOs.[30] Considering the electrical properties (including N) of TCOs generally vary with the thickness of the TCO layer, it is imperative to investigate the thickness-dependent TCO/doped silicon layer contact properties when designing SHJ solar cells with reduced TCO thicknesses.

In this work, we choose three types of TCOs. These are tin-, fluorine-, and tungsten-doped indium oxides (namely, ITO, IFO, and IWO). They are In_2O_3-based TCOs that exhibit different opto-electrical properties from post-transition metallic cationic doping, anionic doping, and transition metallic cationic doping, respectively. From optical simulations, different required minimal TCO thicknesses for maintaining good optical performance are calculated. Further, we evaluate the lateral and vertical carrier transport behaviors in solar cells with varied TCO thicknesses. Finally, different bifacial SHJ devices with reduced TCO use are fabricated.

2 | EXPERIMENTAL

2.1 | Deposition of TCO films

TCO films were deposited on corning glass substrates by RF magnetron sputtering technique (Polyteknic AS), including a reference tin-doped indium oxide (ITO) layer. Prior to sputtering, the substrates were cleaned in acetone and isopropyl alcohol sonication baths for 10 min, respectively. All the TCO films were deposited at room temperature and power density of $\sim$0.8 W/cm^2. The ITO films were grown with a chamber pressure of 3.2×10^{-3} mbar and Ar flow of 20 sccm; the IFO films were deposited at a chamber pressure of 4.0×10^{-3} mbar, water vapor partial pressure 1.6×10^{-5} mbar, and Ar flow of 20 sccm; the IWO films were fabricated at a chamber pressure of 4.0×10^{-3} mbar and Ar flow of 20 sccm (mixed with 0.25% O_2).[19] The utilized ceramic targets were 90 wt% In_2O_3 and 10 wt% SnO_2 for ITO, a commercial In_2O_3-based *SCOT* target as described in Han et al.[31] for IFO, 95 wt% In_2O_3 and 5 wt% WO_3 for IWO. The chamber was evacuated to a base pressure below 1×10^{-7} mbar before deposition to eliminate the contribution of the water during the processing. The deposition rates were around 2 nm/min on flat surface. For one specific type of TCO layer, only the deposition time was changed to vary the TCO thickness. For the TCO deposition on textured wafer-based substrates, the deposition time is calculated from multiplying the deposition time on flat substrate by a geometrical factor of 1.7. To mimic the TCOs as used in SHJ device fabrications, a post annealing procedure was performed in oven at 180°C for 5 min, which would be required to cure the sputter damage on our SHJ cell precursors during TCO deposition at room temperature.[19] Additionally, standard 75-nm-thick TCOs were also deposited onto corning glass coated with thin-film silicon layer stacks as we applied in device fabrication.

2.2 | Fabrication of SHJ solar cells and samples for contact study

For fabricating wafer-based samples, 4-inch float zone (FZ) 280-μm-thick n and p-type flat (100) oriented wafers (1–5 Ω cm) were randomly textured in a heated solution composed of 5% TMAH and 2.4% ALKA-TEX 8 from GP-Solar-GmbH. The double-side textured wafers were then cleaned in two subsequent baths of HNO_3 for

10 min each: HNO_3 99% at RT and HNO_3 69.5% at 110°C to remove the organic and inorganic contaminations, respectively. Wafers were dipped in 0.55% HF for 4 min to remove the superficial native oxide layer and immediately after loaded into the plasma enhanced chemical vapor deposition (PECVD) system. Unless otherwise specified, SHJ cell precursors with front 10-nm-thick *i*/*n* stack and rear 26-nm-thick *i*/*p* stack thin-film silicon layers were prepared, based on *n*-type wafer. TCO films with specified thicknesses on both sides of the wafers were sputtered, through hard masks, which define different cell areas on each wafer. After sputtering, the cell precursors were annealed in air at 180°C for 5 min for curing purposes. For monofacial cells, front metal Cu fingers were electroplated at RT, with an underlying full-area sputtered 100-nm-thick Ag as seed layer. Photolithography was utilized for patterning the metal grid area.[32] The rear metal contact was 500-nm-thick PVD Ag. For bifacial cells, both sides were endowed with Cu-plated metal contacts. In addition, for a double layer anti-reflection coating (DLARC) purpose, 100-nm-thick SiO_x layer was e-beam evaporated on the illuminated side(s) of the completed SHJ devices. The fabricated solar cells feature a designated illumination area of 2×2 cm^2. The bifacial solar cell structure and the front side image of a complete device is shown in Figure S1a,b, in which the designed metal coverage is 1.6%, and the finger distance is 915 μm. We applied the same metal design on both sides of the wafer. The patterning was done with photolithography. The metallization approach for bifacial solar cell is electrochemical copper plating on a 200-nm-thick evaporated silver seed layer. The contact width is 15 μm, and the finger height is around 25 μm. For monofacial solar cell fabrication, we firstly did Cu-plating on the front side (i.e., *n*-side) of the wafer, with the rear side protected by a full area photoresist layer; then, a full area 500-nm-thick evaporated silver was deposited through hard masks as rear metal. For fabricating samples for contact study, we used stacks consisting of (*i*)a-Si:H, (*n*)nc-Si:H, (*n*)a-Si:H, TCO and metal for *n*-contact, and (*i*)a-Si:H, (*p*)nc-SiO_x:H, (*p*)nc-Si:H, TCO and metal for *p*-contact, respectively. The layers were kept the same as those used in SHJ device fabrication, except TCO variations. The symmetric sample structures for contact study are depicted in Figure S1c,d. Details about how we extracted the contact resistivity values are elaborated in Supporting Information.

2.3 | Characterizations

The opto-electrical properties of the TCO films were evaluated with a Hall effect measurement setup HMS-5000 (ECOPIA CORP) and with a spectroscopic ellipsometry (SE) system M-2000DI system (J.A. Woollam Co., Inc.). The former gave information on the carrier density (N_e), carrier mobility (μ_{hall}), and resistivity (ρ) of the TCO films. The latter was instead used to derive the film thickness (*d*) as well as the wavelength-dependent complex refractive index (*n*, *k*) and absorption coefficient (α) spectra. The optical band gap (E_g) was extracted from Tauc plot.[33] The single and multi-layer strategy approach in SE modelling is described in Han et al.[19] Besides, to obtain the absorptance (*A*) of the single TCO layers, the transmittance (*T*) and reflectance (*R*) spectra were obtained from a PerkinElmer Lambda 1050 system. The *A* was calculated as 1-*R*-*T*. Additionally, the surface roughness of the thin-film silicon layers was evaluated by atomic force microscope (AFM) measurements.

2.4 | Simulations

A first-principles density-functional theory (DFT) calculation was carried out via the Vienna Ab initio Simulation Package (VASP). Based on the projector augmented wave (PAW) method, the equilibrium geometric and electronic structures of In_2O_3 (IO), ITO, IFO, and IWO were calculated. The Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional was applied. The conventional cell of bixbyite In_2O_3 of 80 atoms was subjected to a geometry optimization. A 400-eV plane wave cut-off energy and a Γ-centered *k*-point grid of $3 \times 3 \times 1$ were utilized. The convergence criterion was below 0.01 eV/Å. To mimic the materials as we utilized in the lab, for ITO, three In 8b sites were replaced by Sn atoms; for IFO, five oxygen sites were replaced by F atoms; and in IWO, one In 24d site was replaced by W atom. The effective electron mass was obtained in the ab initio calculation through fitting the curvature of the conduction band.[34] The work function of a TCO was obtained from an additional simulation, in which a vacuum slab was added in the input file and the work function was extracted by taking the potential at the center of the vacuum.[35] Furthermore, ray-tracing GenPro4 optical simulations[36] of our SHJ device structure were performed based on double-side textured c-Si wafer with SE-fitted complex refractive index of each functional layer as input. For the simulation of bifacial cells, we used a rear side irradiance of 100 W/m^2. A superposition principle was employed to calculate the implied photocurrent densities in c-Si absorber ($A_{c\text{-}Si}$). Specifically, $A_{c\text{-}Si}$ values of the front and rear side illumination were separately obtained at a default 1000 W/m^2, which were $A_{c\text{-}Si,front}$ and $A_{c\text{-}Si,back,0}$. Then the overall $A_{c\text{-}Si}$ value was calculated via $A_{c\text{-}Si} = A_{c\text{-}Si,front} + 0.1 \times A_{c\text{-}Si,back,0}$.

2.5 | Solar cell measurements

Quasi-steady-state photoconductance (QSSPC) lifetime measurements were performed using a Sinton Instruments WCT-120 on cell precursors before and after the TCO sputtering. Current–voltage (*I*–*V*) characteristics of complete SHJ devices were measured using a class AAA Wacom WXS-90S-L2 solar simulator under 1-sun illumination conditions (100 mW cm^{-2}, AM 1.5G). For monofacial cell measurements, the *n*-contact side is the illuminated side, and the *p*-contact side is covered with full-area metal electrode. For the bifacial cell measurements, a piece of black velvet was used to minimize the influence of rear side illumination. The solar cell was mounted on top of the black velvet, with the probe contacting through a small hole across the black velvet on the back side of the cell. In the bifacial cell measurements, we got *I*–*V* curves for the front and rear side of one cell, which corresponded to our *n*-side and *p*-side of the cell. In addition, for contact study, we utilized symmetric sample structures as shown in Figure S1. The resistance (*R*) values of the sample were measured from four-point probe measurements via the electric stage as we used for the *I*–*V* measurements of solar cells. The principle and procedure of extracting contact resistivity (ρ_c) in our experiments are described in the Supporting Information, which is in line with.[37] For the statistic data plotting, we utilized one standard deviation as the error bar value.

3 | RESULTS AND DISCUSSION

3.1 | Optical evaluations regarding TCO reduction in SHJ

3.1.1 | Opto-electrical properties of TCOs

Hall measurements show that all the TCO films are *n*-type semiconductor. Figure 1A,B shows the carrier density (N_e) and electron mobility (μ_e) values of nominal 75-nm-thick TCOs on glass and on *i*/*n*/glass and *i*/*p*/glass, respectively. The *i*/*n* and *i*/*p* thin-film silicon layer stacks have the same layer thickness as used in SHJ devices. To mimic the layer performance in actual device fabrication, a hot-plate annealing at 180°C for 5 min was performed after the deposition of TCO at RT, which is a required step to recover the damage of the passivation quality of our SHJ cell precursors due to sputtering.[19] For the ITO and IFO films, with respect to the layers deposited on glass substrates, we observed increased N_e and decreased μ_e on the layers deposited on top of thin-film silicon layers. The N_e increase indicates a more absorptive nature in the TCO layers, and could be mainly owing to the diffused hydrogen from the thin film underneath, as it was elucidated by Cruz et al.[38] and Ritzau et al.[39] While the reason for the μ_e decrease is still unclear. We exclude the cause from the substrate surficial roughness as observed by Cruz et al.,[38] Erfurt et al.,[40] and Tutsch et al.[41] In fact, AFM measurements show similar root-mean-square roughness values of ~1 nm for both of our *i*/*n* and *i*/*p* stacks. Due to the N_e increase and μ_e decrease with respect to the layers deposited on glass substrates, the overall the resistivity (ρ) of

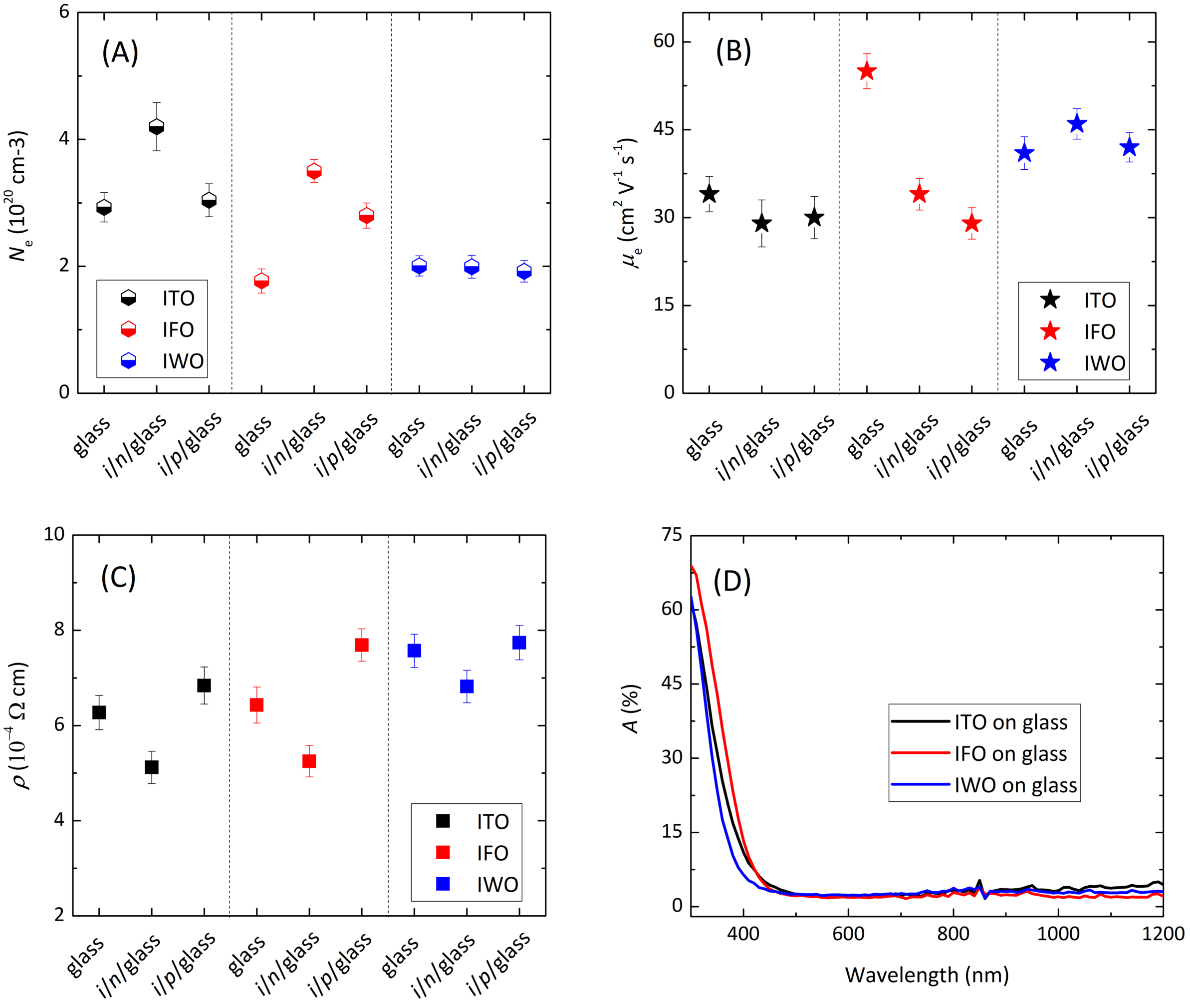

FIGURE 1 (A) Carrier density, N_e, (B) electron mobility, μ_e, and (C) resistivity, ρ, of the 75-nm-thick TCOs on top of different substrates. The results are based on three groups of experimental data. (D) Absorptance (*A*) curves of the TCO layers deposited on glass substrates

the ITO and IFO layers decreases when deposited on *i*/*n*/glass while slightly increases when deposited on *i*/*p*/glass (as shown in Figure 1C). In contrast, for the IWO layers, with respect to the layers deposited on glass substrates, a slightly decreased N_e and mildly increased μ_e were observed on layers deposited on thin-film silicon layers. As elucidated in our previous work,[19] the N_e decrease indicates more oxygen incorporation during the post-deposition annealing process, and the μ_e increase could be associated with an increased Lewis acid strength of the tungsten dopants, increased crystallization, and possible defect passivation of thermally effused hydrogen from underlying thin-film silicon layers. With respect to the layer deposited on glass substrates, the ρ of the IWO layers decreases when deposited on *i*/*n*/glass, while increases when deposited on *i*/*p*/glass, which is in accordance with the cases in ITO and IFO layers.

Figure 1D displays the absorptance (*A*) spectra of the TCO films deposited on glass substrates. The results were calculated from 1-*R*-*T* and exhibit the same trend as observed in ellipsometry measurements (data not shown). In the short wavelength range, the sharp transition range of *A* varies with different TCOs, indicating varied optical band gap (E_g) values. From Tauc plots,[33] the E_g values were obtained as 3.78 eV, 3.80 eV, and 3.86 eV for ITO, IFO, and IWO, respectively. We performed DFT calculations to obtain the band structures and density of states (DOS) of the host indium oxide (IO), ITO, IFO, and IWO materials. Interestingly, the calculated IFO shows significantly higher effective electron mass and notably lower fundamental band gap than the other two types of TCOs, which are inconsistent with experimental observations.[31,33,42] Tentative interpretation of the discrepancy is provided in Supporting Information. From Figure 1D, in the near infrared wavelength range, according to the classical Drude theory, the lower absorptance of the IFO and IWO films could be attributed to their lower N_e values as shown in Figure 1A.[18] In addition, with the multi-layer strategy from spectroscopic ellipsometry fittings as described in Han et al.,[19] we extracted the refractive index (*n*) and extinction coefficient (*k*) curves of the TCOs deposited on *i*/*n*/glass and *i*/*p*/glass, respectively, as shown in Figure S3. The data are the input for our subsequent optical simulations.

3.1.2 | Optical simulations on bifacial SHJ solar cells

Figure 2A–C shows GenPro4 optical simulation results of bifacial SHJ devices based on different TCO/SiO_x stacks.[36] For comparison, we provide the optical simulation results on monofacial cells in Figure S4. We applied the same type of TCO at the front and rear sides. The thicknesses of the front TCO and rear TCO are variables. In bifacial cell simulations, constant 100-nm-thick SiO_x layers were utilized on top of TCO and both sides of the wafer. This thickness was chosen from the procedures as described in the Supporting Information. From Figure 2A, for ITO-based devices, thinner ITO continuously leads to higher implied photocurrent densities in c-Si absorber ($J_{c\text{-}Si}$) values. The optimal optical response of 43.5 mA/cm^2 appears when 20-nm-thick front ITO and 0-nm-think back ITO layers are applied. Within the range of 0- to 50-nm-thick front ITO and 0- to 50-nm-thick back ITO, the $J_{c\text{-}Si}$ could be kept above 43.0 mA/cm^2. Above this range, the increased parasitic absorption due to thicker ITO use compensates the optical gain from decreased reflectance due to DLARC use. As a result, $J_{c\text{-}Si}$ decreases with further increase of front ITO and rear ITO thicknesses. From Figure 2B, the IFO-based devices show the highest $J_{c\text{-}Si}$ of 43.9 mA/cm^2, for 40-nm-thick and 20-nm-think IFO layers at front and rear sides of the wafer, respectively. With respect to Figure 2A, $J_{c\text{-}Si}$ of above 43.5 mA/cm^2 could be achieved in a wide range of IFO thicknesses, which is 20–70 nm for front IFO and 0–70 nm for rear IFO. Among the simulated devices, the IWO-based cells exhibit the best optical response within the widest range of TCO thicknesses, as shown in Figure 2C. The highest $J_{c\text{-}Si}$ of IWO-based devices is 44.3 mA/cm^2, which corresponds to a front side 50-nm- and rear side 10-nm-thick IWO layers use. The $J_{c\text{-}Si}$ is calculated to be above 44.0 mA/cm^2 in a broad range of IWO thickness, namely, 40 to 80 nm for front IWO and 0 to 100 nm for rear IWO (entire range investigated). Furthermore, it is noteworthy that considering the front side is dominating in the current contribution in the bifacial device, the results show more tolerance in the rear side TCO use. However, one should also take into consideration the bifaciality factor change upon rear TCO variations in practical device design.

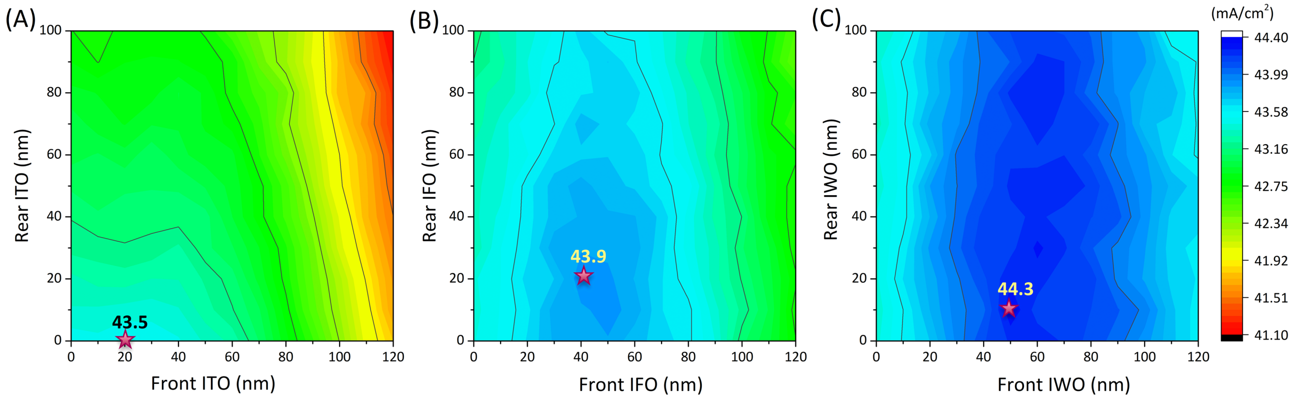

FIGURE 2 The simulated implied photocurrent densities in c-Si absorber ($J_{c\text{-}Si}$) as a function of front side TCO and SiO_x thicknesses for (A) ITO-, (B) IFO-, and (C) IWO-based bifacial SHJ devices. Constant 100-nm-thick SiO_x layers were utilized on top of TCO and on both sides of the wafer. The stars show the positions corresponding to the highest $J_{c\text{-}Si}$ values

To summarize, from the optical point of view, the optimal front TCO thicknesses are dependent on the TCO type. For the ITO-based SHJ devices, the thinner, the better. While for IFO- and IWO-based devices, appropriate thicknesses are required to ensure good optical performance. Table 1 shows the optical evaluations of SHJ devices with reduced TCO thicknesses, in which the DLARC optimizations for both mono- and bi-facial cells are included. The cases of single-layer ARC of TCO act as the references. One can see that, with respect to the reference devices, applying DLARC on the front side of mono-facial device helps to reduce the TCO consumption to some extent, which is typically below 33% reduction. At the same time, the $J_{c\text{-}Si}$ could be improved by up to 1.0 mA/cm^2 for ITO-based devices and 0.7 mA/cm^2 for IFO- and IWO-based devices, respectively. By contrast, the bifacial device design provides the most effective way to reduce the TCO consumption, meanwhile boost the optical performance of the device. Assuming a rear side illumination of 100 W/m^2, with respect to the reference cell, the bifacial cell could potentially improve the $J_{c\text{-}Si}$ by up to 5.0 mA/cm^2, 4.3 mA/cm^2, and 4.0 mA/cm^2, for ITO-, IFO-, and IWO-based devices, respectively. We note that with favorable albedo settings, the current improvements could be even higher.[43]

3.2 | Electrical evaluations regarding TCO reduction in SHJ

3.2.1 | Lateral transport

To realize such optical potential in device level, the electrical properties regarding the charge carrier transport behavior need to be considered. Figure 3A illustrates the schematic electron and hole transport paths towards the metal grid in the SHJ structure. As for the electron contact at the front side (*n*-contact), the lateral carrier transport layer can be either the c-Si absorber or the front TCO layer. Similarly, for hole contact at the back side (*p*-contact), the lateral carrier transport layer can be either the c-Si absorber or the rear TCO layer. In dark condition, the resistivity of c-Si bulk is normally higher than that of TCO layer. However, thanks to the excess carries that are generated with illumination, the resistivity of the c-Si material bulk could be largely reduced. For a more practical evaluation of the lateral conductivity of the materials, the parameter of sheet resistance (R_{sh}), rather than the resistivity (ρ), was utilized in this section. Figure 3B illustrates the calculated sheet resistance (R_{sh}) versus excess carrier density (Δn) of our lab-use wafer under illumination, following $R_{sh} = \frac{1}{(qn\mu_n + qp\mu_p)t}$, in which q is elementary charge, n and p are electron and hole concentrations, respectively, μ_n and μ_p are the electron and hole mobilities, respectively, t is the thickness of the layer (wafer in this case). The μ_n of 1300 cm^2 V^{-1} s^{-1} and μ_p of 450 cm^2 V^{-1} s^{-1} were utilized in the calculation.[44] The separate R_{sh} curves for electrons and holes are also included in Figure 3B. Figure 3C shows the measured R_{sh} data for TCOs deposited on glass with varied thicknesses at 25 nm, 50 nm, and 75 nm. All the films show a decreasing trend with thickness reduction, which is expected since R_{sh} is thickness-dependent ($R_{sh} = \rho/t$, where t is the thickness of the TCO layer). Figure 3D illustrates the data points of (N_e, μ_e) of the TCO layers from Hall measurements, that is, electron mobility (μ_e) versus corresponding carrier densities (N_e) plot. Resistivity (ρ) lines are also provided according to the relation $\log(\mu_e) = -\log(N_e) + \log(1/\rho e)$.[45] One can see that, with the TCO thicknesses reducing from 75 nm to 25 nm, the ρ values decrease to different extents for different TCOs. Therefore, the R_{sh} change in Figure 3C is related to the changes of both ρ and t.

Furthermore, from a comparison between Figure 3B and Figure 3C, one can see that the $R_{sh,e}$ in the wafer is comparable with that of 75-nm-thick TCO layers at the Δn region that corresponds to implied maximum power point (iMPP) appearing at 0.2 suns illumination. When the iMPP appears at the Δn region of 1 sun illumination, the $R_{sh,e}$ in the wafer is lower than that of the standard 75-nm-thick TCO layers. This implies that the c-Si absorber is able to provide efficient lateral electron transport towards metal contacts during operation, which has been proven in literature.[12,13,27] On the other hand, for the lateral hole transport, the $R_{sh,h}$ of the wafer is above 350 Ω/sq at 0.2 suns illumination, which is comparable with that the R_{sh} of 25-nm-thick TCO layers. The $R_{sh,h}$ of the wafer could be reduced to below 200 Ω/sq at 1 sun illumination. This implies that with the

TABLE 1 Optical evaluations of monofacial (MF) and bifacial (BF) SHJ devices with reduced TCO thicknesses

TCO	Device type	$t_{TCO,front}$ (nm)	$t_{TCO,back}$ (nm)	Δ t_{TCO} reduction	Δ $J_{c\text{-}Si}$ gain (mA/cm^2)
ITO	MF (ARC)	75	150	–	–
	MF (DLARC)	0–40	150	16–33%	0.5–1.0
	BF (DLARC)	0–50	0–50	56–100%	4.5–5.0
IFO	MF (ARC)	75	150	–	–
	MF (DLARC)	0–40	150	16–33%	0.3–0.7
	BF (DLARC)	20–70	0–70	38–91%	3.9–4.3
IWO	MF (ARC)	75	150	–	–
	MF (DLARC)	10–60	150	7–29%	0–0.7
	BF (DLARC)	40–80	0–100	20–82%	3.7–4.0

Note: MF cells with single-layer ARC act as the reference cells. The $t_{TCO,front}$ and $t_{TCO,back}$ (nm) denote the thicknesses of front TCO and back TCO, respectively.

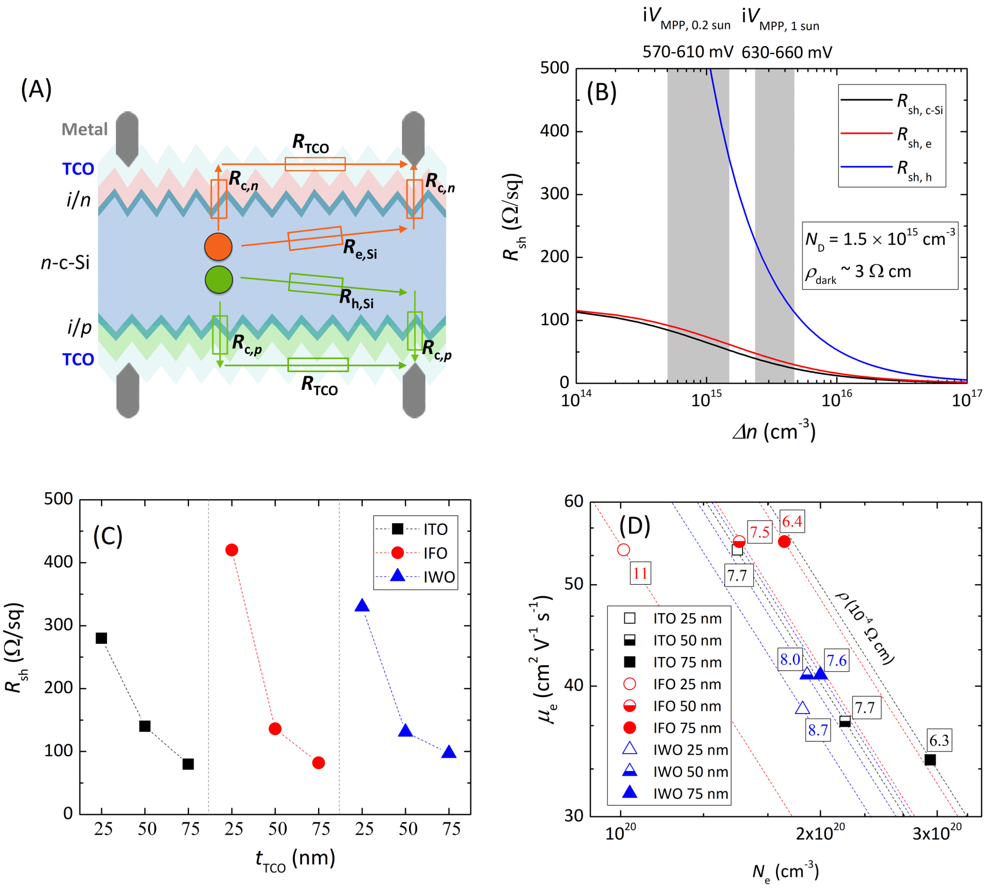

FIGURE 3 (A) Schematic electron and hole transport paths towards the metal grid in the bifacial SHJ structure. (B) Calculated sheet resistance (R_{sh}) versus excess carrier density (Δn) of our lab-use c-Si absorber under illumination. The separate R_{sh} curves for electrons and holes are also presented. The grey shadowed areas show the normally used Δn regions that maximum power point (MPP) appears. (C) Thickness-dependent R_{sh} of our ITO, IFO, and IWO layers. (D) Electron mobilities (μ_e) versus corresponding carrier densities (N_e) of the TCO layers with varied thicknesses, from Hall measurements. The resistivity (ρ) lines of the TCOs are also provided in (D)

development of high-quality SHJ cell precursors, the c-Si may also be able to provide effective lateral hole transport. Looking back to Figure 3A, a large portion of the lateral charge carrier transport towards local metal contacts could be accomplished by the silicon wafer itself during operation. As mentioned in Introduction, due to the possible technical constraints related to TCO-free solar cell fabrication, we only talk about SHJ solar cell design with reduced TCO use within the scope of this article.

3.2.2 | Vertical transport: Contact resistivity study

Figure 4A,B displays the contact resistivity values of *n*-contact ($\rho_{c,n}$) and *p*-contact ($\rho_{c,p}$) stacks in our SHJ device structure, respectively. The cross symbols represent non-ohmic contacts in our dark current–voltage measurements. For the *n*-contact, the $\rho_{c,n}$ values of ITO- and IWO-based samples show almost TCO thickness-independent characteristic. The $\rho_{c,n}$ values are maintained at ~120 mΩ cm^2 and ~80 mΩ cm^2 for ITO- and IWO-based samples, respectively. These values basically fall into the reported value range in Bivour.[13] Interestingly, the IFO-based samples show non-ohmic behaviors in *n*-contact stacks when 25-nm- and 50-nm-thick IFO layers are applied. With increasing the IFO layer thickness to 75 nm, ohmic contact is detected. However, the IFO-based samples with 75-nm-thick IFO layer use show a relatively high average $\rho_{c,n}$ values of 411 mΩ cm^2.

For the *p*-contact, all the $\rho_{c,p}$ values show significant TCO thickness-dependent characteristics. Interestingly, the ITO- and IFO-based samples show opposite trends, that is, with increasing the TCO thickness from 25 nm to 75 nm, the average $\rho_{c,p}$ values of the ITO-based samples increase from 114 mΩ cm^2 to 390 mΩ cm^2, while that of IFO-based samples decrease from 471 mΩ cm^2 to 175 mΩ cm^2. As for the IWO-based samples, we observed an average $\rho_{c,p}$ value of 148 mΩ cm^2 with 75-nm-thick IWO layer use, yet non-ohmic features when using 25-nm- and 50-nm-thick IWO layers. It may be worth noting that when the standard 75-nm-thick ITO is applied, the $\rho_{c,p}$ of 390 mΩ cm^2 is higher than our previously reported 222 mΩ cm^2 with the same thin-film silicon layer thickness use.[37] This might be mainly caused by the fine-tuned intrinsic layer in our laboratory. Besides, the ITO deposition parameters also changed, which might also induce a change in the $\rho_{c,p}$ values.

Combined with the band diagrams of the *n*- and *p*-contact stacks from TCAD simulations[29] as shown in Figure 5A, we provide our interpretation on Figure 4A,B as follows.

Regarding the *n*-contact (or electron contact), the TCO/doped silicon junction is isotype, in which the transport of electrons is simple since it only occurs in the conduction band. From the left part of Figure 5A, a low work function of the TCO layer is preferable due to a low electron transport barrier (Φ_{BN}) at the TCO/*n*-layer interface. Therefore, the observation of lower $\rho_{c,n}$ values of IWO than that in ITO samples in Figure 4A may indicate a lower work function of IWO

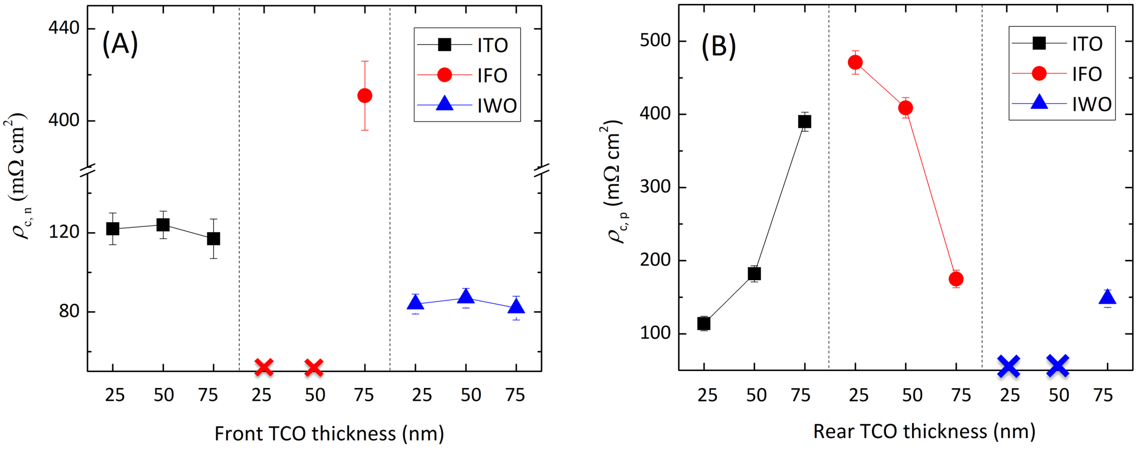

FIGURE 4 The contact resistivity of (A) *n*-contact, $\rho_{c,n}$, stack at the front and (B) *p*-contact, $\rho_{c,p}$, stack at the rear of our SHJ device structure for different TCO and variable thicknesses. The cross symbols represent non-ohmic contacts in the dark current–voltage measurements. The results are based on three groups of experimental data from one batch

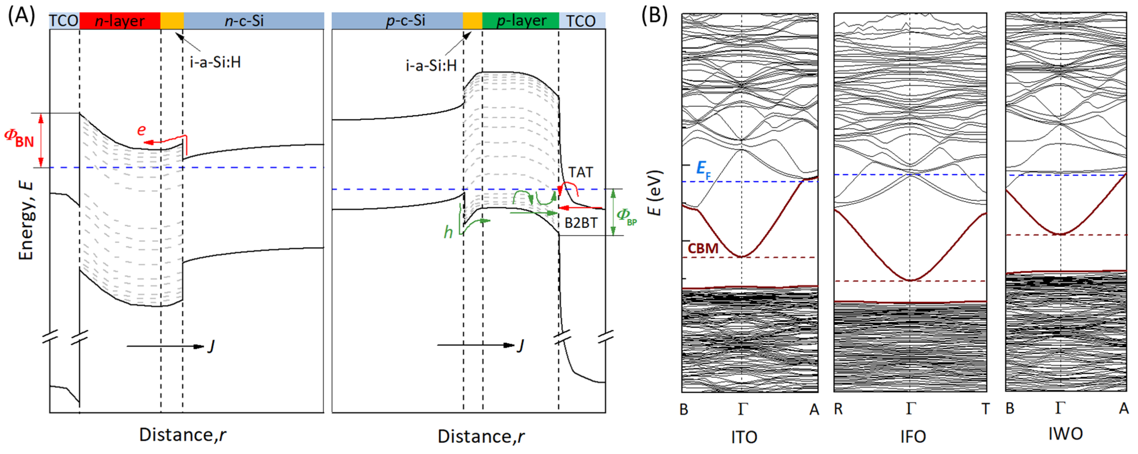

FIGURE 5 (A) Schematic band diagram of the charge carrier transport for *n*-contact (left part) and *p*-contact (right part). Corresponding transport barrier height of electrons (*e*) and holes (*h*) are marked as Φ_{BN} and Φ_{BP}, respectively. In *p*-contact, carrier transport mechanisms of band-to-band tunnelling (B2BT) and trap-assisted tunnelling (TAT) are indicated.[29] (B) Band structures of ITO, IFO, and IWO layers from density-functional theory simulations. The calculations were performed based on the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional, and the results are used for qualitative comparison analysis purposes among different TCO types

layer than ITO layer at the interface. While the IFO layer is speculated to hold the highest work function values among our tested lab-use TCO layers since the IFO-based samples show the highest $\rho_{c,n}$ values.

Figure 5B depicts the simulated band structures of the ITO, IFO, and IWO materials, respectively. The work function values of ITO, IFO, and IWO are calculated to be 4.42 eV, 4.26 eV, and 4.29 eV, respectively. The lower work function of IWO than ITO layer is in line with the observation that the IWO-based samples show lower $\rho_{c,n}$ values that ITO-based samples. While compared with ITO, the IFO material shows a slightly lower work function, but a visibly higher electron affinity (lower CBM position in Figure 5B). This makes it challenging to interpret the comparative properties between ITO- and IFO-based contact samples. Detailed investigation is ongoing. It is important to mention that our simulated work function data as shown in Figure 5B helps to some extent in qualitatively exploring the intrinsic material properties. However, one cannot directly associate the calculated data with the measured individual data, since the real deposited TCO thin films are influenced by multi-factors, such as deposition condition (target composition, temperature, pressure, O_2 flow, and residual water in the chamber),[46] substrate morphology,[38,40,41] and the adjacent doped silicon layers[19,38] or dielectrical layer[47,48] in practical conditions.[49,50]

For the *p*-contact (or hole contact), whose band diagram is shown in the right part of Figure 5A, the carrier transport is more complex than that in *n*-contact. In general, the TCO/*p*-layer interface acts as a recombination junction. Holes in the *p*-layer valence band recombine with electrons in the TCO conduction band. As elaborated by Procel et al.,[29] the $\rho_{c,p}$ variations could follow different combinative trends, depending on the dominating carrier transport mechanism(s). In this scenario, $\rho_{c,p}$ can be significantly influenced by the energy alignment of the *p*-layer with the TCO, which is affected by the hole transport barrier (Φ_{BP}) and/or different tunnelling mechanisms, as indicated in the right part of Figure 5A. Presumably, for the ITO-based samples, with reducing ITO thickness, the energy alignment at the TCO/*p*-layer interface is improved due to a possibly increased work function of ITO layer. The better the alignment, the better the transport of carriers (i.e., lower $\rho_{c,p}$).[51] As for the IFO and IWO cases, we speculate that with increasing the TCO thickness, the N_e change negligibly affects the energy alignment at the TCO/*p*-layer interface. However, N_e increase allows more energy states available for collecting holes from the *p*-layer,[29] thus facilitates a reduction of $\rho_{c,p}$ for thicker TCO use. Further research remains to be carried out to confirm the above hypothesis.

3.3 | Bifacial SHJ solar cell results

From previous observations, for the *n*-contact stack, the *n*-type c-Si absorber could provide sufficient lateral electron transport towards local metal contacts. Besides, low vertical contact resistance could be ensured by utilizing the ITO or IWO layers, since they show low WF values and the $\rho_{c,n}$ is observed to be independent of the TCO thickness. This means that ITO and IWO layers are both promising options for the *n*-contact side of the SHJ solar cell design with reduced TCO use. To verify this hypothesis, we fabricated monofacial rear emitter, ITO-, IFO, and IWO-based SHJ devices, with varying the front TCO layer thickness from 25 nm to 75 nm; 100-nm-thick SiO_x layers are applied on the illuminated side. The results are shown in Figure S5. One can see that IFO- and IWO-based SHJ devices show the best optical performance, while ITO- and IWO-based devices show the best fill factor values (electrical properties). Consequently, the best monofacial cell was observed among the IWO-based devices, in which the 50-nm-thick front IWO layer is applied. Elaborate analysis on the performance of our monofacial cells is provided in Supporting Information, where the comparison between simulated $J_{c\text{-}Si}$ and measured J_{SC_EQE} is also included. Considering the high ρ_c values in IFO-based contact samples and the low *FF* values in IFO-based monofacial SHJ devices, we only included ITO and IWO layers in our final bifacial cells. Besides, the IWO cells are proven to exhibit the best optical performance (Figure 2 and Figure S5), and 25-nm-thick ITO shows the most

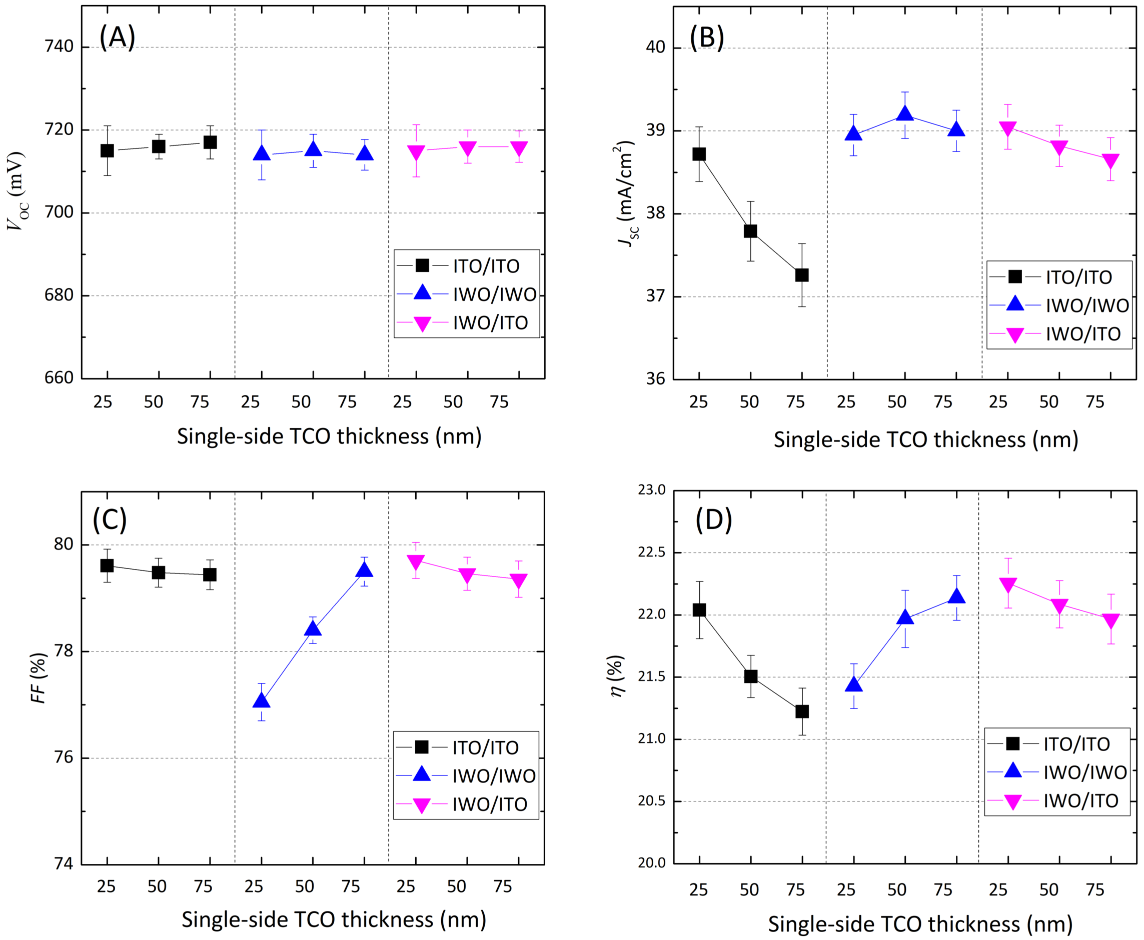

FIGURE 6 The measured (A) open-circuit voltage, V_{OC}, (B) short-circuit current density, J_{SC}, (C) fill factor, *FF*, and (D) power conversion efficiency, η, of bifacial SHJ device with varied TCO thicknesses of 25 nm, 50 nm, and 75 nm on both sides; 100-nm-thick SiO_x layers are applied on top of the TCOs on both sides. The results are based on three devices on the same wafer from one batch of processes. The data are the results from front side illumination

promising results in the hole-collecting *p*-contact (as shown in Figure 4B); thus, we included a novel type of IWO/ITO-based bifacial cell in this work.

We fabricated Cu-plated bifacial SHJ devices, with front and rear TCOs of ITO/ITO, IWO/IWO, and IWO/ITO. For each type, three TCO thicknesses were tested on both sides of the device, which are 25 nm, 50 nm, and 75 nm; 100-nm-thick SiO_x layers are applied on top of the TCOs on both sides. Figure 6A–D shows the measured bifacial SHJ solar cell results from *n*-side illumination. From Figure 6A, the V_{OC} values are similar to that are observed in monofacial cells (as shown in Figure S5a). From Figure 6B, the average J_{SC} values of ITO/ITO- and IWO/ITO-based devices show decreasing trends with increasing the TCO thicknesses on both sides. Especially, the ITO/ITO-based solar cell show a dramatic J_{SC} decrease with TCO thickness increase, reflecting a notably higher parasitic absorption in the thick TCO film. This could be related to the fact that as compared to the thin ITO film, thick ITO film is more absorptive in nature (i.e., higher absorption coefficient, as indicated by a higher N_e in Figure 3D[18]) and higher TCO thickness induces higher absorptance. As for the IWO/IWO-based devices, the average J_{SC} values do not show significant change among the tested cells, which are 38.95 mA/cm^2, 39.19 mA/cm^2, and 39.00 mA/cm^2, for devices with double-side 25-nm-, 50-nm-, and 75-nm-thick IWO layers, respectively. Combining our optical simulation results in Figure 2, the decreasing trend in the average J_{SC} values of ITO- and IWO/ITO-based devices could be attributed to the increasing parasitic absorption when increasing the ITO layer thickness. From Figure 6C, surprisingly, with increasing the ITO thickness from 25 nm to 75 nm, we observed slightly decreased *FF* values in the ITO-based devices. We note that the *FF* of a real solar cell is not only influenced by the vertical contact resistance, but also lateral carrier transport contributions on both sides of the wafer. According to Figure 4, with increasing the ITO thickness from 25 nm to 75 nm, the $\rho_{c,n}$ almost remains constant yet the $\rho_{c,p}$ notably increases. We presume that the increasing trend in $\rho_{c,p}$ in the vertical hole transport is somehow compensated by the decreasing trend in R_{sh} in the lateral hole transport (as shown in Figure 3C). The overall results from lateral and vertical hole transports at the *p*-contact side could be the driving force behind our observed *FF* trend in the ITO-based devices. As for the IWO-based devices, with increasing the IWO layer thickness from 25 nm to 75 nm, the *FF* shows an increasing trend. The high *FF* in the 75-nm-thick IWO-based devices could be attributed to both the low $\rho_{c,p}$ in the vertical hole transport (Figure 3B) and the low R_{sh} in the lateral hole transport (as shown in Figure 3C). Furthermore, with increasing the TCO thickness from 25 nm to 75 nm, the IWO/ITO-based devices show a similar *FF* trend with ITO-based devices. This can be expected from previous observations in Figure 3, Figure 4, and the separate ITO and IWO cases in Figure S5c. Figure 6D shows the overall power conversion efficiencies of the bifacial devices from front side illumination. Efficiencies above 22% were obtained in the IWO/ITO-based devices in the 25 nm/25 nm case. The best cell performance in this batch is shown in Table 2. With respect to a reference bifacial solar cell with 75-nm-thick TCO on both sides, such a total TCO thickness of 50 nm represents a 67% TCO reduction.

It may be noteworthy on the following aspects: (i) regarding the hybrid IWO/ITO use, we also performed optical simulations on the

TABLE 2 The device parameters of the best bifacial SHJ solar cell in the experimental series with using the same TCO thickness on both sides of the wafer

TCOs	t_{TCOs} (nm)	Illuminated side	V_{OC} (mV)	J_{SC} (mA/cm^2)	*FF* (%)	*η* (%)
IWO/ITO	25/25	front	721	39.20	79.57	22.50
		rear	717	38.72	79.91	22.19

Note: 25-nm-thick front IWO in *n*-contact and 25-nm-thick rear ITO in *p*-contact were applied.

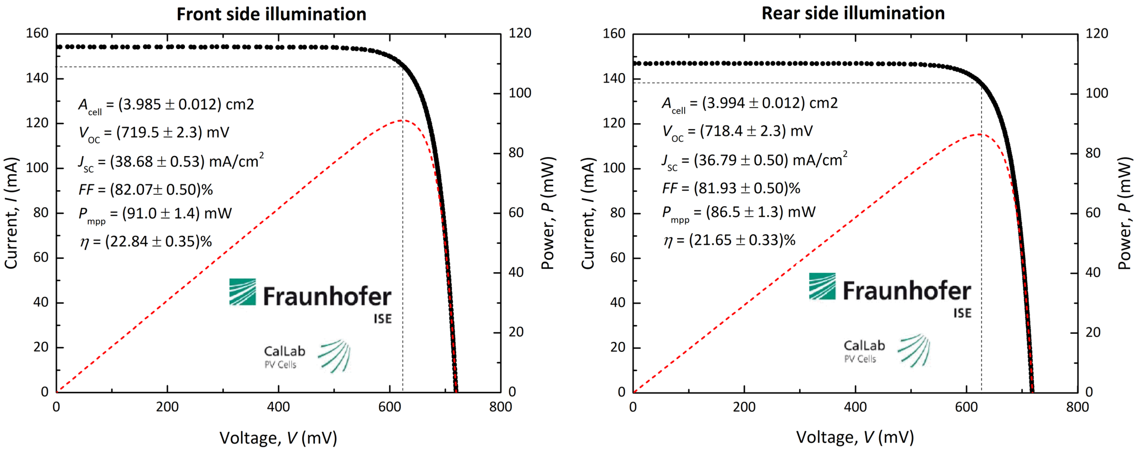

FIGURE 7 Certified solar cell parameters of our champion bifacial SHJ device, in which 25-nm-thick front IWO in *n*-contact and 75-nm-thick rear ITO in *p*-contact were utilized

IWO/ITO-based bifacial cell structures (data not shown). Results show that the optimal $J_{c\text{-}Si}$ (44.3 mA/cm^2) is the same as that obtained in Figure 2C, which appears when 50-nm-thick front IWO and 0-nm-thick back ITO are applied; (ii) regarding the J_{SC} reading in Figure 6B, the values were collected from single-side illumination, thus are even lower than that of monofacial solar cells (opposite to the expectation from Table 1). Besides, the possible optical overestimations in our simulation results (as shown in Figure S4 and Figure 2) are discussed in monofacial case (see Supporting Information, Figure S6); (iii) regarding the further improvement, the *FF* of our bifacial solar cells in Figure 6 are generally below 80%. Considering our *n*-c-Si absorber possibly provides sufficient lateral electron transport for the *n*-contact (see Section 3.2.1), and the contact resistance between IWO and *n*-type doped silicon layer is sufficiently low (see Section 3.2.2), we suspect that the carrier transport of our bifacial cell is still limited by the *p*-contact.

Furthermore, with utilizing a modified SHJ solar cell precursor and increasing the ITO thickness on the *p*-side to 75 nm, we realized notably increased *FF* and further improved solar cell efficiencies. The certified solar cell parameters of our champion bifacial SHJ device are shown in Figure 7. The front side efficiency is 22.84%, and bifaciality factor is calculated to be 0.95.

4 | CONCLUSIONS

We utilized TCOs with different opto-electrical properties, which are tin-, fluorine-, and tungsten-doped indium oxides, namely, ITO, IFO, and IWO. By adding a double layer anti-reflection coating formed by TCO/SiO$_x$ layer stacks on the illumination side(s), we performed optical simulations with varied TCO/SiO$_x$ stacks on both mono- and bi-facial SHJ solar cells. Results show that (i) bifacial solar cell architecture provides the most effective way to reduce TCO usage, and (ii) appropriate TCO thicknesses are needed to ensure an optimal optical response. Furthermore, with applying TCO thicknesses of 75 nm, 50 nm, and 25 nm, we performed electrical evaluations from both lateral and vertical charge transport perspectives. Our IFO and IWO are found to be favorable for *p*-contact and *n*-contact, respectively. While for ITO, it can work well in both *p*-contact and *n*-contact, but thinner ITO shows lower contact resistance in *p*-contact, although its sheet resistance becomes higher. TCO thickness-dependent contact properties for both *n*-contact and *p*-contact were tentatively interpreted by means of first-principles density-functional theory study. Based on the observations, preferable bifacial SHJ solar cells with reduced TCO use are designed and fabricated. With applying 25 nm-thick IWO on the front side and 25-nm-thick ITO on the rear side of the device, we obtained front side efficiencies >22%. This represents a 67% TCO reduction with respect to a reference bifacial solar cell with 75-nm-thick TCO on both sides. Moreover, with utilizing modified SHJ solar cell precursors and further TCO adjustment, our champion bifacial SHJ solar cell showed front side efficiency of 22.84%. The bifaciality factor is 0.95.

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DATA AVAILABILITY STATEMENT

The data that supports the findings of this study are available in the supplementary material of this article.

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SUPPORTING INFORMATION

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