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Experimental Qualification of a Low-Noise Charge-Sensitive ROIC with Very High Time Resolution

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***Abstract*—Small charge detection is used for a wide range of applications: advanced industrial process control, experimental physics and space instruments, and material testing and medical imaging. These applications give rise to the development of a wide variety of charge-sensitive readout integrated circuits (ROICs). The trend in the state-of-the-art systems is to design low-noise and low-power readout electronics with a low detection error rate and small silicon area occupation, allowing the pixelization of the detector area. This paper presents the methodology and the test setup for the challenging experimental characterization of a state-of-the-art, high time-resolution, low-noise, power-efficient, charge-sensitive ROIC intended for counting single particles detected by a silicon PIN detector. The ROIC is designed to detect charge portions as small as 160 aC, with 0.14 mW power consumption. For every charge pulse of the detector, the ROIC generates voltage signals with a peak amplitude of 29.45 mV, a rise time of 2.56 ns, and an SNR above 20. Detailed information about the operation principle of this ROIC, designed in TSMC 40-nm MS/RF CMOS technology, is reported in a previous publication.**

Keywords— readout integrated circuit ROIC, charge-sensitive amplifier, low-noise, power-efficient, high time-resolution, wideband, data acquisition, pixel

I. INTRODUCTION

Highly developed instrumentation and imaging devices have become powerful inspection and metrology tools in the modern world of industrial technology. Advances in electronics, fast data processing, and image reconstruction have enabled the development of very elaborate investigation techniques that are now used in many different fields of science and many domains of applications [1]. The availability of high-resolution pixelated detectors has led to manifold technological advances in particle physics, astrophysics, materials science, medicine, biology, and many other application domains [2] - [5].

The diversity of applications and system constraints have motivated the development of a variety of front-end architectures. These are usually attained by cascading a few stages (Fig. 1), including a preamplifier which provides the interface for the detector, a signal shaper for generating an output signal with a well-defined shape, and a threshold discriminator for distinguishing the signal concerning the noise level as well as digitizing the hit data [6].

The trend in the state-of-the-art readout front-ends is to design low-power, high time-resolution, and high-accuracy readout electronics with low silicon area occupation. The weak input signal can be looked at as a beam of particles reaching the surface of a detector. This results in a particle-counting mode of operation for the ROIC, with high time-resolution of the arrival moment of each particle of only a few nanoseconds. The quality of operation then is determined by the counting error rate: the number of missed or false counts compared to the total number of counts per unit time. Accurate detection of weak charge signals with a high event rate requires high bandwidth and low-noise readout electronics. This poses significant challenges for the experimental verification of the performance of such circuits [7], [8].

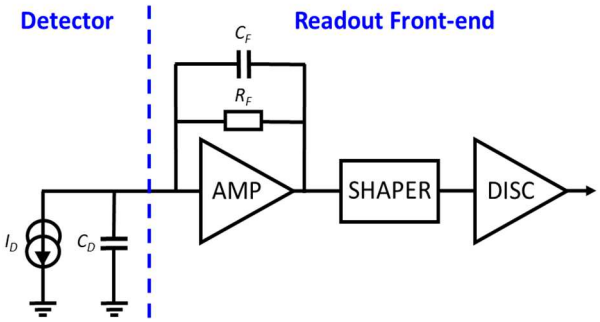

Fig. 1. Simplified block diagram of the readout front-end electronics.

Most of the reported solutions are using as a first stage either a transimpedance amplifier (TIA) or a charge-sensitive amplifier (CSA) [9], [10]. The TIAs are known for being noisier and more power hungry, compared to the CSAs. While the CSAs suffer from inter-symbol interference (ISI), resulting in counting one particle multiple times due to the tail of the charge-sensitive amplifier (CSA) output signal. Fortunately, there are solutions to mitigate this problem with the help of additional power efficient stages (a signal shaper, for example).

In [12] a charge-sensitive ROIC is proposed, designed to convert a charge signal of $160\,aC$ (equivalent to 1000 electrons) generated by a PIN detector, into a voltage signal with a peak amplitude of $V_P = 30.6\,mV$, with a rise time of $t_r = 2.35\,ns$, and a signal-to-noise ratio (SNR) of 22.7, when configured in high-gain and slow mode. The experimental verification of the performance of a device with such specifications is a big challenge of its own. It requires the use of auxiliary functional blocks integrated on the same chip, as well as an advanced external test set up and dedicated test algorithms.

This paper presents the test setup and the set of challenging experimental qualification tests implemented to monitor and

characterize the CSA functionality and performance. Section II introduces the measurement setup and the internal block diagram of the charge-sensitive ROIC. In Section III, the building blocks of the ROIC (i.e. detector model, CSA, and voltage buffer), as well as the operation principle, are presented. Section IV provides the experimentally obtained performance results. The paper ends with conclusions.

II. ROIC Qualification Setup

Proper characterization and assessment of the charge-sensitive ROIC necessitate a competent and qualified test setup, and high-precision lab devices. The qualification test setup used (Fig. 2) consists of a power supply and a current source to bias the chip and generate the charge injected into the CSA, an FPGA device to program and then test the charge-sensitive ROIC, and an oscilloscope and a multimeter for signal monitoring and measurement. To reduce the peripheral noise injection and avoid loading effects, all of the test setup devices are connected to the chip through isolation buffers.

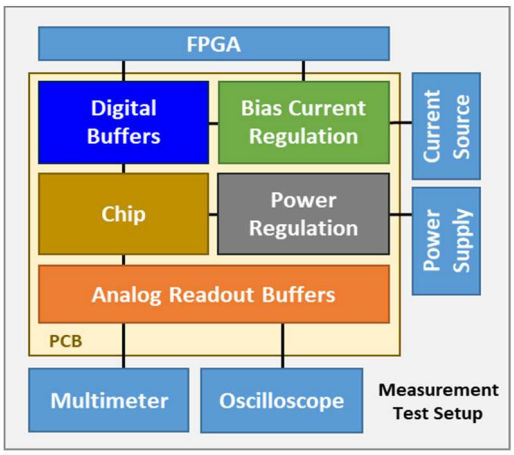

Fig. 2. Measurement and qualification test setup.

Since CSA is treated as the most critical block of the ROIC, additional auxiliary and peripheral blocks are implemented on the chip together with the CSA to facilitate the testability of its performance (Fig. 3). These auxiliary blocks are: a detector emulator to provide the amount of charge necessary for detection with the help of a current generator and a current regulator, when externally triggered; a wide-bandwidth voltage buffer to avoid loading effects for signal monitoring purposes; a power regulator to provide proper biasing; and a set of programmable configuration switches to change the operating modes of the building blocks.

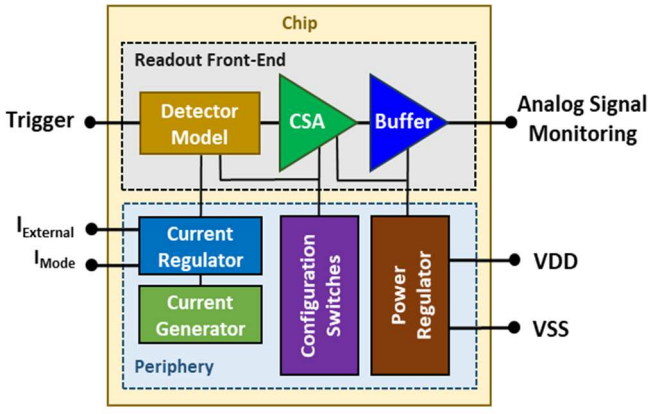

Fig. 3. Internal block diagram of the ROIC.

The FPGA device, through a high-speed low-voltage differential signaling (LVDS) interface, programs the status of the configuration switches to test the ROIC functionality and evaluate the operation efficiency under different working conditions. In the programming phase, the following parameters for the ROIC can be set: the value of the equivalent detector capacitance (C_D), and the value of the CSA feedback components (C_F and R_F) which sets its gain and time constant.

III. ROIC Building Blocks

A. Detector Model

In this set of experiments and throughout this work, in order to only focus on the operational accuracy of the CSA, the detector is substituted by a network which models its characteristics. As shown in Fig. 4, this network contains an array of capacitors in parallel with a digitally controlled current source (DCCS), which represents the detector equivalent capacitance C_D and equivalent charge pulse, respectively. The current regulator block generates the desired current amplitude for the DCCS, which includes a switch followed by a buffer to deliver the generated current to either the CSA input node or an arbitrary node depending on the status of the Trigger pin. The FPGA device would fire the Trigger pin through a chain of digital pulses for the desired period and time width to generate a sequence of small and fast current pulses (i_s).

The current regulator block could be biased by either an internal current generator implemented on the periphery of the chip ($I_{Internal}$) or an external current generator ($I_{External}$) by the status of the I_{Mode} pin. Using the internal generator, the regulator block is biased with a fixed current amplitude; however, in the case of the external generator, the current amplitude could be tuned, providing a higher order of flexibility in terms of adjustment and calibration of the DCCS current amplitude (i_s). Thus, a set of much more accurate test results could be obtained with the detector model.

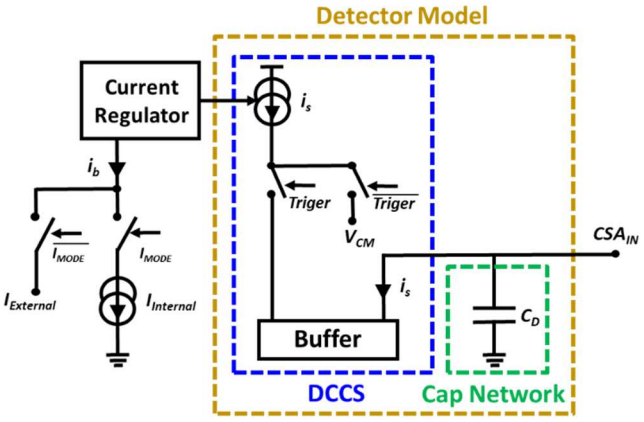

Fig. 4. Simplified schematic of the detector model.

Emulating the signal generated by a real detector with an equivalent model is the main challenge. Principally, the current pulse induced by the moving charge inside the detector toward its electrodes emerges as a voltage signal after the preamplifier. The shape of this voltage signal is a function of the time constant of the preamplifier feedback network (τ_F). If the time constant is larger than the detector charge collection time (t_c), which is the case for the CSA, the detector current signal is integrated into the feedback capacitor C_F [11]. Therefore, the charge stored in C_F represents the charge pulse

produced within the detector plates. The integrated charge will finally discharge through the feedback resistor (R_F), and the shape of the voltage signal after the preamplifier will become largely independent of the shape of the detector current pulse, leading to a voltage that can be represented as:

$$V = \frac{Q}{C_F} e^{\frac{-t}{\tau_F}} \quad (1)$$

where Q is the overall charge produced in the detector, and $\tau_F = C_F R_F$. In the CSA, the time constants of the feedback network are $\tau_{F_{Fast}} = 27.13$ ns in fast mode and $\tau_{F_{Slow}} = 53.86$ ns in slow mode, which are larger than the detector charge collection time $t_c = 1.8$ ns; hence, the current signals produced within the detector can be emulated by square-wave current pulses with the same equivalent charge [11]. In this regard, the FPGA must generate a chain of trigger pulses with a certain pulse time width for a fixed amplitude of current (i_s) to generate current pulses with an equivalent charge of 160 aC for every individual pulse [8]. The generation of each current pulse by the DCCS corresponds to the charge generated by the detector upon the landing of an event. The detector model consumes 2.5 µW of static power and occupies an area of 26 µm × 16 µm.

B. Charge-Sensitive Amplifier

The charge-sensitive amplifier (CSA), as illustrated in Fig. 5, consists of the following functional blocks [12]: a core amplifier followed by a common source stage, and a current conveyor (called an ICON Cell) in the feedback network. These blocks implement a large feedback resistance equivalent to $R_F = (K+1) \times R_1$ using a physical resistor of R_1 as proposed in [13], where K is the mirroring factor.

For observing the CSA performance under different operating conditions, the value of some parameters can be tuned in the programming phase. By changing the value of the feedback capacitance C_F, the CSA can operate in high-gain ($C_F = 5$ fF) or low-gain ($C_F = 10$ fF) mode, while by changing the value of the equivalent feedback resistance R_F, the CSA can operate in slow ($R_1 = 133$ KΩ) or fast ($R_1 = 67$ KΩ) mode. A complete set of post-layout simulation tests representing the CSA operative characteristics for different values of programmable parameters are published in [12]. Verified by experimental tests, the CSA consumes 0.14 mW of power and occupies an area of 30 µm × 15 µm.

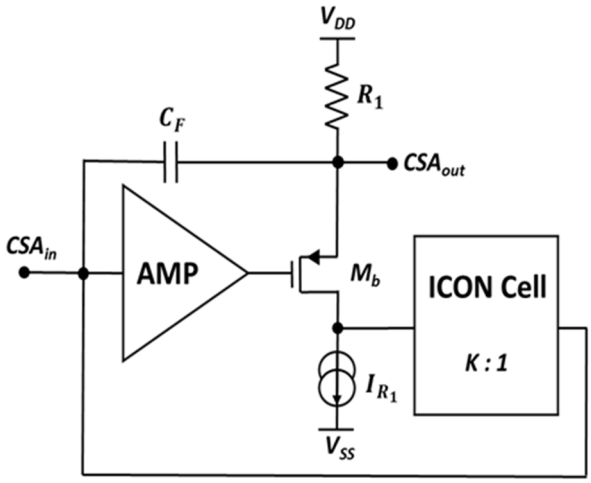

Fig. 5. Detailed schematic of the CSA with the ICON Cell.

C. Voltage Buffer

To monitor the voltage signal generated by the CSA without the loading effect of the impedances associated with the pad network, bond wire, and PCB traces, the CSA is followed by a wide-bandwidth unity gain voltage buffer to provide impedance transform. In practice, the protection is realized by driving the load with a current generated by this voltage buffer stage rather than the CSA. Figure 6 presents a schematic of the voltage buffer consisting of a core amplifier (differential stage followed by a common-source stage) and a unity feedback path.

Post-layout simulation results indicate that the designed voltage buffer has a bandwidth of 920 MHz with a gain of ~1 for a load with an equivalent impedance of $C_L = 200$ fF making it a good candidate for monitoring the fast-rising voltage signals of the CSA. Verified by experimental tests, the voltage buffer consumes 0.15 mW of power and occupies an area of 16 µm × 14 µm.

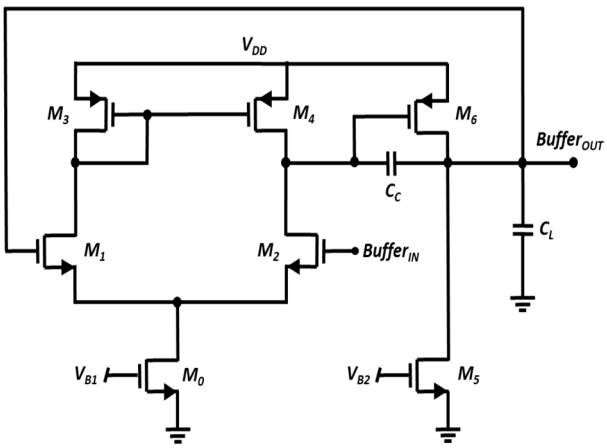

Fig. 6. Schematic of the unity gain voltage buffer.

IV. Experimental Results

The goal of the experimental tests presented is to evaluate the data acquisition process by characterizing the voltage signal generated by the CSA for different sets of current signals provided by the detector model. For this purpose, the FPGA must trigger the DCCS block with a pattern of logical '0s' and '1s'. Every trigger pulse must be assigned to a time frame of 2.5 ns; hence, a reference clock with a 400 MHz frequency is implemented on the FPGA, allowing a trigger rate up to 4×10^8 triggers/s. To emulate the detector properties, every charge pulse generated by the DCCS must have a time width of 1.8 ns, which, in combination with a current amplitude of $i_s = 88$ nA, results in an equivalent charge of 160 aC (1000 e^-). Hence, the FPGA trigger signals representing logical '1' must have a time width of 1.8 ns. Figure 7 illustrates the trigger pulses generated within the time frames of 2.5 ns by the FPGA for the '01000100' logical pattern.

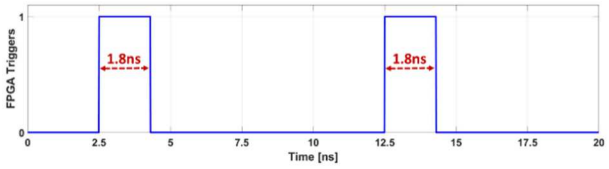

Fig. 7. FPGA trigger pulses within time frames of 2.5 ns for the '01000100' logical pattern.

To observe the operation and performance of the CSA under different working conditions, the values of the tunable parameters (C_D, C_F, R_F) are changed by programming the configuration switches. The goal is to verify if the CSA can convert the detector current pulses into voltage signals with an SNR > 14 and a rise time $t_r < 2.5$ ns (within one time frame) for every operating mode of the CSA. Once the CSA is programmed into the desired mode, the DCCS is fired with typical patterns of trigger pulses and the generated voltage signals are collected. Figure 8 illustrates the PCB designed for the experimental qualification of the chip. It is worth mentioning that the experimental tests are repeated 100 times to reduce the noise and eliminate the high-frequency components of the signal during the characterization; thus, the reported values are averaged 100 times.

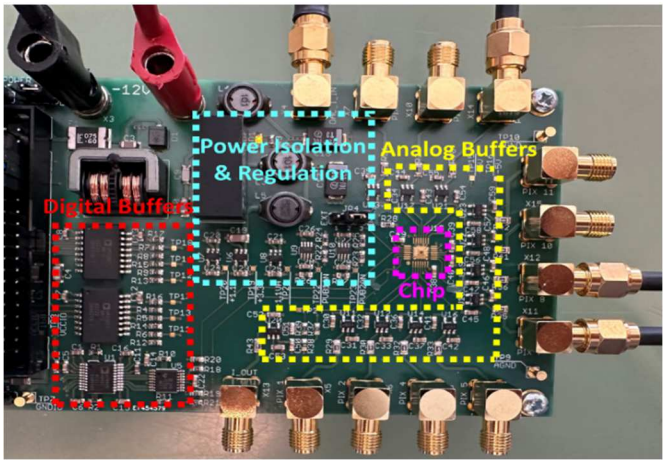

Fig. 8. PCB designed for experimental qualification of the chip.

Figure 9 presents the measured voltage signal of the ROIC for a CSA configured in high-gain mode ($C_F = 5$ fF) once it is fired by a single trigger pulse from the FPGA. The signals have average amplitudes of $V_{Amp}|_{Slow} = 29.45$ mV and $V_{Amp}|_{Fast} = 28.53$ mV for the slow and fast modes, respectively. Figure 10 presents the measured voltage signal of the ROIC for a CSA configured in low-gain mode ($C_F = 10$ fF) once it is fired by a single trigger pulse from the FPGA. The signals have average amplitudes of $V_{Amp}|_{Slow} = 16.47$ mV and $V_{Amp}|_{Fast} = 13.64$ mV for the slow and fast modes, respectively. The blue lines represent the slow mode while the red lines represent the fast mode.

Table I and Table II summarize the measured characteristics of the charge-sensitive ROIC (including the CSA and the voltage buffer) for different values of feedback resistance R_F and an ICON Cell with a mirroring factor of $K = 80$ in the high-gain ($C_F = 5$ fF) and low-gain ($C_F = 10$ fF) modes, respectively. As seen, in both the slow and fast modes, the ROIC can fulfill the requirements of the SNR and rise time for either of the gain modes. The chip has a total power consumption of less than 0.3 mW and occupies an area of 60 µm × 37 µm.

The value of the detector equivalent capacitance C_D is a critical parameter for the bandwidth of the CSA and hence the SNR. To probe into the effect of the detector equivalent capacitance value, the DCCS is fired by a single trigger pulse for every programmable value of the C_D. Thanks to the configuration switches, the value of the C_D could be swept along 20 fF to 50 fF on the chip. Figure 11 plots the SNR as a function of the detector equivalent capacitance C_D for a CSA programmed in slow and high-gain modes. The green dotted line corresponds to the SNR obtained through post-layout simulations while the blue solid line represents the SNR attained through experimental measurement tests. Following the slope of the blue sold line, the red dashed line corresponds to the estimation of the SNR for $C_D = 10$ fF with no capacitance connected to the CSA. It is worth mentioning that, due to area limitations, these two later cases of C_D could not be implemented in the chip for experimental qualification. As demonstrated, the SNR improves as the value of the detector equivalent capacitance (C_D) diminishes and the experimentally obtained values approach the post-layout simulation results with a reasonable error.

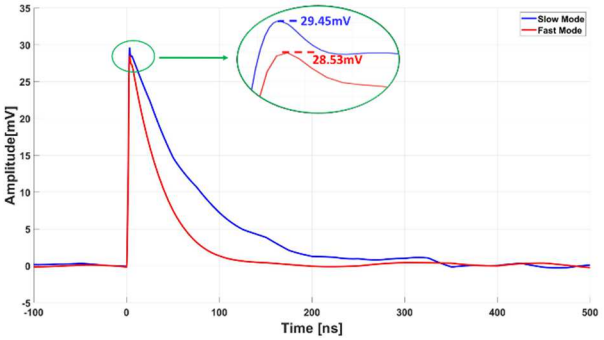

Fig. 9. Measured voltage signal of the ROIC with $C_F = 5\,fF$ (high-gain mode) for the slow and fast modes in blue and red, respectively.

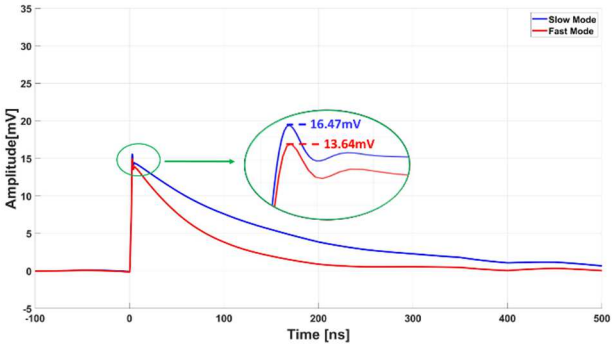

Fig. 10. Measured voltage signal of the ROIC with $C_F = 10\,fF$ (low-gain mode) for the slow and fast modes in blue and red, respectively.

TABLE I. MEASURED CHARACTERISTICS OF THE ROIC FOR DIFFERENT VALUES OF FEEDBACK RESISTABCE IN HIGH-GAIN MODE

Operation Mode	V_{Amp} [mV]	σ_{Noise} [mV_{rms}]	SNR	t_{rise} [ns]	t^*_{tail} [ns]
Slow ($R_F \approx 11$ MΩ)	29.45	1.43	20.59	2.56	286.91
Fast ($R_F \approx 5.3$ MΩ)	28.53	1.38	20.67	2.41	159.34

Discharge tail of the CSA voltage signal

TABLE II. MEASURED CHARACTERISTICS OF THE ROIC FOR DIFFERENT VALUES OF FEEDBACK RESISTABCE IN LOW GAIN MODE

Operation Mode	V_{Amp} [mV]	σ_{Noise} [mV_{rms}]	SNR	t_{rise} [ns]	t^*_{tail} [ns]
Slow ($R_F \approx 11$ MΩ)	16.47	0.91	18.1	2.27	537.64
Fast ($R_F \approx 5.3$ MΩ)	13.64	0.82	16.63	2.11	249.62

Discharge tail of the CSA voltage signal

Studying the CSA operation and the amplitude of the voltage signal generated for two consecutive triggers pulses is another important qualification test, as it will reveal the CSA performance in the case of signal pileup in its output. For this purpose, the DCCS is fired by '1100' and '1010' logical trigger patterns. The former pattern is meant to measure the voltage amplitude for the ROIC triggered in two consecutive time frames, while the latter corresponds to the addition of an idle time frame between the two trigger pulses. Measuring the amplitude of the voltage signal in either case allows the order of gain compression associated with the CSA to be estimated. By comparing the amplitude of the voltage signals of the aforementioned cases, the order of amplitude loss within an idle time frame can be calculated.

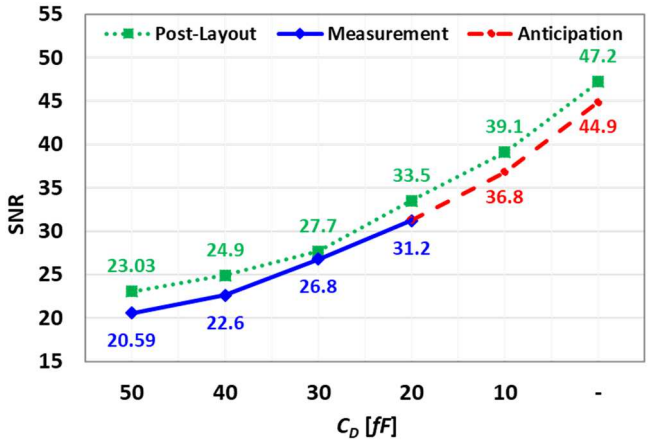

Fig. 11. SNR as a function of the detector equivalent capacitance C_D for a CSA programmed in slow and high-gain modes. The green dotted line and blue solid line represent the post-layout and measured results, respectively. The red dashed line is the estimation of the SNR.

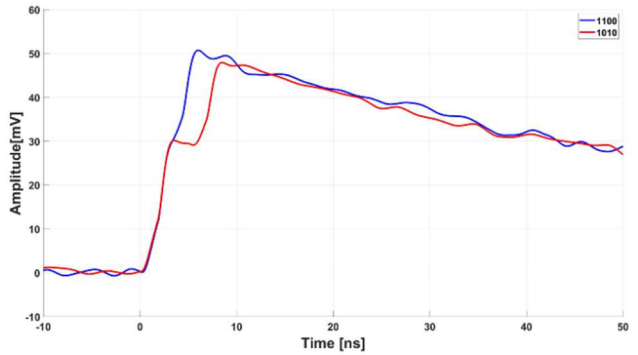

Fig. 12. Voltage signals of the charge-sensitive ROIC for '1100' and '1010' logical trigger patterns in blue and red once the CSA is configured in slow and high-gain modes, respectively.

Figure 12 illustrates the ROIC voltage signals for '1100' and '1010' logical trigger patterns in blue and red once the CSA is configured in slow and high-gain modes, respectively. The amplitude of the second voltage signal in the former case (blue line) is 50.47 mV while in the latter case (red line) it is 48.92 mV. In the case of the '1100' logical trigger pattern, by comparing the signal amplitude associated with the first and the second trigger pulses, it can be concluded that the ROIC has a 28.6% gain compression in the case of the signal pileup. The majority of this compression is imposed by the limited input dynamic range of the buffer block. For the buffer block, the design focus is on the bandwidth, rather than the input dynamic range, in order not to limit the time domain characteristics of the voltage signal for one trigger pulse. With respect to the post-layout simulation results, by measuring the ROIC voltage signal directly after the CSA (i.e. eliminating the voltage buffer), the CSA gain compression is 2.8%; however, the gain compression after the voltage buffer is 27.9 %, which is very close to the measured value and confirms that the voltage buffer is the major source of error. By subtracting the amplitude of the second voltage signals associated different trigger patterns, there is a 1.55 mV amplitude loss within 2.5 ns due to the idle time frame in the '1010' logical trigger pattern.

V. Conclusions

This paper presented the experimental characterization of a state-of-the-art, high time-resolution, low-noise, power-efficient, charge-sensitive ROIC intended for counting single particles detected by a silicon PIN detector. For proper characterization and assessment of the charge-sensitive ROIC, a dedicated test setup was created and high-precision lab measurement equipment was used. Additionally, some auxiliary blocks were designed and integrated in the same chip to facilitate the testability of the ROIC/CSA performance including: a network modeling the detector characteristics, a wide-bandwidth voltage buffer to avoid loading effects for signal monitoring purposes, a power and current regulator to provide proper biasing, and a set of programmable configuration switches to change the operating modes of the building blocks. Verified through experimental qualification tests, the charge-sensitive ROIC detects charge portions as small as 160 aC, with 0.14 mW power consumption. For every charge pulse of the detector, the ROIC, configured in slow and high-gain modes, generates voltage signals with a peak amplitude of 29.45 mV, a rise time of 2.56 ns, and an SNR of 20.59; however, in the fast mode, the generated voltage signal has a peak amplitude of 28.53 mV, a rise time of 2.41 ns, and an SNR of 20.67.

The presented solution is intended for accurate detection of a weak input signal comprising a beam of particles reaching the surface of a detector with a high time resolution of only a few nanoseconds. A follow-up to this work is in progress, focused on the additional functional blocks needed after the CSA, to realize the particle-counting mode by eliminating the tail of the CSA output signal.

Acknowledgment

This work started as a master's research project [13] and has been extended into a Ph.D. project at TU Delft, the Netherlands, supported by the Dutch Top Consortium for Knowledge and Innovation (TKI) HTSM.

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